

# LeCroy

CALIFORNIA

CAMAC MODEL 8212

DATA LOGGER

instrumentation  
for the study of  
transient phenomena

PALO ALTO, CA.

# technical information manual

CAMAC MODEL 8212

DATA LOGGER

## WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT  
**LeCroy / CALIFORNIA**  
PALO ALTO, CALIFORNIA

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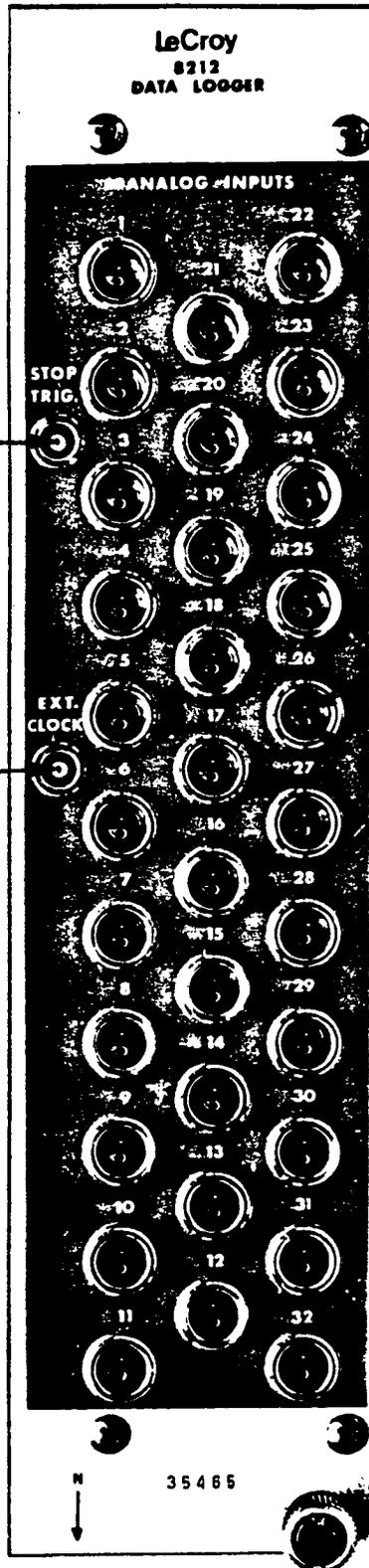
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FRONT PANEL PHOTOGRAPH AND DESCRIPTION



Stop Trigger Input:  
Normal Voltage = Ground

Stop Trig. Voltage = +5V  
Lemo Connector

External Clock Input:  
Clocks on the Rising  
Edge of a TTL Pulse

Non-inverting (+) input

Differential Lemo  
Connectors

Inverting (-) input

Front Panel Inputs

CAMAC Model 8212  
32-Channel 5 kHz Data Logger

- \* High density-32 channels in one CAMAC module
- \* Independent measurements-operation same as 32 separate ADC's
- \* High sensitivity-12 bits, or 0.025% resolution
- \* Bipolar operation-covers 10 volt range between +5 and -5 volt limits
- \* Differential inputs-eliminate 50-60 cycle and other common mode noise
- \* 50 kHz bandwidth-permits full resolution at maximum sampling speed
- \* Expandable memory-utilizes convenient Model 8800 Series Memory Modules
- \* Simultaneous sampling for ease of data correlation

The LeCroy Model 8212 is a 32-input, 12-bit ADC intended for use with the LeCroy Model 8800 Series 32K Memory Modules in low frequency transient monitoring applications. This combination of units provides 4, 8, 16, or 32 channels of 12-bit fast data logging with memory capacity determined by the number of 8800/12's utilized. With the 8212 used in the 4-channel mode, for instance, one memory module provides 8 K words of storage for each input. Similarly, one 8800/12 provides 1024 words of memory for each channel of an 8212 used in the full 32-input mode.

Simultaneous sampling, available for the first time on the transient recorder market in a 32-channel device, is of prime importance in reducing software overhead and improving real time analysis of the data. Large analog bandwidth makes this feature mandatory.

The Model 8212 is capable of sampling each input from a maximum rate of 40 kHz in the 4-input mode to a maximum rate of 5 kHz in the full 32-input mode. Sampling rate is determined either by a front-panel adjustable internal clock or by an external clock. The external clock can be varied during sample-taking to achieve "importance sampling," a concept which permits savings in memory size while maintaining the ability to focus on specific areas of interest.

SPECIFICATIONS

CAMAC Model 8212

32-CHANNEL 5 kHz DATA LOGGER

Analog Inputs: 4, 8, 16, or 32 differential, voltage-sensing inputs; direct coupled, differential Lemo connectors for cabling flexibility.

Full-Scale Range: Input Voltage Range: Units will normally be delivered with a bipolar  $\pm 5$  volt range. The user, however, may specify a 0 to +10 volt range positive (or 0 to -10 volt range negative).

Common Mode Rejection Ratio: 60 db (DC-60 Hz).

Integral Non-Linearity:  $\pm 1/2$  count.

ADC Resolution: 12 bits ( $\pm 0.012\%$  of full scale  $\pm 1/2$  LSB relative accuracy).

Conversion Time: Approximately the number of Active Channels times 5.5 $\mu$ sec. During conversion, the data is presented to the memory port for transfer to the LeCroy Model 8800 Memory.

Sampling Rate: DC to 40 kHz maximum for 4 active inputs, 20 kHz maximum for 5-8 inputs, 10 kHz maximum for 9-16 inputs, and 5 kHz for 17-32 inputs. The Sampling rate is determined by internal or external clocks.

Internal Clock: Program selectable from .2 kHz to 40 kHz. Stability,  $\pm 0.01\%$ .  
Clocking rates are: 40 kHz (4-channel mode only)  
20 kHz (4,8 channel modes only)  
10 kHz (4,8,16 channel modes only)  
5 kHz (all modes)  
2 kHz (all modes)  
1 kHz (all modes)  
.2 kHz (all modes)

External Clock Input: One, Lemo-type connector; 510 $\Omega$ ; TTL level required, valid frequency range from 0 to 40 kHz (up to 40 kHz if 4 channels are used). The external clock can be varied in frequency to achieve importance sampling. The external clock must be program selected.

The analog signals at the inputs of the 8212 are converted sequentially, each input requiring 5.5  $\mu$ sec dwell time. A complete scan of all 32 inputs takes 176 $\mu$ sec. In the sweep and log mode, the 8212 operates autonomously. The digitized data remains in the 8212 and is updated every 200  $\mu$ sec, available for direct single word per channel readout via normal CAMAC F(0) and F(1) read functions and selected addresses. Each clock signal initiate a full scan of all input channels and subsequent storage of the digitized results in the Model 8800 Memory. A convenient CAMAC function F(2) permits appropriate readout of 8800 Memory contents, correctly formatted one channel at a time.

The LeCroy Model 8212 can be used for logging and storing thermocouple and strain gauge readings on tokamaks, mirror machines, or other fusion devices, biomedical transducers, superconducting magnet currents, or other measurements where a computer-compatible high-resolution measurement of millisecond-type transients with storage in memory can be useful.

Readout Time:

Internal Memory: Before or during any scan, the 8212 may be switched to the "single scan" mode with a CAMAC F(19) which causes the LAM to be generated when conversion is complete. The internal memory may then be read at the maximum CAMAC rate.

External Memory: After the stop trigger and the Post trigger samples, the 8212 automatically enters the data out mode. Seven microseconds after conversion of the final sample, the 8212 issues a LAM. A single channel or "data streaming" must be selected for readout of the external model 8800/12 memory module. If data streaming is selected, the data may be read at the maximum CAMAC rate. If a single channel is selected, the time between (valid Q=1) reads is given by (number of active channels). 0.6 $\mu$ sec. An additional 0.6 microseconds must be added if 32 active channels are selected. If Reads are done too fast, a Q=0 or negative response is generated.

Memory Output Port:

TTL data levels; one 40-conductor cable (Model DC8800) consists of 12 data lines, 12 ground, 7 control lines, and 7 grounds. Output is compatible with LeCroy Model 8800/12 32K Memory Module.

Data:

The proper CAMAC function and addressing scheme gates the 12 binary bits of the selected channel onto the R1 to R12 ( $2^0$  to  $2^{11}$ ) Dataway bus lines. Successive F(2) commands read successive sample values from the selected channel. Output is offset binary with all zeros corresponding to the most negative value and all ones to the most positive value.

CAMAC Commands:

L: A LAM is generated at the end of the next conversion following the F(19) "single scan" command. A LAM is also generated 7 $\mu$ sec following the final conversion after a stop trigger and post trigger scans. A LAM is also generated following the reading of external memory.

Z or C: Resets the 8212 into the "sweep and log" mode.

CAMAC Commands:  
(Continued)

Q: A Q=1 response is generated for valid F(0), F(1), and F(2) reads and also for a test LAM F(8) if the LAM is on. When F(2) readout is used, Q=1 will be generated until the last word from the selected channel is read. The next read will generate a Q=0 response facilitating rapid DMA transfers. The size of the available memory must be programmed into the 8212 by a switch, having been determined by the number of memory modules attached.

X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is applied.

F(0): Read data from inputs 1-16 requires N and A; A(0) through A(15) are used for channel addresses.

F(1): Read data from inputs 1-16 requires N and A; A(0) through A(15) are used for channel addresses.

F(2): Read successive values from each channel onto the Dataway. Requires N and F(16). If channel 33 is selected with F(16), subsequent F(2)·N will read successive memory words (data streaming).

F(3): Reads function data back to computer. Same data written with F(17).

Bit Pattern

| CAMAC | <u>PTSL</u>    |                |                | <u>CLK</u>     |                |                | <u>NOC</u>     |                |
|-------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
|       | 2 <sup>2</sup> | 2 <sup>1</sup> | 2 <sup>0</sup> | 2 <sup>2</sup> | 2 <sup>1</sup> | 2 <sup>0</sup> | 2 <sup>1</sup> | 2 <sup>0</sup> |
| F(17) | W8             | W7             | W6             | W5             | W4             | W3             | W2             | W1             |
| F( 3) | R8             | R7             | R6             | R5             | R4             | R3             | R2             | R1             |

Function representation Data: NOC (Number of Channels)  
CLK (Clock Frequency)  
PTSL (Post Trigger Scans)

F(8): Test LAM.Q response if a LAM is being generated even if the CAMAC L line is disabled.

F(9): Resets 8212 into the "sweep and log" mode just like C & Z except a X=1 response is generated.

F(10): Reset LAM

CAMAC Commands:  
(Continued)

F(11): Re-enable the "sweep and log" mode. Used only after the LAM generated by the F(19) "single scan" command. The data in external memory remains valid unlike the result of C, Z, and F(9) resets.

F(16): Load data from write lines into Channel Select memory.

F(17): Writes function data into module (See F(3)).

F(19): Enables the "single scan" mode causing an LAM at the end of the next scan.

F(0), F(1) reads are then valid.

F(24): Disable the CAMAC L line. LAM's can still be detected using F(8).

F(27): When the external clock is enabled, instead of using an external clock, a single clock pulse can be generated using F(27) and S2.

F(26): Enable LAM.

Packaging:

In conformance with CAMAC standard for nuclear modules (European ESONE Committee Report EUR 4100 or IEEE Standard #583). RF-shielded CAMAC #3 module.

Voltages Used:

|             |             |
|-------------|-------------|
| +6V - 825mA | -6V - 300mA |
| +24V- 300mA | -24V- 225mA |

8212 TECHNICAL INFORMATION

OPERATIONAL DESCRIPTION

a. General

The LeCroy Model 8212 analog to digital converter can simultaneously sample up to 32 voltages at the 32 differential inputs; convert these voltages to 12 bit binary numbers and then store the data in internal memory, and the external LeCroy 8800/12 memory modules. Using just the internal memory, the 8212 can store one sample from each channel.

There is a trade-off between the Number of Samples (NOS) stored, the Number of Channels (NOC) converted and the maximum sampling frequency (CLK). The NOC is CAMAC settable to 4, 8, 16, or 32 active inputs. The maximum sampling frequency is 40, 20, 10, or 5 KHz for 4, 8, 16, or 32 channels respectively. The Number of Samples (NOS) per channel is given by:

$$NOS/CH = (32768/NOC) \cdot NOM$$

where NOM = the number of 8800/12 memory modules (0-3). (Each memory module has a capacity of 32768 words).

b. Front Panel

The front panel contains 32 differential LEMO connectors and 2 single conductor LEMOS; control and data are written and read over CAMAC.

Stop Trigger

The memory modules are organized as a circular shift register. After the memory is filled, further readings are written over initial readings (see Fig. 1).

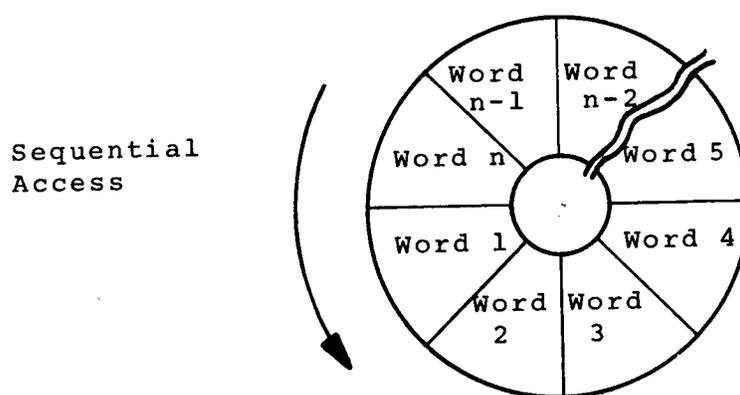


Fig. 1

A stop trigger can be generated by a TTL high level through the front panel STOP TRIG. LEMO connector or by executing a CAMAC F(25). After the stop trigger, the 8212 counts the CAMAC settable number of Post-Trigger Samples (PTS) and then prepares for data readout by executing the LAM mode that has been CAMAC selected. In order to make sure the memory has completely filled up, the following time must be waited after a Reset before giving a Stop Trigger:

$$T_{\text{cycle}} = 32768 \cdot \text{NOM} / (\text{NOC} \cdot \text{CLK})$$

where

|     |   |                               |
|-----|---|-------------------------------|
| CLK | = | sample clock frequency,       |
| NOM | = | number of memory modules, and |
| NOC | = | number of channels.           |

#### External Sample Clock

Each sample clock causes the data to be measured and stored in both internal and external (8800/12) memory. The memory internal to the 8212 stores only one sample (up to 32 words).

A number of CAMAC settable clock frequencies (CLK) 0.2, 1, 2, 5, 10, 20, and 40 kHz are available to control the sampling rate. If these frequencies are insufficient or importance sampling is desired, a TTL CLOCK (Positive edge triggered) may be applied to the EXT. CLOCK LEMO on the front panel with the internal clock set by CAMAC to external. When the external clock is selected, samples can be clocked on F(27) at the first edge of CAMAC strobe S2 provided that the EXT. CLOCK LEMO is not left pulled to TTL high. With importance sampling, the time between samples must always exceed or equal the period of the maximum allowable sampling frequency.

#### Analog Inputs

The front panel contains a differential LEMO input for each of the 32 channels. The + inputs and the - inputs are marked in Section 1. The unipolar model measures the difference between the + and - inputs in the range of 0-10 volts while the bipolar model measures differences in the range of -5 to +5 volts. In both cases the voltage is converted to a number that increases linearly with voltage from 0 for the lowest voltage to 4095 for the highest voltage, i.e., binary conversion in the unipolar model and offset binary conversion in the bipolar model. Thus a one count increase in data represents a voltage increase of 2.442 millivolts. The absolute maximum input voltages are  $\pm 100$  volts. To guarantee the accuracy of the measurements, the inputs must be kept in the range of  $\pm 20V$ .

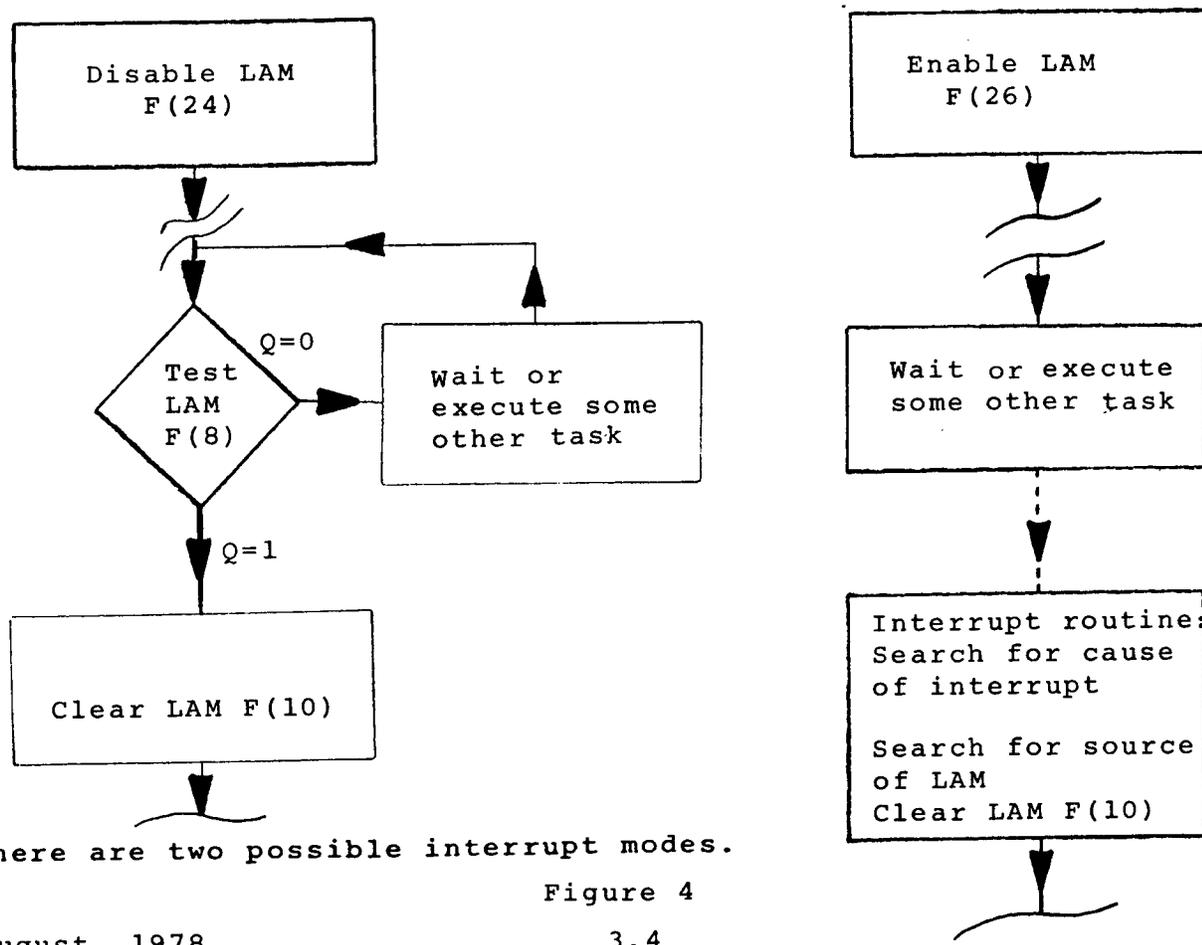


c. CAMAC Control

All CAMAC functions require N and a X=1 response is returned for valid commands. A more complete description of the CAMAC system standard is given later in this manual.

Interrupt-Look At Me (LAM)

The 8212 has two methods of indicating that conversion is complete. The LAM can be enabled, F(26), causing the CAMAC L line to fire when N is deselected for the 8212. If the LAM is disabled, F(24), completed conversion can be detected by a Test LAM F(8) which returns a Q=1 response if the interrupt circuitry has been activated whether or not the LAM is Enabled or Disabled. If the Test LAM returns a Q=1 response with the LAM Disabled, and the LAM is then Enabled, the CAMAC L line will fire. Always clear the LAM after detection. The LAM is cleared by a CLEAR LAM, F(10), or by one of the resets (see Reset section). The LAM Enable/Disable is not affected by a Reset.

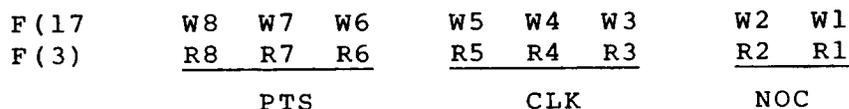


There are two possible interrupt modes.

Figure 4

Set Latch (NOC, CLK, PTS)

The Number of Channels (NOC), Clock Frequency (CLK), and number of Post-Trigger Samples (PTS) are all set by an eight bit word written on the CAMAC write lines with a Set Latch F(17) command. The data written into the latch can be read with the Read Latch F(3) command. The bit patterns are shown in the following diagram.



The binary number representing the NOC is given by 0, 1, 2, 3 for 4, 8, 16, 32 channels respectively. The CLK representation is 0, 1, 2, 3, 4, 5, 6, 7 for External Sample Clock, 0.2, 1, 2, 5, 10, 20, 40 kHz respectively.

If the external clock is selected, not only can samples be clocked using the front panel connector, but also samples can be clocked on the first edge of CAMAC strobe S2 during execution of F(27) only if the front panel EXT. CLOCK connection is not pulled to TTL high voltage by some external source.

The maximum recommended Sample Clock Frequency (CLK) is given by:

$$CLK \leq 160 \text{ kHz} / \text{NOC}.$$

In selecting NOC and CLK it is useful to remember that although the total number of stored readings is constant for a given number of memory modules, the Number of Samples (NOS) stored is dependent on the NOC:

$$NOS = 32768 \cdot \text{NOM} / \text{NOC}$$

where NOM = Number of 8800/12 Memory Modules.

| NOC | W2<br>R2 | W1<br>R1 |
|-----|----------|----------|
| 4   | 0        | 0        |
| 8   | 0        | 1        |
| 16  | 1        | 0        |
| 32  | 1        | 1        |

| SAMPLE<br>CLOCK | W5<br>R5 | W4<br>R4 | W3<br>R3 |
|-----------------|----------|----------|----------|
| External        | 0        | 0        | 0        |
| 0.2 KHz         | 0        | 0        | 1        |
| 1 KHz           | 0        | 1        | 0        |
| 2 KHz           | 0        | 1        | 1        |
| 5 KHz           | 1        | 0        | 0        |
| 10 KHz          | 1        | 0        | 0        |
| 20 KHz          | 1        | 1        | 0        |
| 40 KHz          | 1        | 1        | 1        |

NOTE: CAMAC lines are inverted so that a "1" is represented by zero volts.

Bit settings for NOC, and CLK are summarized in these tables. These bit values are written/read with Write/Read Latch F(17)/F(3) commands. These commands also control the Post-Trigger samples (PTS).

PTS is dependent on the Number of Memory modules (NOM) switches which are located in a small package on the digital board at position 2I and are accessible through a cutout on the side panel. The NOM switch must be set to the correct position or the data will become confused when read out. The PTS are counted by a pre-settable 16 bit counter that disables the sampling and switches to the readout mode when it counts to a number equal to  $32768 \cdot \text{NOM} / 2$ . The PTS counter begins counting on a Stop Trigger. Thus the PTS is dependent on the number the PTS counter is pre-set to which is designated PTSC:

$$\text{PTS} = (32768 \cdot \text{NOM} / 2) - \text{PTSC}.$$

The PTS must be set to 1 or greater or the 8212 will switch to the readout mode without a Stop Trigger. Thus the PTS is settable over a range from 1 (virtually all pre-trigger samples) to  $32768 \cdot \text{NOM} / 2$ . Although the PTS counter is 16 bits, it is settable by only the three bits W8, W7, and W6, which are called PTSL when output from the latch. These three latch bits must be connected to the 16 PTS bits on a jumper plug that plugs into a jumper socket on the digital board at position 1H and is accessible through a cutout in the side panel. The pin numbers of the jumper socket increase in a counterclockwise direction and pin 1 is located in the upper left hand corner. The identification of the pins is given on the following charts:

|                         |       |       |       |
|-------------------------|-------|-------|-------|
| PTSL (outputs) bits     | $2^2$ | $2^1$ | $2^0$ |
| Jumper socket (1H) pin# | 3     | 2     | 1     |

|                    |          |          |          |          |          |          |       |       |       |               |                   |
|--------------------|----------|----------|----------|----------|----------|----------|-------|-------|-------|---------------|-------------------|
| PTSC (inputs) bits | $2^{15}$ | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6 2^5 2^4$ | $2^3 2^2 2^1 2^0$ |
| Jumper (1H) pin #  | 6        | 11       | 12       | 13       | 14       | 15       | 16    | 8     | 10    | all to 5      | all to 7          |

Pin 9 is ground (a source of binary 0).

Pin 4 is +5 volts (a source of binary 1).

The PTSL pins are low impedance output voltages and should not be connected together or to +5 volts or ground. The PTSC pins are inputs and may be connected together and connected to an output voltage.

Judicious selection of the jumpers is necessary to optimize the versatility of the 8212 for a particular application. For all Post Trigger Samples, the PTS must be set equal to the Number of Samples (NOS),

$$PTS = NOS.$$

Substituting in the previous two equations gives

$$(32768 \cdot NOM/2) - PTSC = 32768 \cdot NOM/NOC$$

which becomes

$$PTSC = 32768 \cdot NOM \cdot (1/2 - 1/NOC).$$

For all Pre-Trigger Samples set  $PTS=1$  so that:

$$PTSC = (32768 \cdot NOM/2) + 1.$$

Note that for all Pre-Trigger Samples, the PTSC setting depends only on the NOM, while for all Post-Trigger Samples, the PTSC is also dependent on the NOC. Various header connections are listed in Appendix A.

Example: The 8212 is to be used with 1 8800/12 memory module, and it is desired to have all pre-trigger and all post-trigger samples for each NOC setting. Substituting into the equation for all Pre-Trigger Samples, we find that:

$$PTSC = 16383 = 0011, 1111, 1111, 1111_2.$$

Substituting into the equation for all Post-Trigger Samples gives:

PTSC= 8192=0010, 0000, 0000, 0000<sub>2</sub> for 4 channels,  
 PTSC=12288=0011, 0000, 0000, 0000<sub>2</sub> for 8 channels,  
 PTSC=14336=0011, 1000, 0000, 0000<sub>2</sub> for 16 channels, and  
 PTSC=15360=0011, 1100, 0000, 0000<sub>2</sub> for 32 channels

It is impossible to achieve all 5 of these PTSC options with the three PTSC bits available. However, a nice compromise can be achieved by making the following connections:

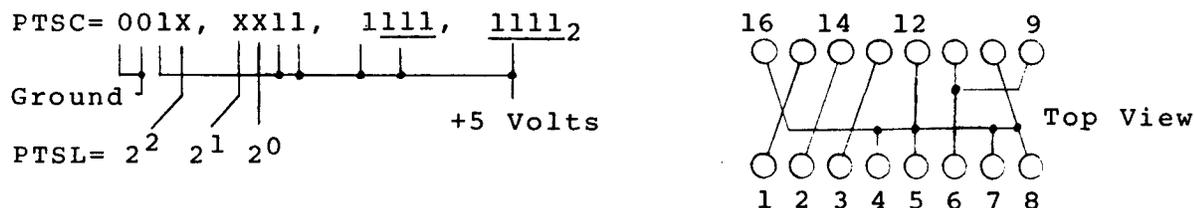


Figure 5

The jumper plug is wired with pins 6 and 11 connected to pin 9, pins 12, 16, 8, 10, 5 and 7 connected to pin 4, pin 13 connected to pin 3, pin 14 connected to pin 2, and pin 15 connected to pin 1. Of course, since only one memory module is used, switch 1 of the NOM switch is turned on while switches 2, 3 and 4 are turned off.

In order for the PTS to decrease monotonically as the PTSL increases, each PTSL bit must be connected to a PTSC bit that is higher than every PTSC bit that is connected to a less significant PTSL bit. In order that the PTS change in equal increments, the sum of the PTSC bits connected to PTSL bit must be twice the similar sum for the next less significant PTSL bit. In order that no two PTSL counts result in almost equal PTS's, it is recommended that each PTSL bit should be connected to a sum of PTSC bits whose total value is greater than or equal to the total PTSC value connected to the next less significant bit.

Reset (initialization) C, Z, or F(9)

The C, Z, or F(9) commands are completely equivalent except that C and Z do not return a X=1 response since they are not CAMAC functions. The reset removes the 8212 from the readout mode and also performs an implicit F(11) (see Continuously Sample) causing the system to continuously sample and store. A reset clears the LAM although it does not affect the Enable/Disable LAM interrupt modes. The reset does not change the contents of the NOC, CLK, PTS latch. A reset is the only way to enable the sample clock after the Post-Trigger Samples (PTS) have been counted out following a Stop Trigger. The data is invalidated by a Reset.

### Single Sample F(19)

The Single Scan F(19) function causes the sample clock to be disabled at the end of the next scan and then causes an interrupt (LAM). The interrupt will occur approximately 5.5 ·NOC microseconds after the sample clock.

The sample clock can be re-enabled for just one sample by a Single Sample F(19) command or for many samples by Continuously Sample F(11) or Reset commands. Of course a Reset will invalidate previous data. However, F(19) and F(27) will not always enable the sample clock since after a Stop Trigger and PTS samples, only a Reset will enable the clock. Use of F(19) after a Stop Trigger should be avoided since it may be impossible to determine which command caused the ensuing interrupt.

### Continuously Sample F(11)

A F(11) will cause the 8212 to keep the sample clock enabled until a Single Sample F(19) command, a Reset or Stop Trigger and PTS samples. After a Stop Trigger and PTS samples, only a Reset will enable the sample clock. A Reset also does everything done by a Continuously Sample command F(11). The F(11) command also resets the channel counter, a necessary step if further samples are to be taken after reading internal memory.

### CAMAC Sample Clock F(27)

With the CLK Latch set to external and the front panel EXT. CLOCK disconnected, a sample can be clocked on the first edge of CAMAC signal S2 during a F(27) CAMAC cycle. If the EXT CLOCK LEMO is held at TTL high, the CAMAC clock is disabled.

### Read Internal Memory F(0), F(1)

Following the interrupt caused by a Single Sample F(19) Command, the internal memory may be read at the maximum CAMAC speed. If the commands have been executed in proper order, a Q response will be returned during Internal Memory Reads F(0), F(1) indicating that the data read is valid. Channels 1 through 16 are read by F(0) with the CAMAC subaddress set to one less than the channel (CH) to be read. Channels 17 through 32 are read by F(1) with the CAMAC subaddress set to 17 less than the channel (CH) to be read. Thus to read channel CH, execute the CAMAC function also given by:

$$F(\text{INT}(\text{CH}/17)) \cdot A((\text{CH}-1) - \text{INT}(\text{CH}/17))$$

READING INTERNAL MEMORY

| <u>Channel</u> | <u>Command</u> | <u>Channel</u> | <u>Command</u> |
|----------------|----------------|----------------|----------------|
| 1              | F(0)·A(0)      | 17             | F(1)·A(0)      |
| 2              | F(0)·A(1)      | 18             | F(1)·A(1)      |
| 3              | F(0)·A(2)      | 19             | F(1)·A(2)      |
| 4              | F(0)·A(3)      | 20             | F(1)·A(3)      |
| 5              | F(0)·A(4)      | 21             | F(1)·A(4)      |
| 6              | F(0)·A(5)      | 22             | F(1)·A(5)      |
| 7              | F(0)·A(6)      | 23             | F(1)·A(6)      |
| 8              | F(0)·A(7)      | 24             | F(1)·A(7)      |
| 9              | F(0)·A(8)      | 25             | F(1)·A(8)      |
| 10             | F(0)·A(9)      | 26             | F(1)·A(9)      |
| 11             | F(0)·A(10)     | 27             | F(1)·A(10)     |
| 12             | F(0)·A(11)     | 28             | F(1)·A(11)     |
| 13             | F(0)·A(12)     | 29             | F(1)·A(12)     |
| 14             | F(0)·A(13)     | 30             | F(1)·A(13)     |
| 15             | F(0)·A(14)     | 31             | F(1)·A(14)     |
| 16             | F(0)·A(15)     | 32             | F(1)·A(15)     |

August, 1978

3.10

where  $INT(X)$  = the greatest integer less than or equal to  $X$ . For example to read channel 22 execute  $F(1) \cdot A(5)$ . The channels may be read any number of times in any order except that if further samples are to be taken, the internal channel counter must be reset by reading the lowest channel  $F(0) \cdot A(0)$ , executing a continuously Sample  $F(11)$  command, or executing a Reset.

Stop Trigger F(25)

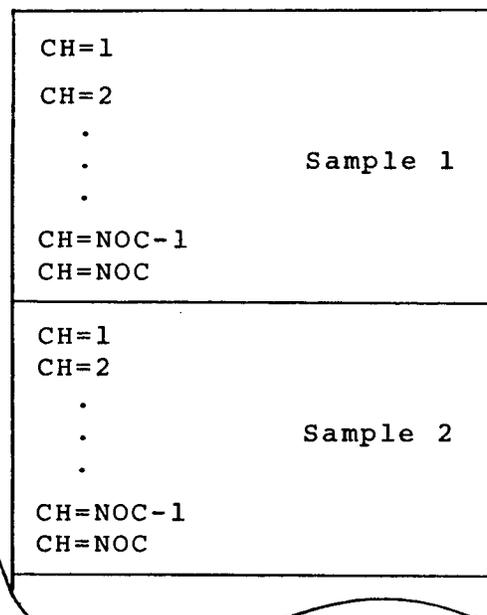
A Stop Trigger is caused by CAMAC strobe S2 during execution of a Stop Trigger F(25) command. This command is identical to, but independent of the front panel STOP TRIG. (See Front Panel Section). An interrupt is generated PTS samples (see Latch Section) after the Stop Trigger to indicate that the 8212 is ready for a Channel Select F(16) command in preparation for reading out the external 8800/12 memory modules. The interrupt occurs approximately  $5.5 \cdot NOC + 7$  microseconds after the final Post Trigger Sample. At least one Sample Clock must be executed before a Stop Trigger. Use of the Single Sample F(19) command after a Stop Trigger should be avoided since it may be impossible to determine which command caused the ensuing interrupt.

Channel Select F(16)

Channel Select F(16) is used before reading external memory. A Channel Select should be executed only once after the interrupt following a Stop Trigger or a previous scan of external memory. The external memory is loaded with NOC number of words each sample clock.

CH = Channel Number  
NOC = Number of Channels

Direction of  
Memory Access



External Memory Organization  
Figure 6

The memory can be read two ways; the data from only one channel can be read or the entire memory can be read sequentially. Reading the entire memory is faster (see the following Read External Memory F(2) Section) but the data from each channel is read sequentially before the next chronological sample is read. To select a single channel and have the data read in chronological order, simply execute a Channel Select F(16) command with one less than the channel number to be read loaded onto the CAMAC write bus. To prepare for the sequential readout of every word in external memory (data streaming), execute a Channel Select F(16) command with the write bus set at any number between 32 and 63 inclusive. Adding any multiple of 64 to the setting of the CAMAC write bus for a Channel Select F(16) instruction will cause no change.

#### Read External Memory F(2)

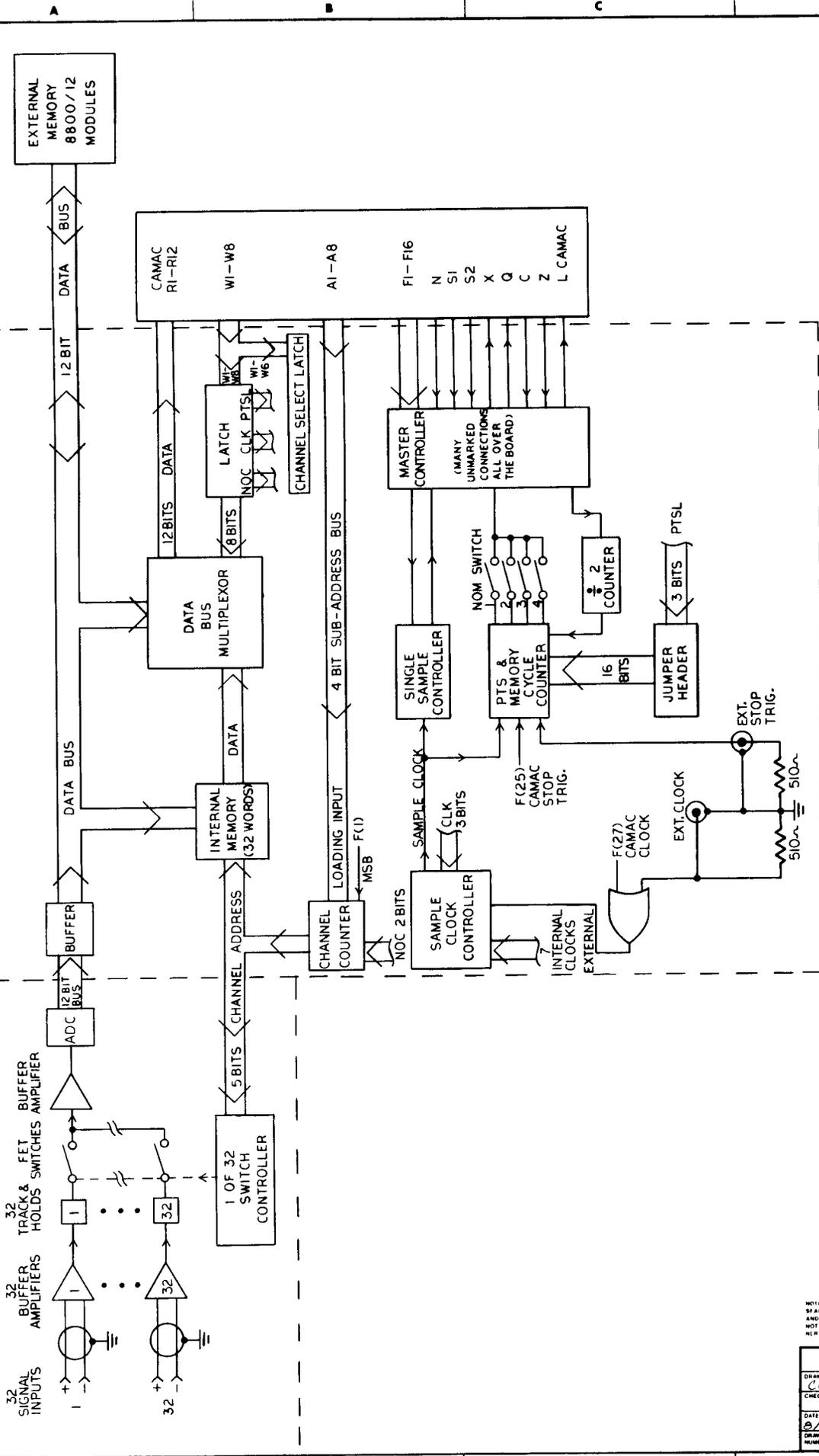
After the Channel Select, the external memory 8800/12 module(s) may be read by executing F(2)s. The 12 bits of data will be returned on the CAMAC read bus (R1-R12). Reading the data invalidates the data until it is updated. Executing F(2) before the data is updated will result in no Q response (Q=0), indicating that the data is invalid because it has not yet been updated. When the data is valid, a Q response will be returned. If every word of external memory is to be sequentially read, the data can be read at the maximum CAMAC rate with valid data (Q=1) returned on every F(2) read. If however a single channel is selected, approximately  $0.6 \cdot \text{NOC} \mu\text{s}$  ( $+0.6 \mu\text{s}$  for  $\text{NOC}=32$ ) will elapse between valid reads.

After the memory is scanned, the 8212 generates an interrupt which must be followed by a Channel Select F(16) or a Reset. The time between the Channel Select and the first valid read, and the time between the final valid read and the interrupt, depend on the channel selected and are between  $0.6 \mu\text{s}$  and the time between valid reads. The times given above vary by several microseconds from cycle to cycle.

The number of valid reads included in a memory scan is equal to the Number of Samples (NOS) when a single channel is selected and is equal to the number of words of memory ( $=32768 \cdot \text{NOM}$ ) when every word of memory is read sequentially. Do not execute a Channel Select until the data previously selected has been read. After the data has been read, further reads will have no Q response. During all reads, the most significant bit of the data is read on R12 and the least significant bit is read on R1.

CONTROLLER BD

ANALOG BD



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| DRAWN                   | CWP        | 8212 SIMPLIFIED BLOCK DIAGRAM |                |
| CHECKED                 |            |                               |                |
| DATE                    | 2/18/78    |                               |                |
| DRAWING NUMBER          | 8212-90010 | SHEET 1 OF 1                  | ECO NO. / DATE |

#### 4. FUNCTIONAL DESCRIPTION

##### 4a. General

The Model 8212 data logger is a 32 channel waveform digitizer. The 8212 is built on two boards, the analog board and the digital control board. The analog board contains 32 buffer amplifiers, 32 track and hold circuits, 32 FET switches, 1 of 32 channel decoding circuitry, and a successive approximation analog to digital converter (ADC). The controller board includes a CAMAC interface, data buses, internal memory, and logic circuitry for controlling the analog bd., the CAMAC interface, and external Model 8800/12 memory modules. These boards are described separately and in detail in the following sections. Refer to the preceding block diagram while reading the following sections. To simplify the block diagram, control wires are left out.

##### 4b. ADC Board

1. Buffer Amplifiers: A balanced shielded cable connects each front panel differential LEMO to one of 32 buffer amplifiers which convert the signal from differential to single ended so that only this first stage need adjustment for common mode rejection. The buffer amplifiers also provide  $1M\Omega$  input impedance.

2. Track and Hold Circuits: The output of each buffer amplifier is connected to a track and hold circuit. The track and hold control signals are connected together so that the outputs simultaneously track the all input voltages or simultaneously store in the hold capacitors the input voltages applied at the instant the track/hold control signal was set to hold.

3. FET Switches and Address Bus Decoder: Each voltage stored in a hold capacitor is sequentially switched to the ADC by FET switches. At a given moment only one track and hold output is connected to the ADC by a 1 of 32 FET switch controller which decodes a 5 bit channel address and determines which channel is to be connected.

4. Buffer Amplifier: Following the FET switches is a high input impedance buffer amplifier which reduces the effect of the FET switches output impedance to a negligible level.

5. Analog to Digital Converter (ADC): The output of the buffer amplifier is connected to a 12 bit hybrid successive approximation ADC which converts the voltage to a 12 bit digital representation. The ADC accepts a convert pulse on the "convert" bus

and returns a pulse on the "dardy" bus when the data is ready.

6. Operation Sequence: When a sample is taken, the track and hold circuits are first set from track to hold. The control and channel decode logic then connects the output of the first track and hold to the high impedance buffer via the FET switches. After a short wait to allow transients to settle, the control logic issues a convert command to the ADC. When the ADC has finished its conversion, it issues a signal on the dardy line. The controller stores the ADC output in memory, switches the output of the next track and hold to the buffer, and the cycle repeats until the last channel voltage is converted and stored. The control logic then sets the track and hold circuits to the track mode and the sample is complete.

#### 4c. Controller Board

1. Master Controller: The master controller co-ordinates timing, sequencing, and synchronization of virtually every section of the 8212. Most of the connections to the master controller are not shown on the simplified block diagram. The master controller decodes the CAMAC commands and co-ordinates the CAMAC timing with the possibly asynchronous task specified by the CAMAC command, asynchronous external memory refresh, reads, and writes, asynchronous Sample Clocks, and the Stop Trigger.

2. Single Sample Controller: When sampling is enabled by the master controller, the single sample controller operates the sequencing of the analog board as explained in part b. of this chapter. The single sample controller starts sequencing on a Sample Clock pulse and returns a signal to the master controller at the end of the sample.

3. Data Bus Multiplexing, Latch, Channel Select Latch: During sampling, the data flows from the ADC through a 12 bit buffer on the controller bd. and is simultaneously stored in both internal memory and external memory. The next sample is overwritten onto internal memory and stored in the next sequential locations of external memory. In the data bus multiplexor, a series of latches and buffers allow this data bus, the output bus of internal memory, or the output bus of the NOC, CLK, PTSL Latch, to be connected to the CAMAC read lines. In all reads, CAMAC bit R1 is the least significant bit. CAMAC write lines W1-W8 are connected to the NOC, CLK, PTSL Latch while only W1-W6 are used for the Channel Select Latch.

4. Sample Clock Controller: The sample clock controller decodes the 3 CLK bits from the Latch and selects 1 of 7 internal clocks or the external clock. As can be seen in the simplified block diagram, the CAMAC clock and the Ext. Clock front panel connector are connected through an inclusive OR gate to the external input of the sample clock controller. Thus if the Ext. Clock LEMO is connected to TTL high (logical true), the output of the OR gate will remain high regardless of the condition of the CAMAC clock function.

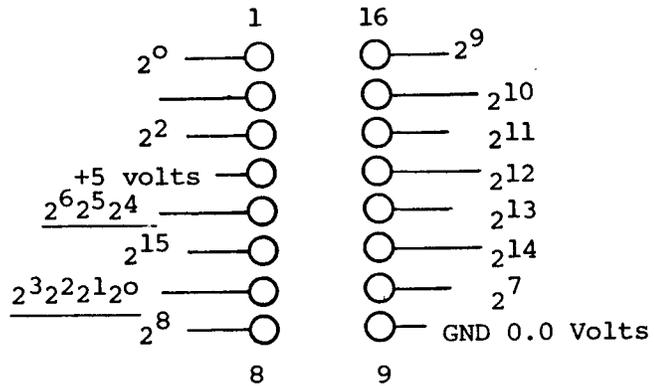
5. PTS and Memory Cycle Counter: The same counter is used to count the Post Trigger Samples and to keep track of the external memory address during external memory reads. Since the memory is cyclic, the absolute location of the data is ignored during conversion and storage, but it is necessary to indicate the end of a complete read of external memory. The NOM switches are numbered 1 through 4, and the switch corresponding to the NOM should be switched on while the other switches should be switched off, otherwise an improper number of reads will result and the data will be confused. The NOM switch setting also affects the PTS count. The counter only counts up to  $32768 \cdot \text{NOM} / 2$  which is  $1/2$  the total memory size; the External Memory reads are first connected to a  $\div 2$  counter so that the total number of reads counted is  $32768 \cdot \text{NOM}$ . The 3 PTSL bits from the latch are connected via the jumper header to the 16 bit loading input of the PTS counter. The counter is loaded with the data at the loading inputs at the end of every sample that occurs before the Stop Trigger. If a Stop Trigger is executed before a sample is taken, the PTS counter will not be loaded with the information from the jumper header.

6. Channel Counter and Internal Memory: During sampling, the 5 bit channel counter provides the channel address used by the FET switch controller on the analog board. This same channel address is used by the internal memory. During F(0)/F(1) reads, the channel counter is loaded from the 4 bit CAMAC subaddress bus and the decoded F(1) signal which is connected to the MSB of the 5 bit channel counter. If further samples are to be taken after reading internal memory, the channel counter must be reset by executing a RESET, F(11), or reading the lowest channel F(0)·A(0). The CAMAC function F(19) can be executed in the middle of a sample and does not reset the channel counter.

7. External Memory: The operation of the external memories is explained in Technical Information Manual Model 8800 Memory Module. However for convenience, Appendix B contains a chart showing the connections of the cable that runs from the 8212 controller board to the external memory modules.

APPENDIX A

Header connections for setting  
the PTS in equal increments.



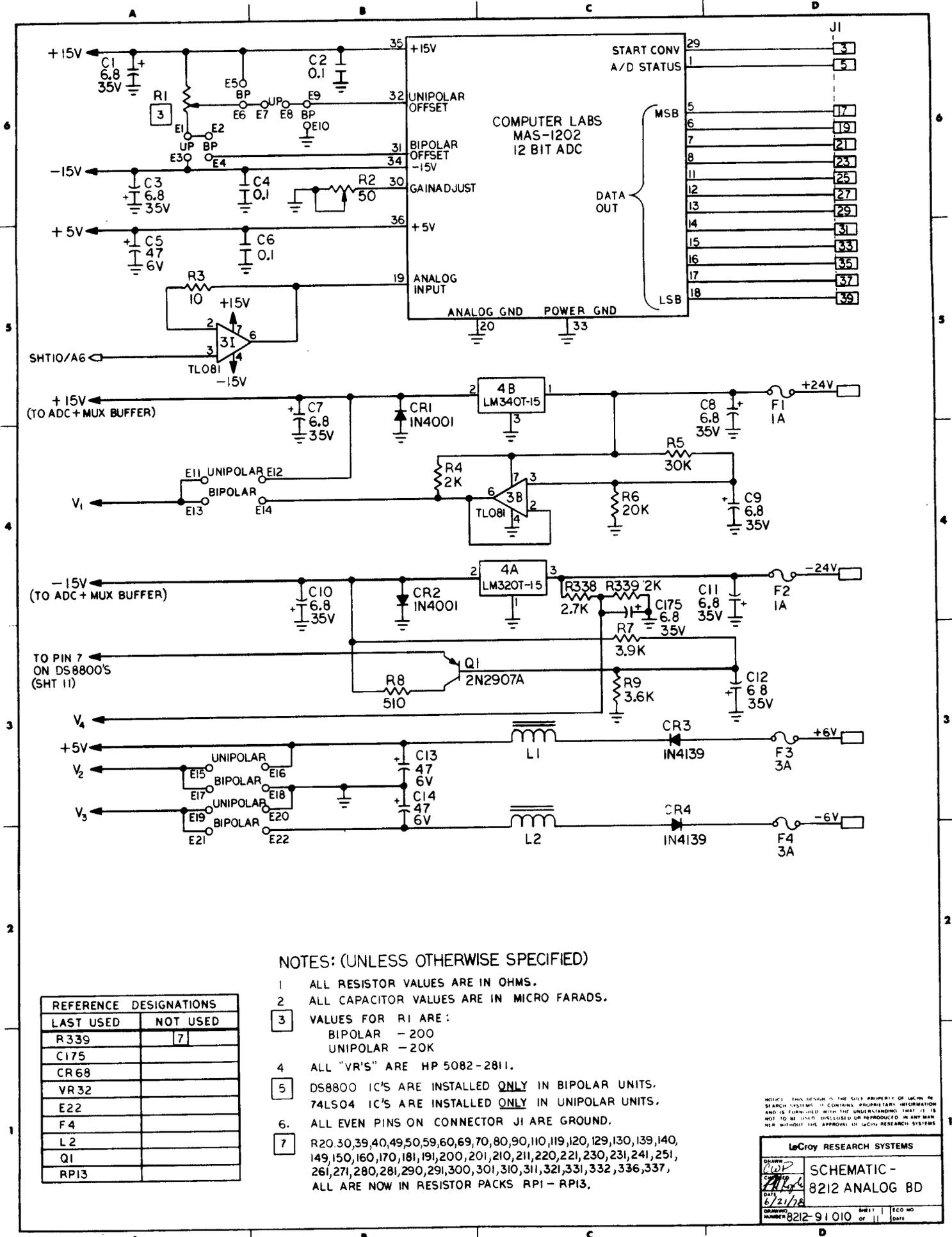
| PTSL | PTS  | NOM=1 | NOM=2                | PTSL | PTS  | NOM=1 | NOM=2 |
|------|------|-------|----------------------|------|------|-------|-------|
| 0    | 1024 |       | <p>TOP<br/>VIEWS</p> | 0    | 2048 |       |       |
| 1    | 896  |       |                      | 1    | 1792 |       |       |
| 2    | 768  |       |                      | 2    | 1536 |       |       |
| 3    | 640  |       |                      | 3    | 1280 |       |       |
| 4    | 512  |       |                      | 4    | 1024 |       |       |
| 5    | 384  |       |                      | 5    | 768  |       |       |
| 6    | 256  |       |                      | 6    | 512  |       |       |
| 7    | 128  |       |                      | 7    | 256  |       |       |
| 0    | 4096 |       |                      | 0    | 8192 |       |       |
| 1    | 3584 |       |                      | 1    | 7040 |       |       |
| 2    | 3072 |       |                      | 2    | 5888 |       |       |
| 3    | 2560 |       |                      | 3    | 4736 |       |       |
| 4    | 2048 |       |                      | 4    | 3584 |       |       |
| 5    | 1536 |       |                      | 5    | 2432 |       |       |
| 6    | 1024 |       |                      | 6    | 1280 |       |       |
| 7    | 512  |       |                      | 7    | 128  |       |       |

NOM = (Number of Memories)  
 PTS = (Post Trigger Sample)  
 PTSL = (Post Trigger Scans)

Appendix C

LIST OF ABBREVIATIONS

- CH = The channel number as written on the front panel of the 8212.
- CLK = The sample clock frequency in Hertz.
- NOC = The number of active channels (CAMAC settable to 4, 8, 16, or 32).
- NOM = The number of 8800/12 memory modules used.
- NOS = The number of samples (each sample includes NOC measurements).
- PTS = The number of post-trigger samples.
- PTSC = The 16 bit binary number loaded into the post-trigger sample counters preset inputs.
- PTSL = A 3 bit number output by the latch used to control the PTSC via a strap option.



NOTES: (UNLESS OTHERWISE SPECIFIED)

- 1 ALL RESISTOR VALUES ARE IN OHMS.
- 2 ALL CAPACITOR VALUES ARE IN MICRO FARADS.
- 3 VALUES FOR R1 ARE:  
 BIPOLAR - 200  
 UNIPOLAR - 20K
- 4 ALL "VR'S" ARE HP 5082-2811.
- 5 DS8800 IC'S ARE INSTALLED ONLY IN BIPOLAR UNITS.  
 74LS04 IC'S ARE INSTALLED ONLY IN UNIPOLAR UNITS.
- 6. ALL EVEN PINS ON CONNECTOR J1 ARE GROUND.
- 7 R20,30,39,40,49,50,59,60,69,70,80,90,110,119,120,129,130,139,140,  
 149,150,160,170,181,191,200,201,210,211,220,221,230,231,241,251,  
 261,271,280,281,290,291,300,301,310,311,321,331,332,336,337,  
 ALL ARE NOW IN RESISTOR PACKS RPI1 - RPI3.

| REFERENCE DESIGNATIONS |          |
|------------------------|----------|
| LAST USED              | NOT USED |
| R 339                  | 7        |
| C175                   |          |
| CR 68                  |          |
| VR 32                  |          |
| E22                    |          |
| F4                     |          |
| L2                     |          |
| Q1                     |          |
| RPI3                   |          |

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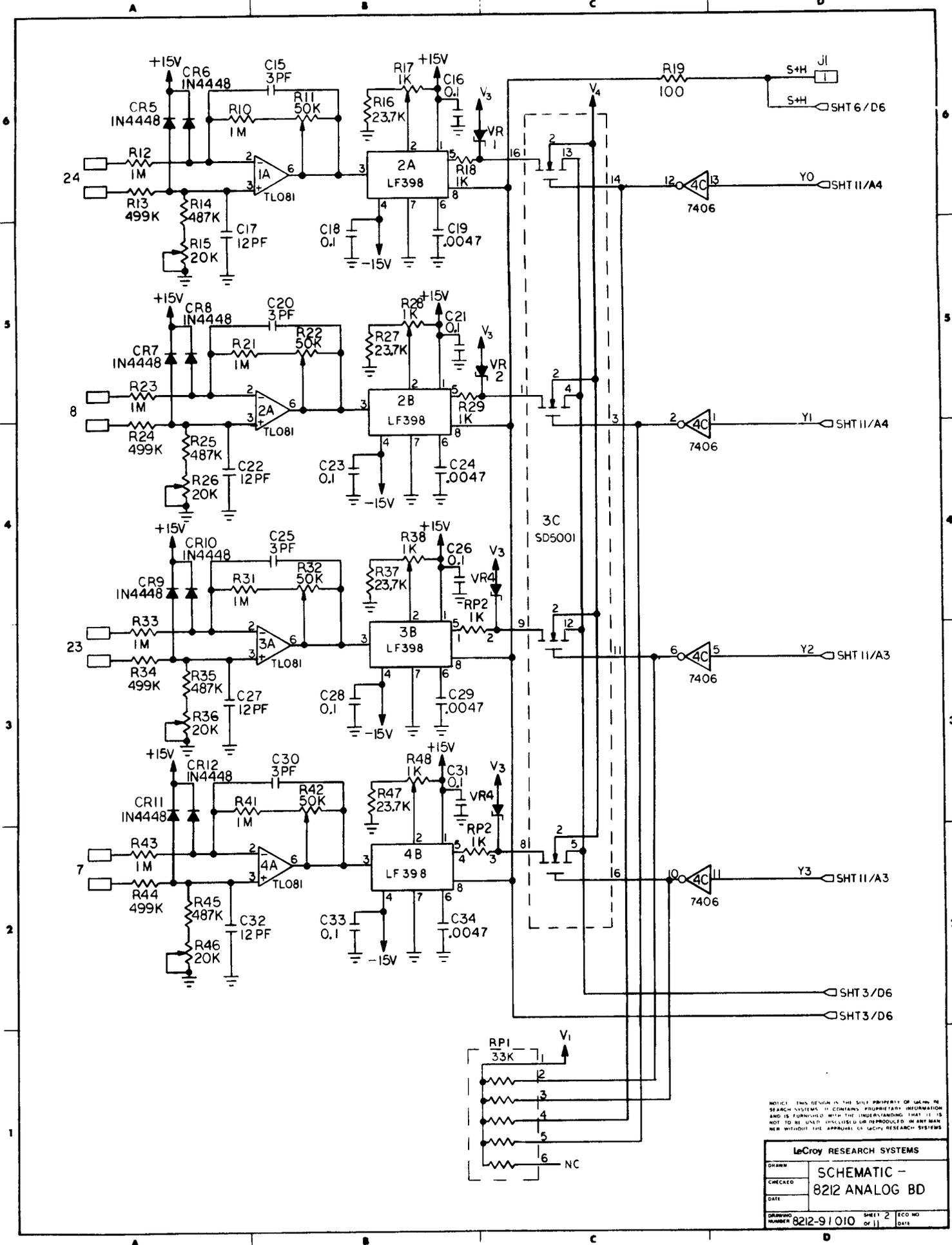
LOCKHEED RESEARCH SYSTEMS

SCHEMATIC - 8212 ANALOG BD

DATE: 6/21/78

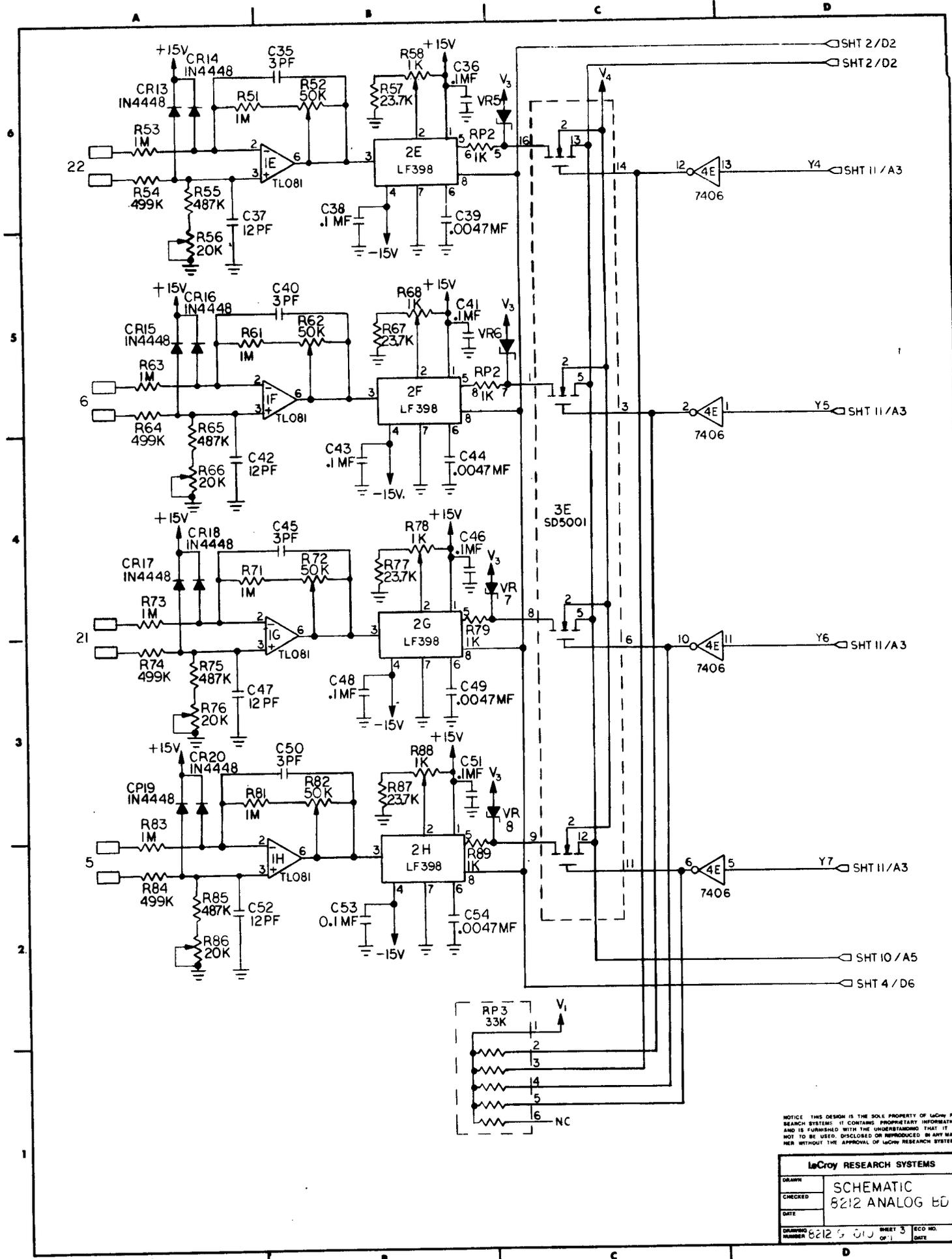
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DRWING NO: 8212-91 010 SHEET 11 OF 11 DATE



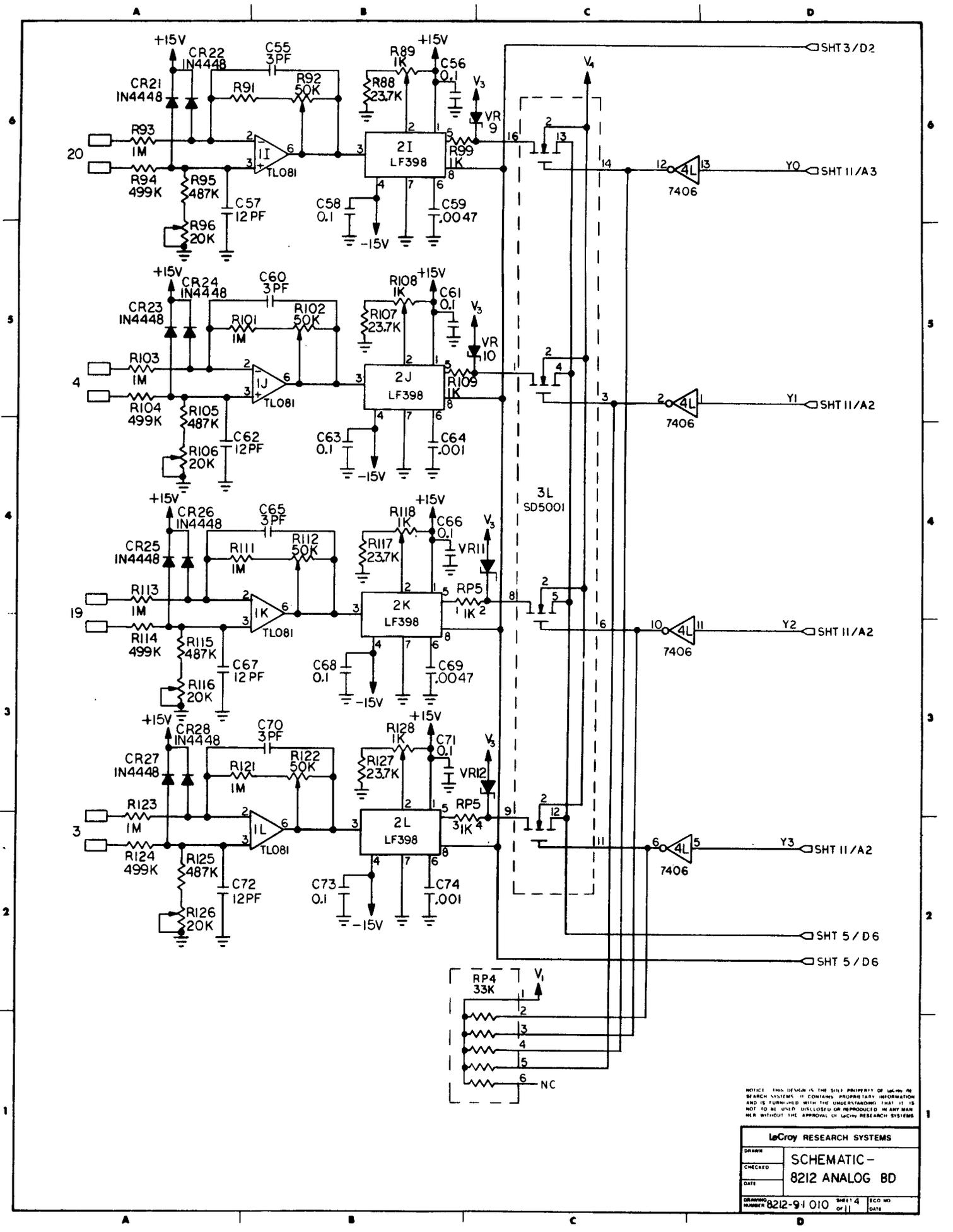
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| DATE                           |              |
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| ECO NO                         | DATE         |



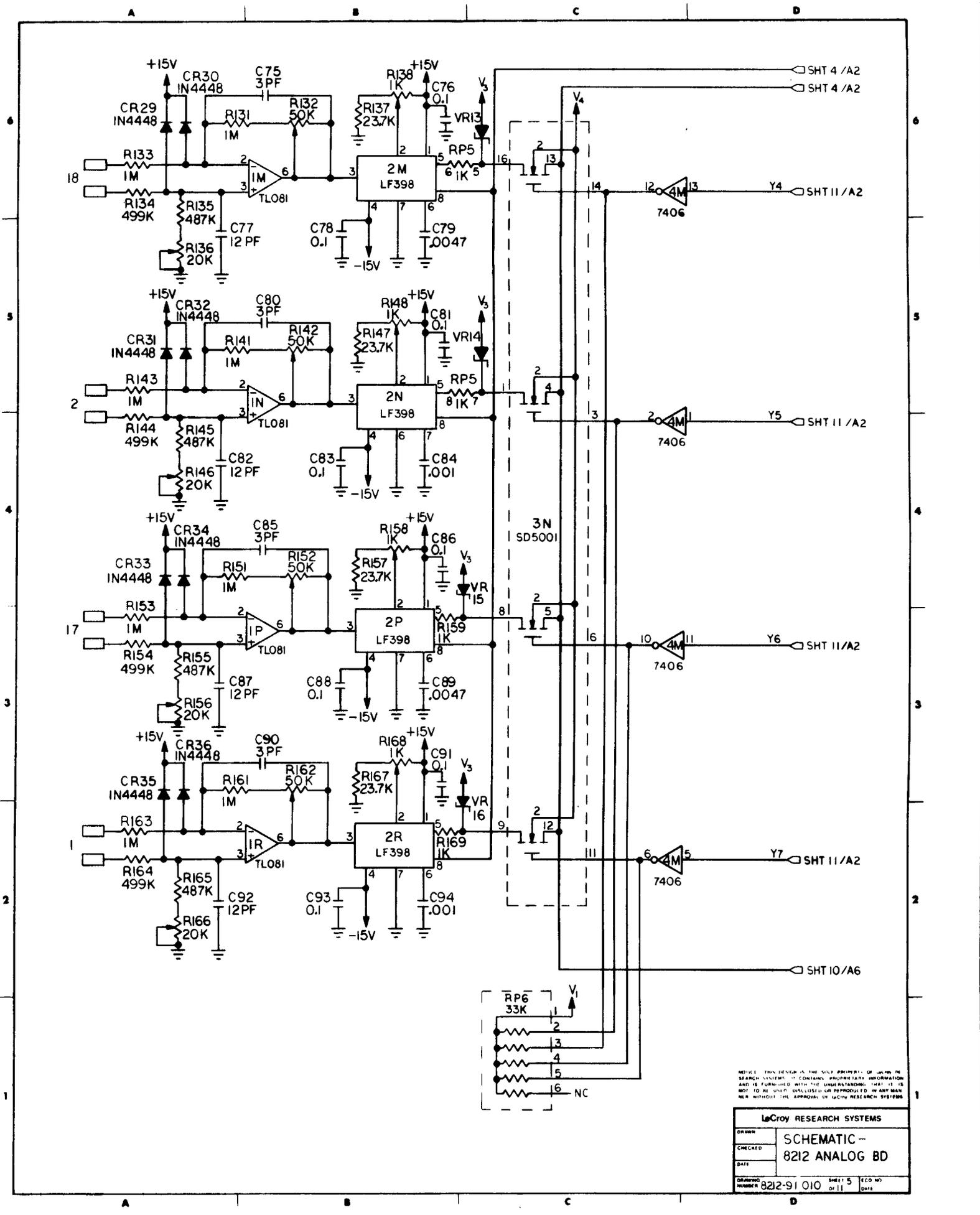
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| ECO NO.                        | DATE           |



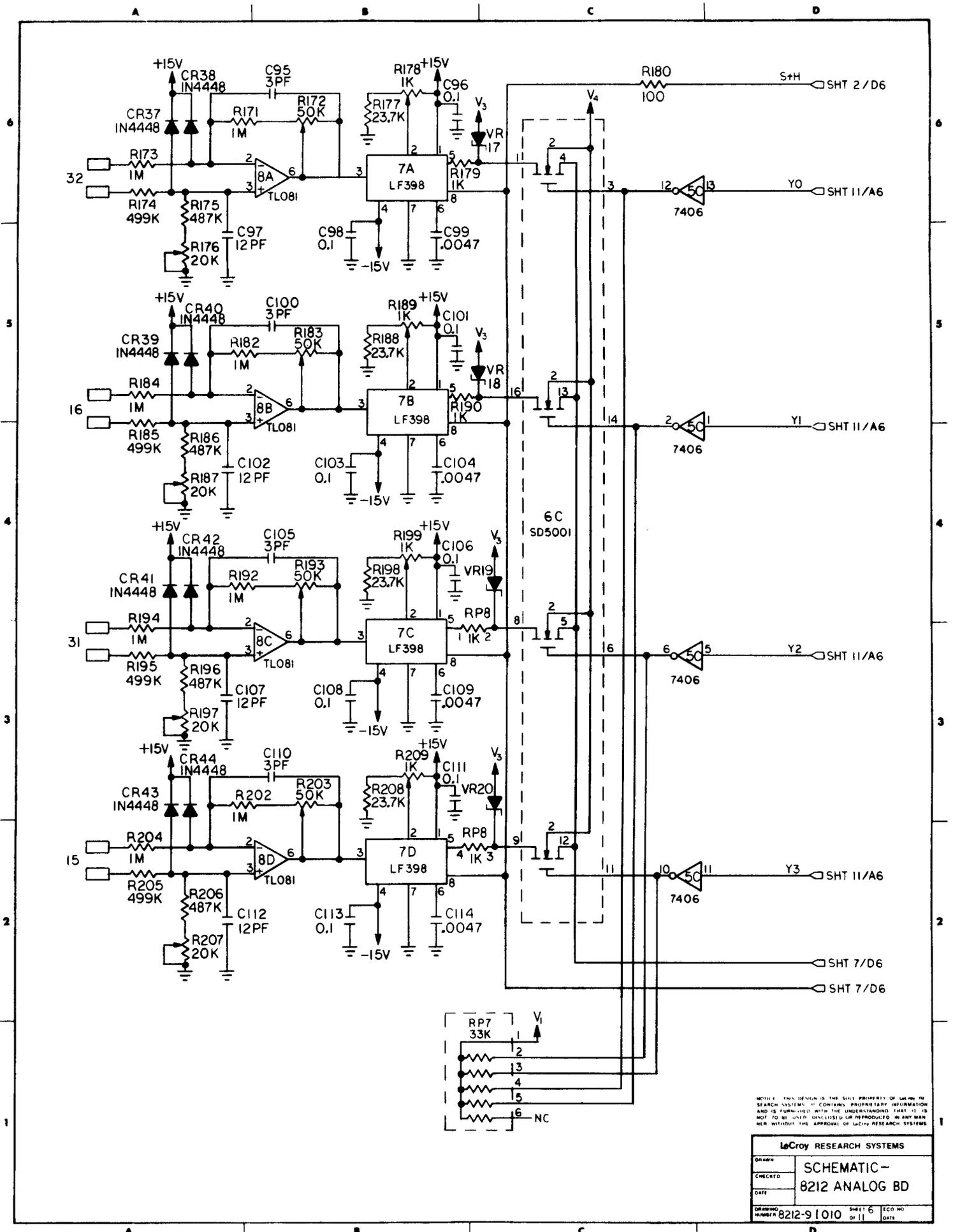
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| OF 11                          | DATE                          |



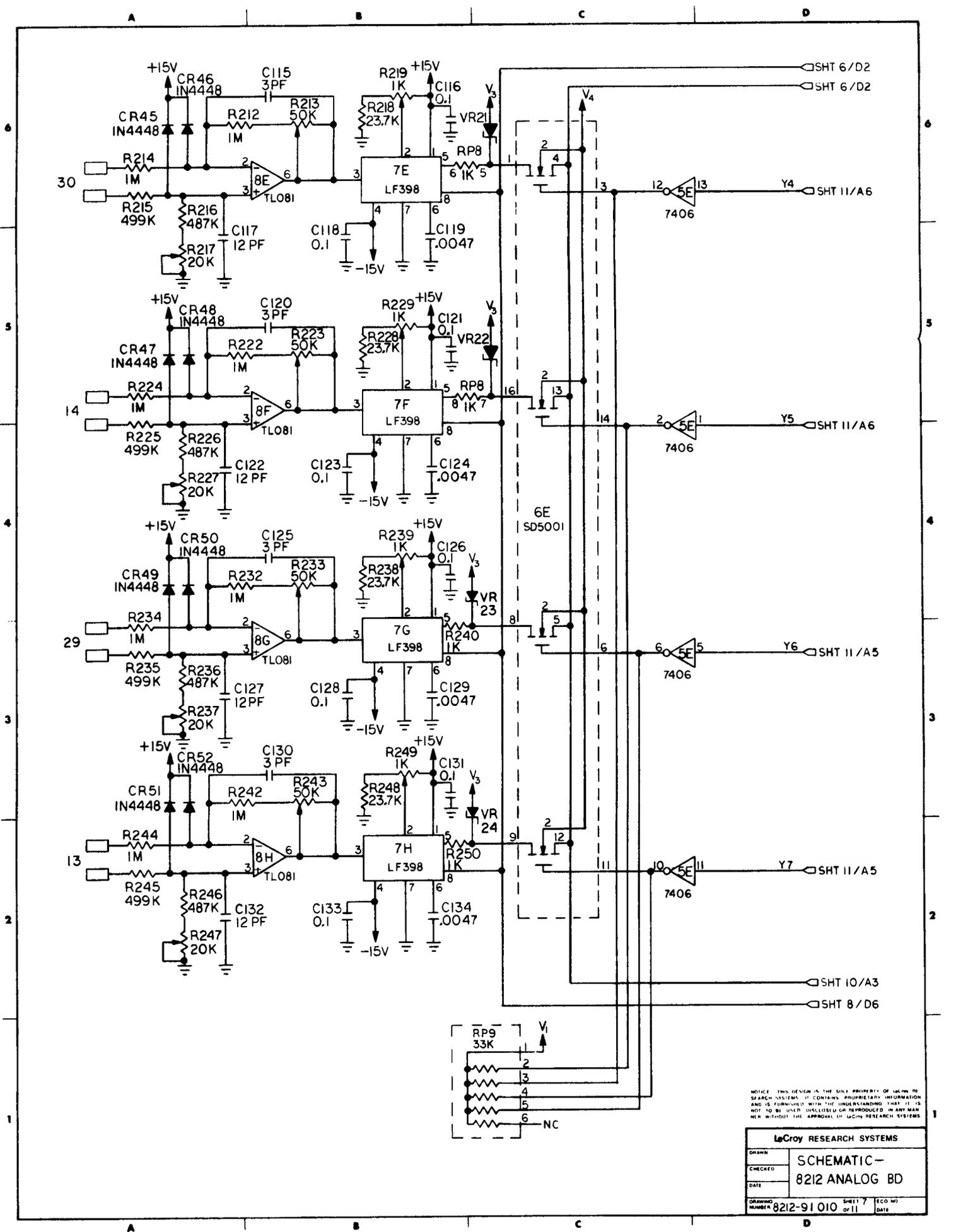
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| DRAWING NUMBER 8212-91 010    | SHEET 5 OF 11  |
|                               | ECO NO. DATE   |



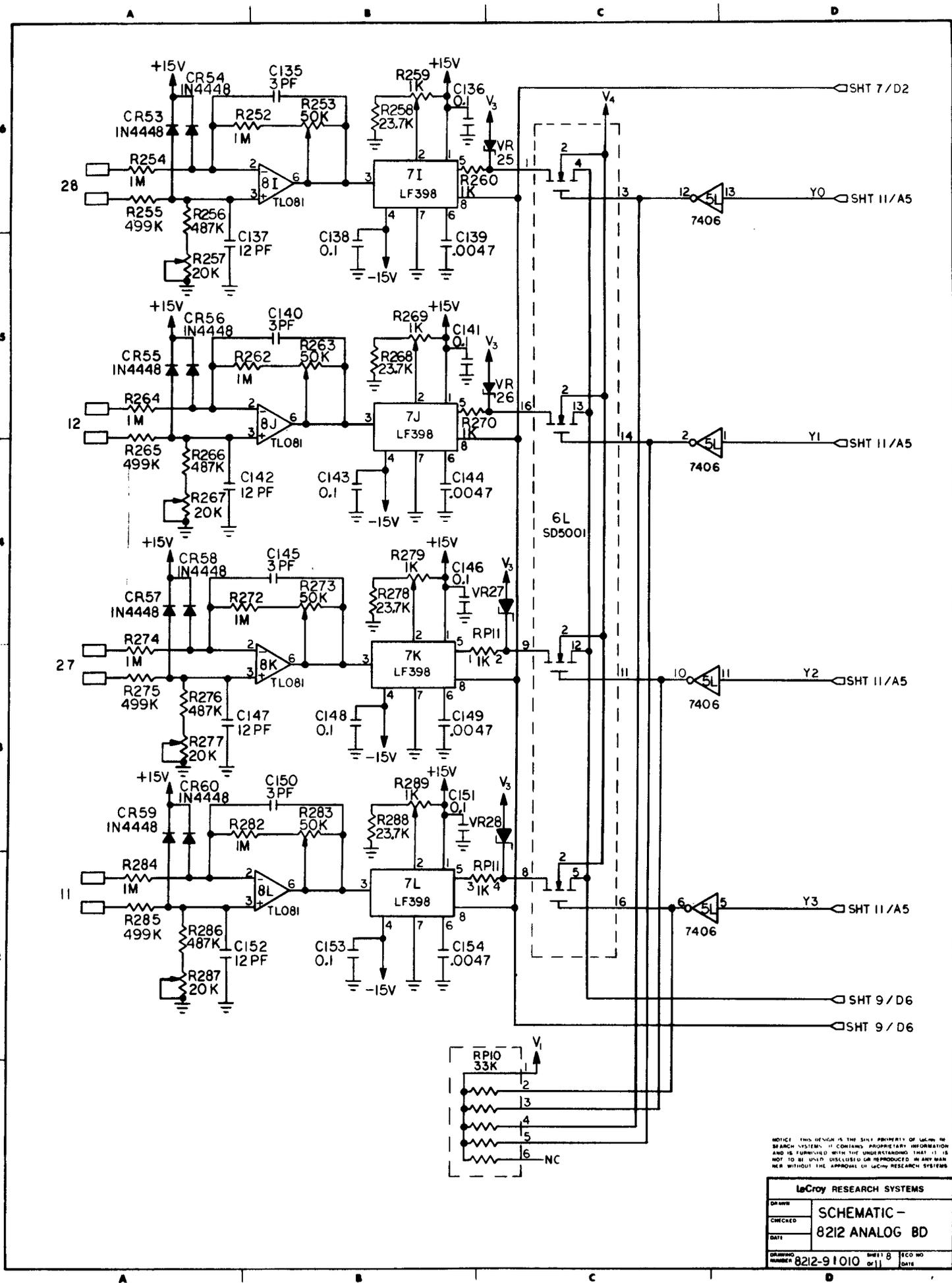
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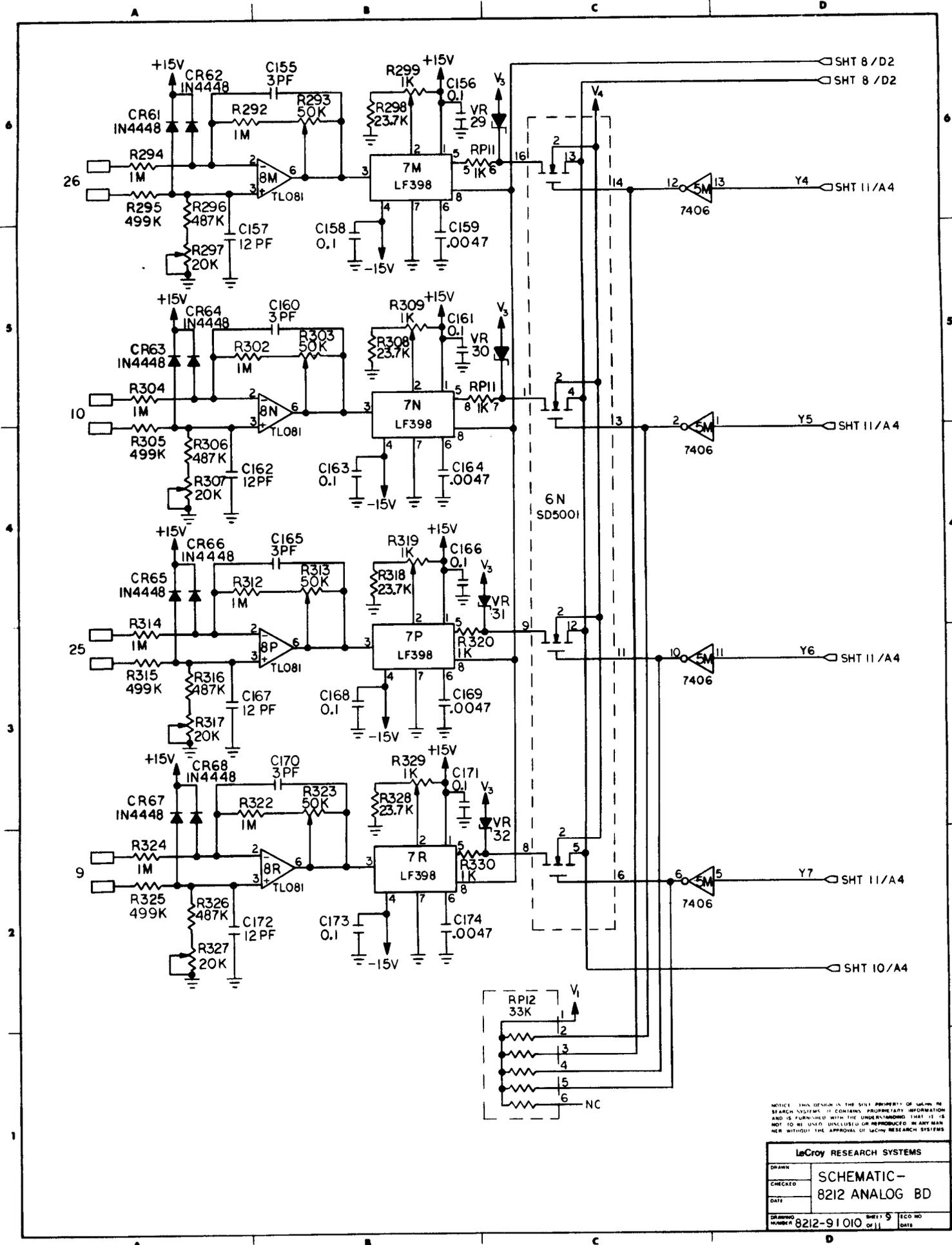
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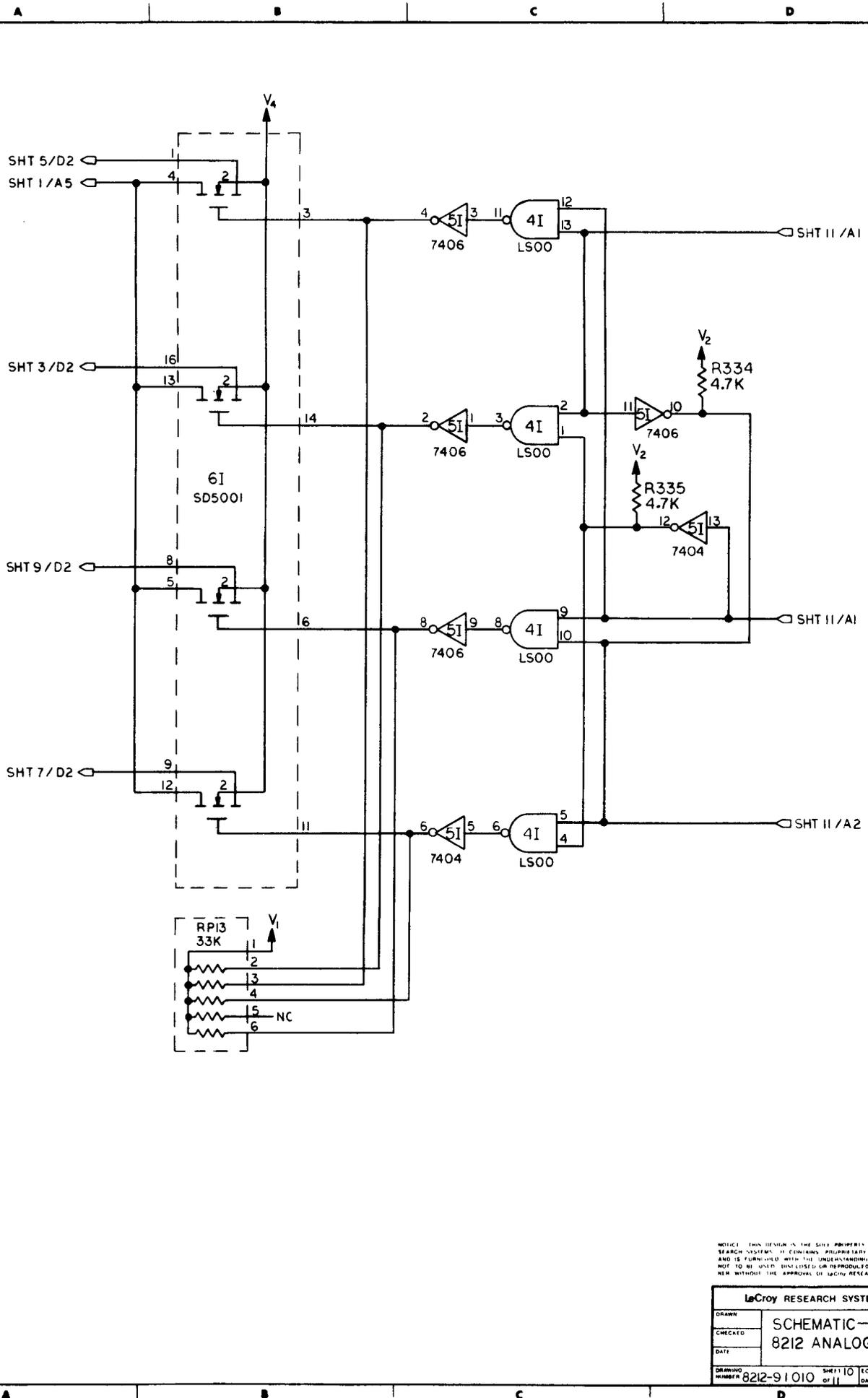
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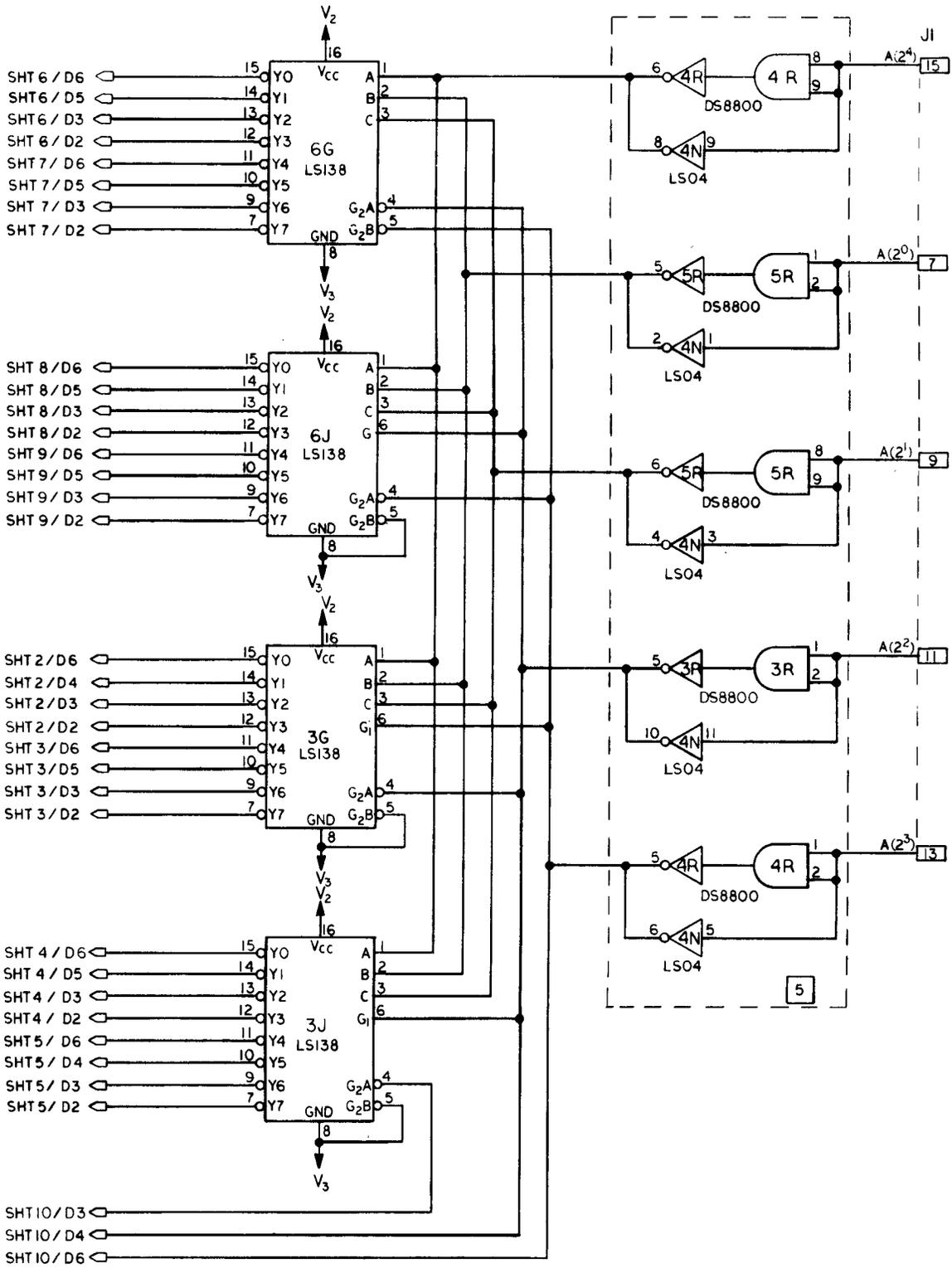
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|                         |                | OF    | 11 |
| ECO NO                  |                | DATE  |    |



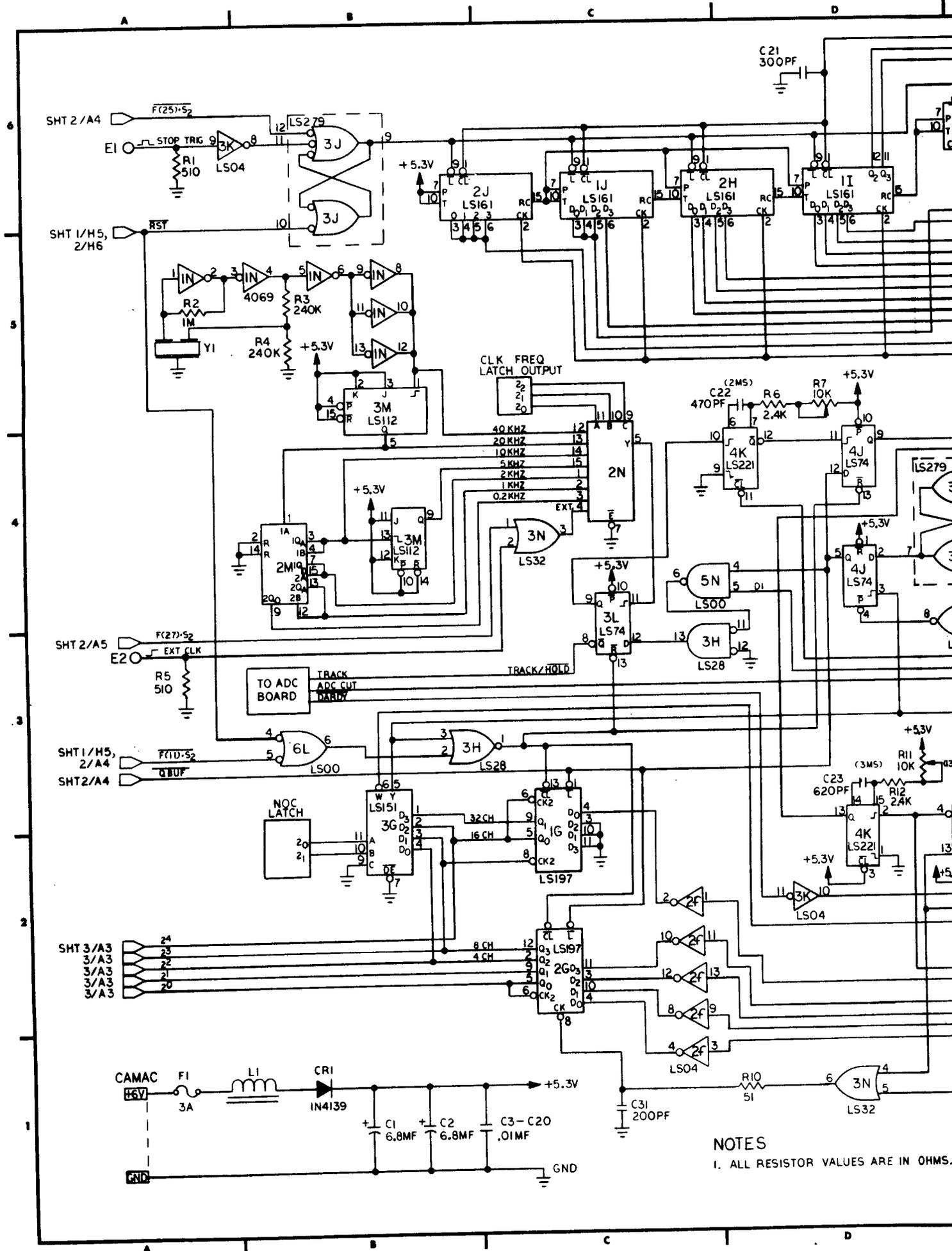
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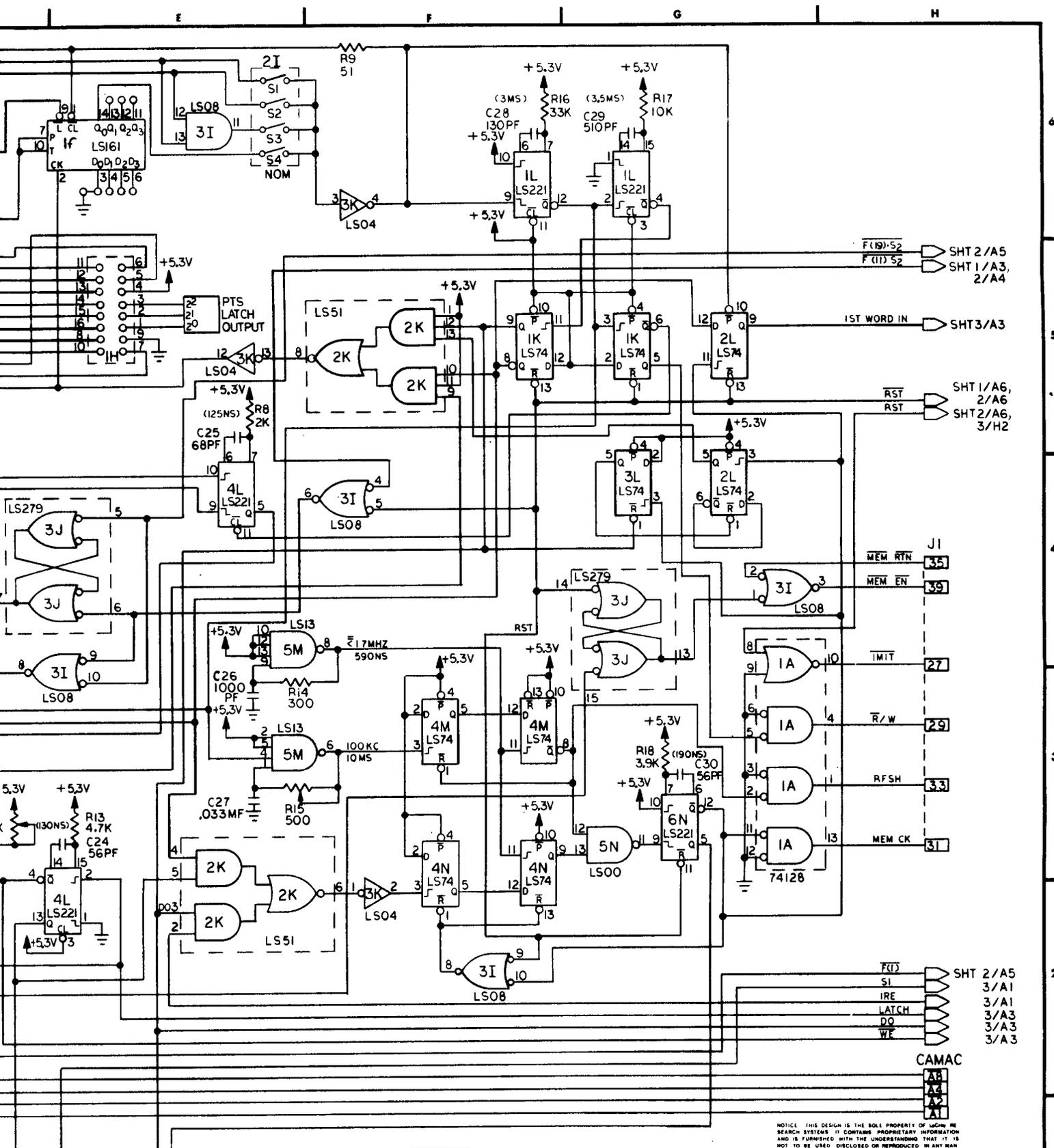


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| DATE                          |                                     |
| DRAWING NUMBER                | 8212 91010                          |
| SHEET                         | 11                                  |
| OF                            | 11                                  |
| ECO NO.                       |                                     |
| DATE                          |                                     |



NOTES  
 I. ALL RESISTOR VALUES ARE IN OHMS.



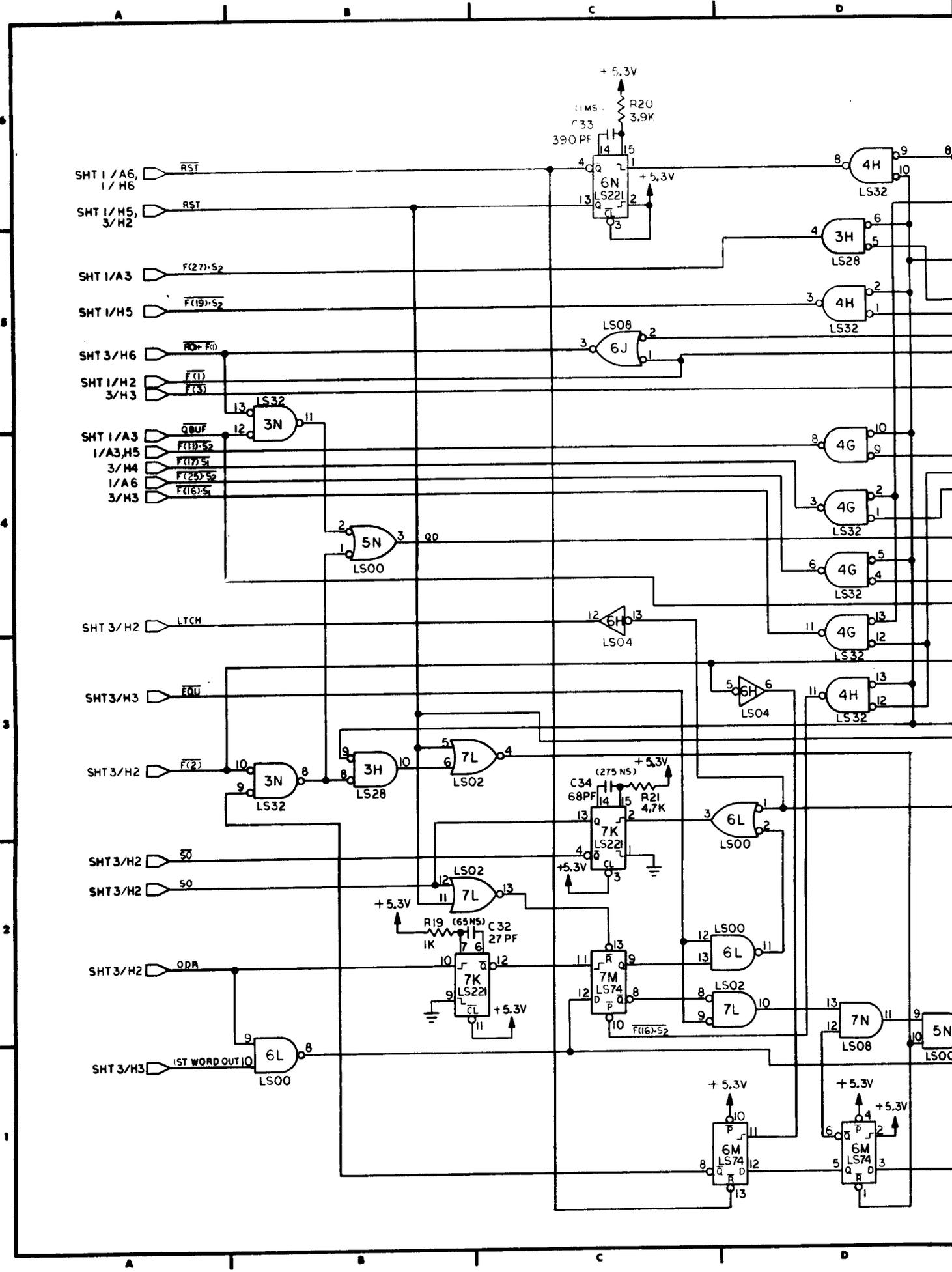
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| F1                     |          |
| E2                     |          |
| Y1                     |          |

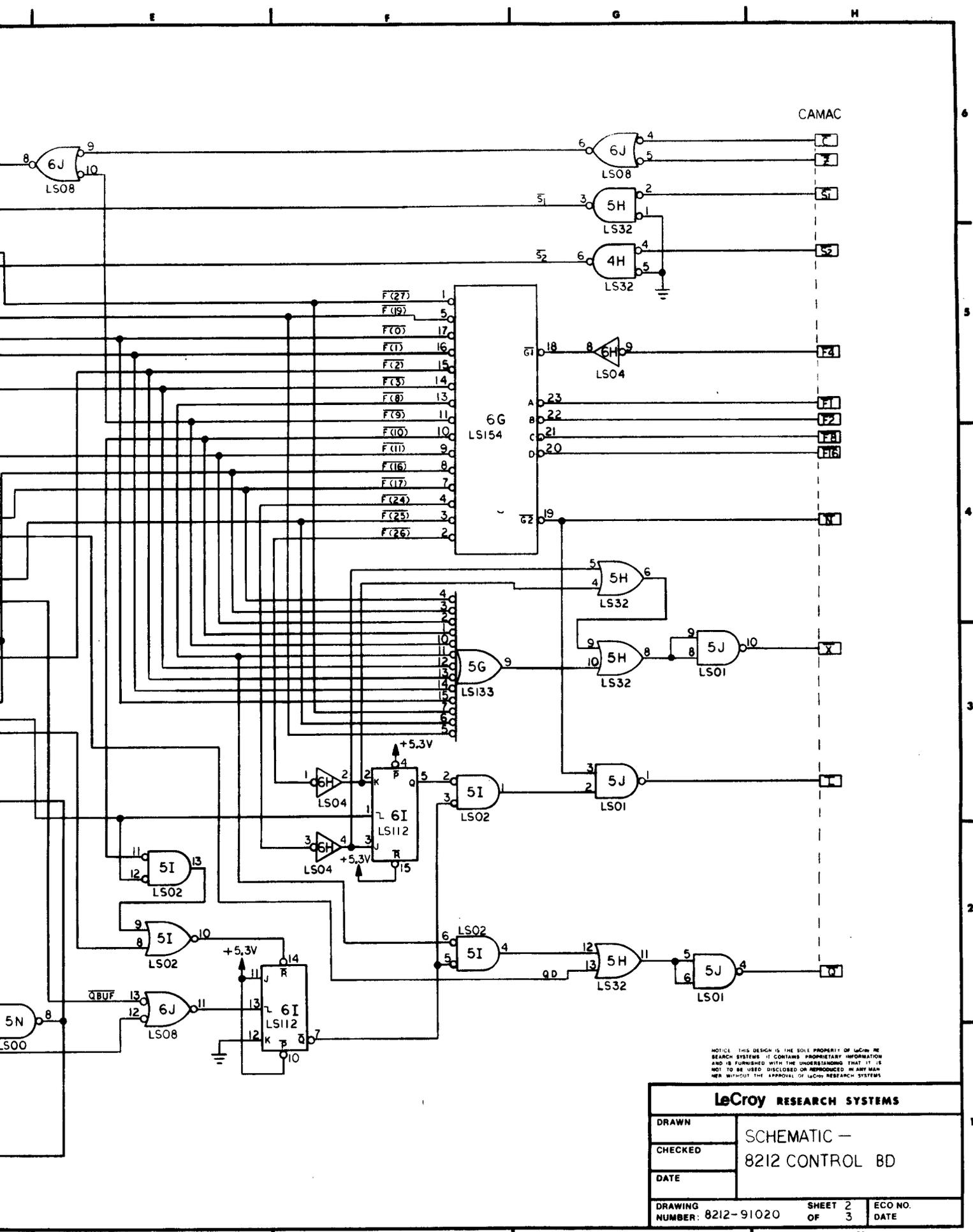
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**LeCroy RESEARCH SYSTEMS**

|                               |                                |
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| DRAWN<br>CWP                  | SCHEMATIC -<br>8212 CONTROL BD |
| CHECKED                       |                                |
| DATE<br>8 / 8 / 78            |                                |
| DRAWING<br>NUMBER: 8212-91020 | SHEET 1<br>OF 3                |
|                               | ECO NO.<br>DATE                |

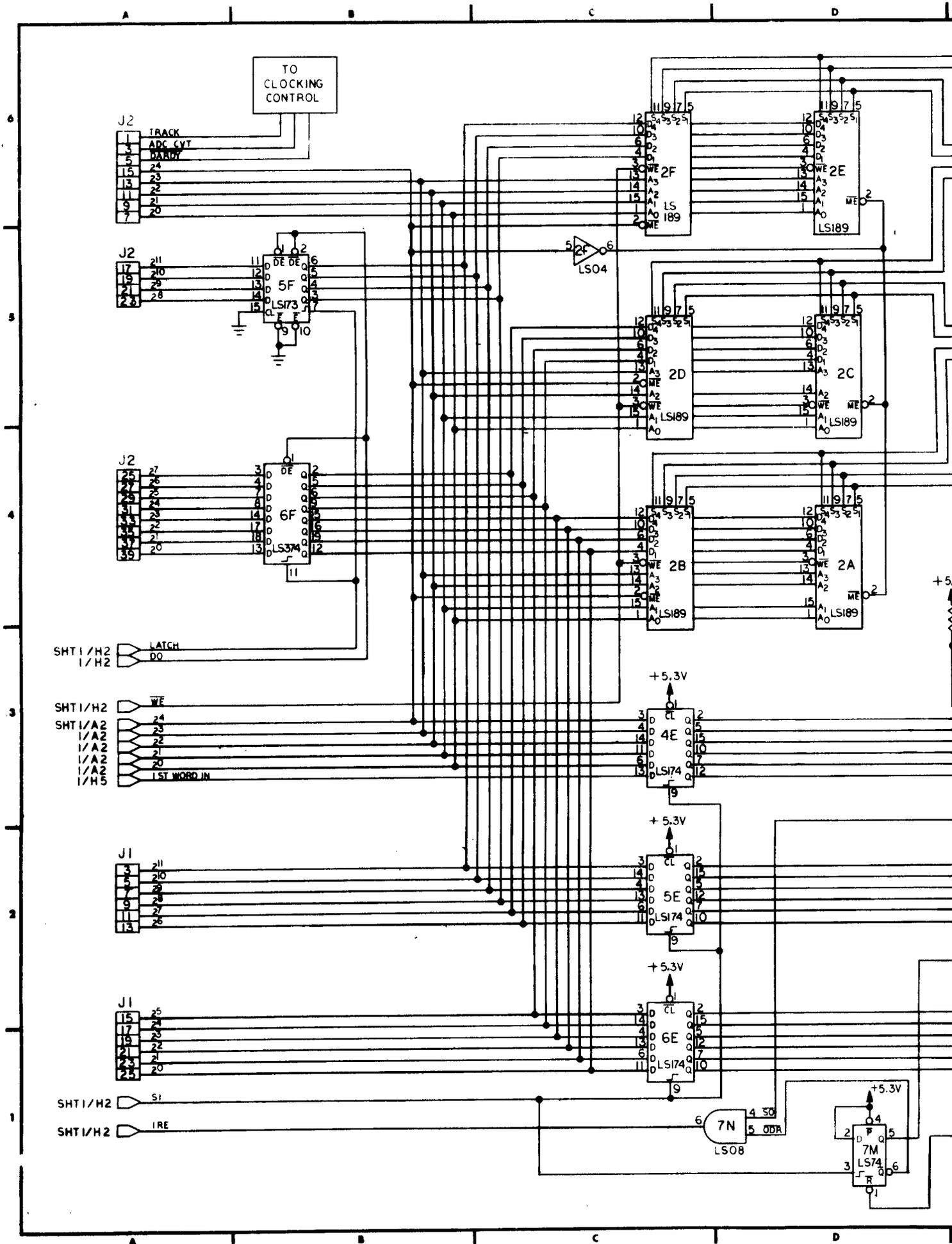
OHMS.

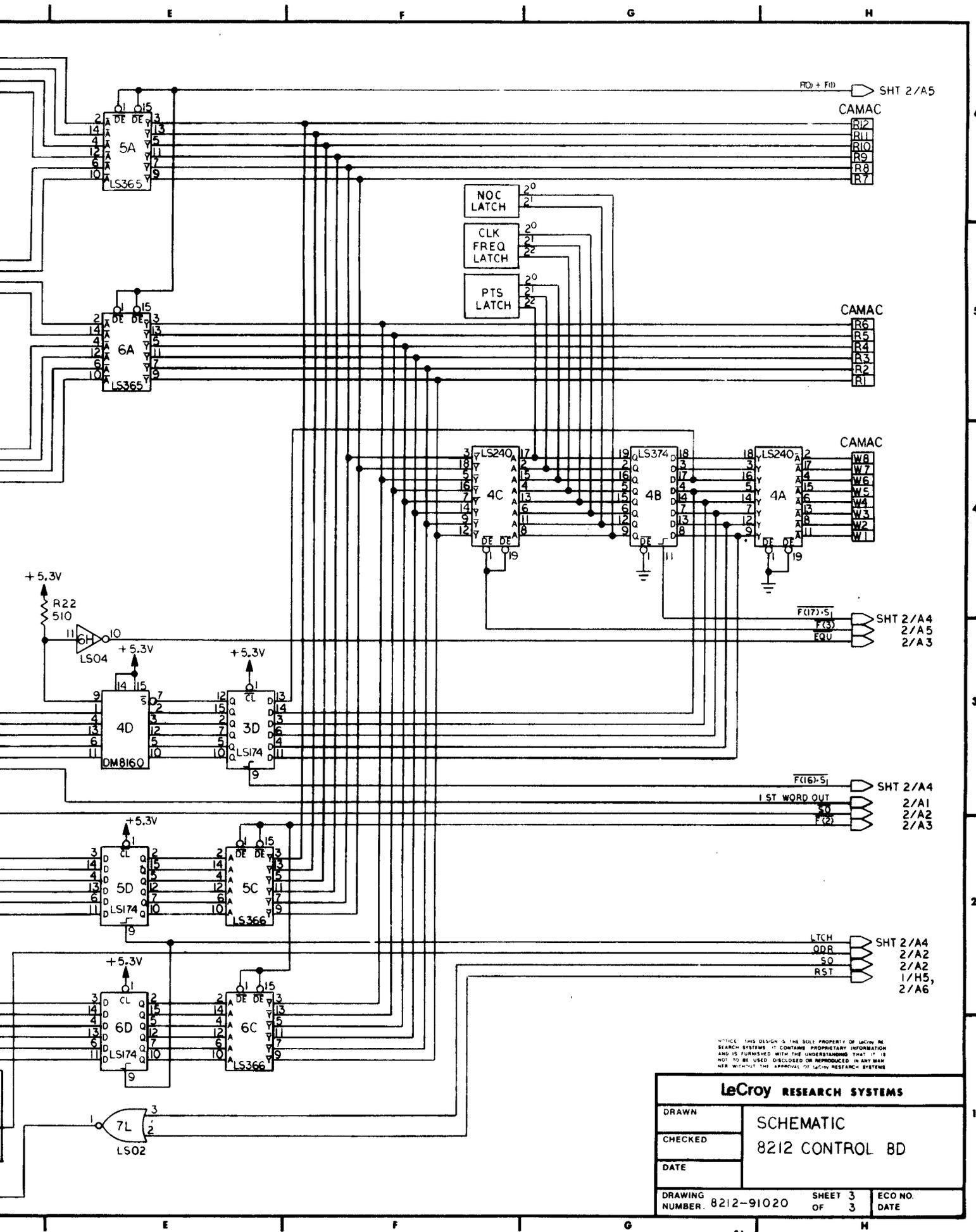




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| LeCroy RESEARCH SYSTEMS    |                                |              |
|----------------------------|--------------------------------|--------------|
| DRAWN                      | SCHEMATIC —<br>8212 CONTROL BD |              |
| CHECKED                    |                                |              |
| DATE                       |                                |              |
| DRAWING NUMBER: 8212-91020 | SHEET 2 OF 3                   | ECO NO. DATE |





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| <b>LeCroy RESEARCH SYSTEMS</b> |  |              |
| DRAWN                          | <b>SCHEMATIC</b><br><b>8212 CONTROL BD</b> |              |
| CHECKED                        |  |              |
| DATE                           |  |              |
| DRAWING NUMBER: 8212-91020     | SHEET 3 OF 3                               | ECO NO. DATE |