CICADA ENGINEERING SPECIFICATION	DOCUMENT NO. TFTR-10B4-H412
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	DATE - May 19, 1981
SUBJECT CAMAC Timing and Sequencing Module	PREPARED BY E. Lawson Ed Lawson

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DATE	DESCRIPTION

1.0 Abstract

This specification, in conjunction with referenced documents, sets forth all characteristics of the subject module. This specification shall take precedence where areas of overlap with the referenced documents occur. The intended use of this document is to provide a minimum design goal for the module as well as a working document for subsequent users.

2.0 Reference Documents

2.1 Standard Timing Pulse, TFTR-10A2-H57.

2.2 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Std. 583-1975.

2.3 Reliability, Quality Control and Temperature Cycling, TFTR-10A2-H58.

2.4 Printed Circuit Board Fabrication and Assembly Specification, TFTR-10A2-H54.

2.5 Printed Circuit Artwork Specification, TFTR-10A2-H53.

2.6 Electronic Schematic Specification, TFTR-10A2-H55.

2.7 Quality Assurance Plan, TFTR-9A1-002.

2.8 TFTR Cable and Connector Definition, TFTR-9C12-015.

3.0 Introduction

The Timing and Sequencing Module is a general purpose dual mode device, designed to provide a serial sequence of time related trigger or variable width pulse outputs. In Mode 1 the output is a series of fixed width pulses with the pulse-to-pulse separation determined by a stored program. In Mode 2 both the pulse-to-pulse separation and the pulse width are variable and are controlled by a stored program.

4.0 Basic Features

4.1 Mode 1

In Mode 1 a serial data stream of up to 1024 pulses shall be available at the output port. Each pulse shall have a nominal pulse width of one microsecond and shall conform to the specification in section 6.3. The pulses shall be programmed to occur at any fixed time up to 16,777,214 clock interval after the module is triggered. Once the module has been triggered it shall ignore all other input trigger pulses until the last requested pulse has been completed. A Cycle Complete output pulse shall be produced immediately after the completion of the last programmed pulse (see 11.4).

4.2 Mode 2

Mode 2 differs from Mode 1 in that the output pulse width is variable. Within 500nanoseconds of reset or the module being enabled, the output shall be a logic 0. When the first set point is reached the output shall switch to a logic 1 state. When the next set point is encountered the output shall switch to a logic 0 state. This cycle shall continue until the last set point has been reached. Up to 512 output pulses, each of which has a variable pulse width shall be allowed. The pulse width resolution is 1 clock interval. As an example, with the following times loaded (using a 10 microsecond clock):

Address	Number Loaded	Time(microseconds)
0	10	100
1	15	150
2	35	350
3	45	450

With the 10 microsecond clock, the mode two output waveform would be:

```
          -----                    ----------
          |   |                    |        |
----------     --------------------         -----------------
0        100  150                 350      450 microseconds
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The selection of mode 1 or mode 2 shall be via a front panel switch. The position of this switch shall be available to the CAMAC bus in the status word.

4.3 Clock

It shall be possible to use this module with a dataway clock (line P2) or with an external clock. The clock source shall be selectable by a front panel switch. The position of this switch shall be available to the CAMAC bus in the status word.

4.3.1 Dataway Clock

The dataway clock will operate at a nominal frequency of 1 MHz. The dataway clock will appear on dataway line P2 with signal levels corresponding to the CAMAC standard (reference 2.2). It shall be possible to divide this clock frequency by factors of 1, 10, or 100 by an internal adjustment. The selected dividing ratio will be obtainable by reading the status word. The dataway clock frequency will vary from 800 KHz to 1.5 MHz and will have a maximum rate of change of 500 KHz/sec. The clock waveform will be a rectangular pulse with a duty cycle between 50/50 and 60/40. The module shall operate as specified under these conditions of clock variation.

4.3.2 External Clock

If an external clock is used, the Clock Out connector shall provide a buffered version of the external clock as divided, with a

100 nanosecond maximum delay when loaded as shown in 11.2.2. The maximum external clock rate will be 1.0 MHz, with an acceptable clock waveform duty cycle of 10% to 90%. The electrical characteristics of this input are described in 6.2. The external clock shall be divided by the same internal divider as the dataway clock.

4.4 Internal Memory

The module shall contain a 24 bit wide by 1024 word long memory which is used to store the 1024 set times. Each of the output pulses is associated with a number from 0 to 1023 corresponding to the address of the setting in the memory. During the timing cycle the memory address shall be provided on the rear panel auxiliary connector (see 6.3 and 11.2) in binary form which allows the user to determine which pulse is occuring. On the trailing edge of the Mode 1 output pulse the address output at this connector shall be changed to the number of the next output pulse. In Mode 2 the address shall be changed 1 microsecond after the leading edge and trailing edge of the output pulse. If all 1024 output pulses are used, the address on the auxiliary connector will be zero after the final pulse.

4.5 Set Time Loading

This system shall have a resolution of 1 clock period and a maximum time of 16,777,214 periods. Each time setting requires a 24 bit binary number. The set times will be in order of increasing time. If an external clock operating at greater than 500 kHz is used, at least two microseconds between consecutive output time settings must be provided, for example: 10.000000---10.000002 seconds. If this condition is not met the results will be unpredictable. If the

external clock is operating at less than 500kHz the set times can be separated by only one clock interval.

4.6 Number of Output Pulses

It shall be possible to use fewer than the maximum number of output pulses. If fewer than the maximum number of set times are to be used, a word of all ones will be loaded into the memory after the final desired time setting. A time setting of all ones shall be a flag that the cycle is complete and not the value of 16,777,215 clock periods.

4.7 Recycle Mode

The module shall be capable of retriggering itself at the end of each timing cycle. In this mode the number of cycles will be specified when the module is loaded. The maximum number of cycles shall be 255. If 0 cycles are selected the module shall retrigger indefinitely, until it is reset or disabled.

4.8 Trigger Input

The Trigger Input shall require a pulse of at least 500 nsec in duration. The electrical characteristics of this input are defined in 6.2.

4.9 Cycle Complete Output

This output shall be a 1 microsecond wide pulse that occurs at the end of each cycle. This pulse shall occur less than 500 nanoseconds after the trailing edge of the final Mode 1 output pulse or 1.5 microsecond after the trailing edge of the Mode 2 output pulse (see 11.4). The electrical characteristics of this output are defined

in 6.3.

4.10 Retrigger Mode

In the retrigger mode, on the falling edge of the last cycle complete output pulse the internal state of the module shall be reset so that the module may be triggered at a later time. The subsequent trigger will not occur until 1 microsecond after the falling edge of the cycle complete pulse, or it may be ignored. The retrigger mode shall be selectable by a front panel switch. If the retrigger mode is not selected an enable command must be issued before the module can be triggered.

4.11 Status Lights

4.11.1 N

The N light shall be illuminated when the module is addressed by the CAMAC N line. It shall remain on for a minimum of 0.1 seconds after the N line goes to a logic 0.

4.11.2 A

The A light shall be illuminated when the module is enabled and ready to be triggered.

4.11.3 C

The C light shall be illuminated when the module has been triggered and is counting.

4.11.4 O

The O light shall be illuminated for a minimum of 0.1 seconds when the output is high.

4.11.5 R

The R light shall be illuminated for a minimum of 0.1 seconds when a

module cycle is started, by the external trigger or when recycling.

5.0 Mechanical Characteristics

5.1 This shall be a standard single width CAMAC module as specified in reference 2.2.

5.2 This module shall conform to the mechanical requirements outlined in reference 2.2.

5.3 The electrical components of this module are to be mounted on a high quality flame retardent epoxy glass printed circuit board such as NEMA type FR-4 or equivalent. See references 2.4 and 2.5.

5.4 This module is to contain all necessary mechanical components, including metal covers, for insertion into a standard CAMAC crate. See reference 2.2.

5.5 All components are to be identified with a standard manufacturer's part number or standard method of marking (e.g. resistor color code).

5.6 All electrical components are to be mounted on only one side of the board.

5.7 The condition of this module shall be monitored by front panel mounted LED's. The front panel shall be of aluminium and both sides are to have a conductive iridite finish. The color of the lettering shall be chosen to contrast with the panel finish and may be engraved or silk screened. See 11.1 for the suggested front panel layout.

5.8 The 36 pin card edge connector shall mate with a Viking 3V18 connector (or equivalent). The card edge connector shall be marked with pin 1 on top and pin 18 on the bottom on each side of the card. It is not necessary to mark each pin.

5.9 All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part

number on the electrical schematic associated with this module. See reference 2.6.

5.10 All front panel connectors shall be 3 pin LEMO type connectors wired in accordance with the TFTR cable and connector specification (reference 2.8). The auxiliary output connector shall be wired as shown in section 11.2.

6.0 Electrical Characteristics

6.1 Input Power

6.1.1 This module shall conform to the electrical requirements outlined in reference 2.2.

6.1.2 Whenever possible, low power circuitry (such as CMOS or 74LS series) shall be used to minimize power dissipation.

6.1.3 The module shall derive its input power from the standard +/-24 volt and +/-6 volt CAMAC supply voltages.

6.1.4 The +6 and -6 volt supply voltages shall be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages shall be bypassed with electrolytic capacitors of at least 6.8 microfarads. In addition, at least half of the integrated circuits shall contain ceramic bypass capacitors of at least 0.01 microfarads on their supply voltage lines. The 0.01 microfarad capacitors should be located as close as possible to the integrated circuits and distributed equally across the board.

6.2 Input signals

All dataway signals are specified in reference 2.2. Other inputs shall be terminated with approximately 120 ohms, and shall be optically isolated from the module (see 11.3 for a typical input

stage). Non-dataway inputs shall be a minimum of 3.5 volts into the rated load. The Trigger Input shall be capable of being triggered by a TFTR standard timing pulse (reference 2.1).

6.3 Output Signal Characteristics

The Clock, Cycle Complete, Mode1/Mode2 outputs and the auxiliary connector outputs shall be differential and shall be capable of driving 120 ohms (see 11.2.2 for a typical output stage). The differential output voltage shall be at least 3.5 volts into the rated load. A HCPL-2601 optically coupled line receiver, in the module to be controlled, is recommended. The Mode 1, Cycle Complete and Clock Out outputs shall have the same timing characteristics as the TFTR standard timing pulse. The Mode 2 output shall have the same rise and fall times as the TFTR standard timing pulse.

6.4 CAMAC Protocol

6.4.1 Load address register A(2).F(16).Write

Address on lines W1-W10 with LSB on W1.

6.4.2 Read set point and increment address A(0).F(0).Read

Set point read on R1-R24 with LSB on R1.

6.4.3 Write set point and increment address A(0).F(16).Write

Set point on W1-W24 with LSB on W1.

6.4.4 * Disable unit A(0).F(24)

This stops the timing cycle and leaves the outputs in whatever state they were in when this command was executed. In Mode 1 the pulse output shall finish and then remain in the logic 0 state. In Mode 2 the output shall not change state.

6.4.5 Enable unit A(0).F(26)

The module must be enabled before it can be triggered.

6.4.6 * Read Module Number A(0).F(6).Read

This produces bit pattern 0000 0000 0000 0001 1001 1100 on the CAMAC bus.

6.4.7 * Read Status Register A(1).F(0)

Bit 1	1=Enabled	0=Disabled
Bit 2	1=Internal Clock	0=External Clock
Bit 3	1=Mode 2	0=Mode 1
Bit 4	1=Retrigger On	0=Retrigger Off
Bit 5	1-Divide Clock by 1	
Bit 6	1=Divide Clock by 10	
Bit 7	1=Divide Clock by 100	

Bits 8-24 0

The enabled bit shall go to logic 0 at the end of the timing cycle unless retrigger mode is selected

6.4.8 * Read Memory Address A(2).F(0)

Bit 1	Memory Address Bit 0 (LSB)
Bit 2	Memory Address Bit 1
Bit 3	Memory Address Bit 2
Bit 4	Memory Address Bit 3
Bit 5	Memory Address Bit 4
Bit 6	Memory Address Bit 5
Bit 7	Memory Address Bit 6
Bit 8	Memory Address Bit 7
Bit 9	Memory Address Bit 8
Bit 10	Memory Address Bit 9 (MSB)

Bits 11-24 0

6.4.9 Set Number of Cycles A(1).F(16).Write

0	Recycle until module is disabled or reset
1-255	Normal recycle mode

Default of 0 on reset
Recycle data is on lines W1-W8 with LSB on W1

6.4.10 * Reset C+Z+Power On

Note: Only those dataway functions marked with a * shall be accepted during the timing cycle; all others shall be ignored. The X line shall be a logic 1 whenever the module is provided with one of the

above commands and 0 otherwise. The Q line shall be a logic 1 only when the module is provided with one of the above commands except during the timing cycle when only the commands marked with a * shall cause Q to be 1.

7.0 Environmental Data

7.1 The module shall operate, as specified, over an ambient temperature range of 0 to +50 degrees C.

7.2 The module shall operate, as specified, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module shall operate, as specified, in the presence of an external magnetic field, changing at a maximum rate of 100 gauss per second, with a peak magnitude of 200 gauss in any direction.

7.4 The module shall operate, as specified, in a radiation environment as follows:

Neutrons:	2×10^{7} n/cm^{2}/sec
Rad-dose:	5×10^{-2} rad(Si)/sec
Integrated dose:	200 rad (Si)

8.0 Safety

All components of this module shall be of flame retardant material.

9.0 Testing

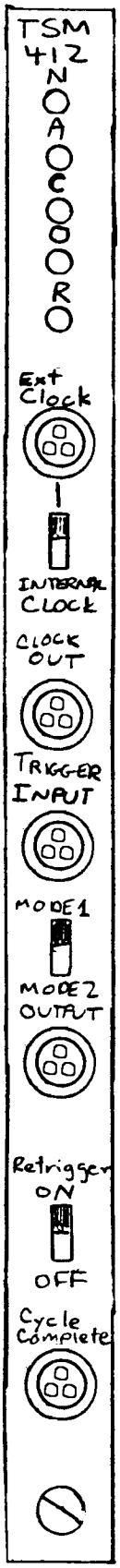
All modules shall be subjected to a temperature cycling period followed by a functional test prior to shipment. A description of the tests to be performed shall be submitted by the seller for approval and for incorporation into this specification. A copy of the test report shall be delivered along with the module.

10.0 Reliability and Quality Control

The module shall meet all applicable requirements specified in reference 2.3.

11.0 Diagrams

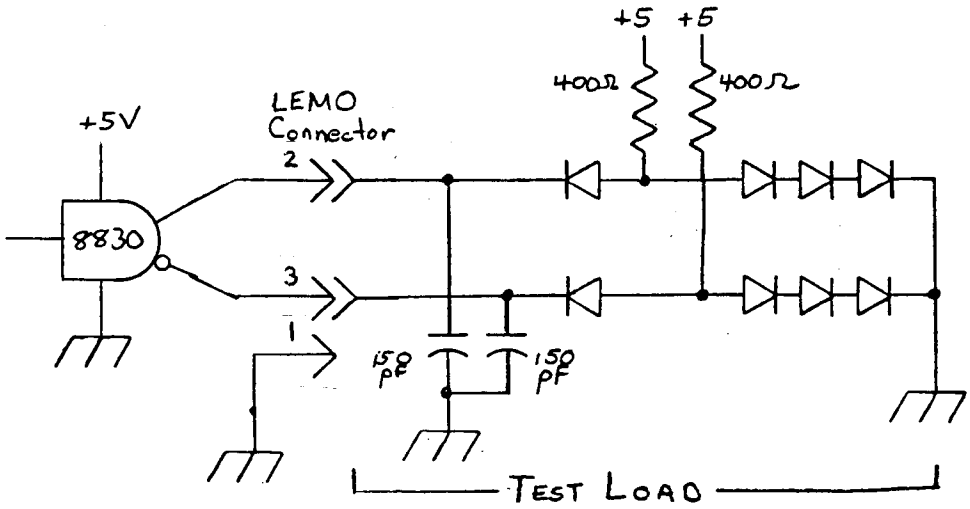
11.1 Proposed Module Front Panel



11.2.1 Auxiliary connector pin-out

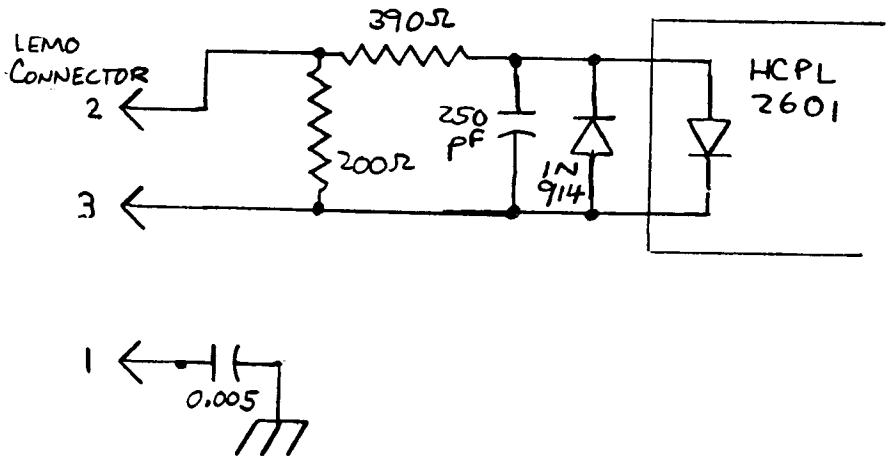
Signal	Non-Inverted Output	Inverted Output
Bit 0 (LSB)	1A	1B
Bit 1	2A	2B
Bit 2	3A	3B
Bit 3	4A	4B
Bit 4	5A	5B
Bit 5	6A	6B
Bit 6	7A	7B
Bit 7	8A	8B
Bit 8	9A	9B
Bit 9 (MSB)	10A	10B

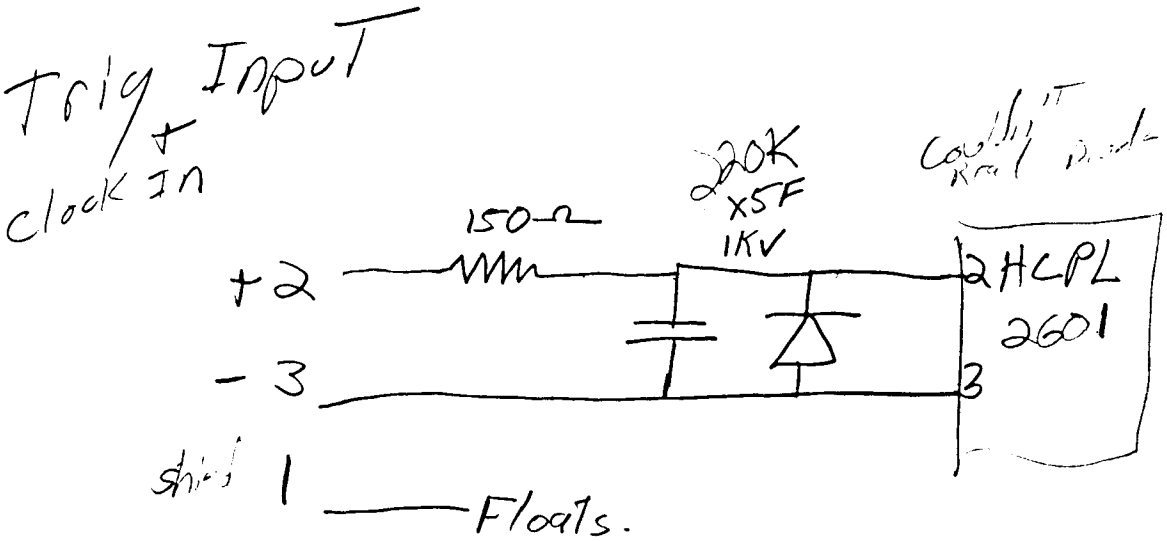
11.2.2 Cycle Complete, Timer Output and Clock Out: Output Stage



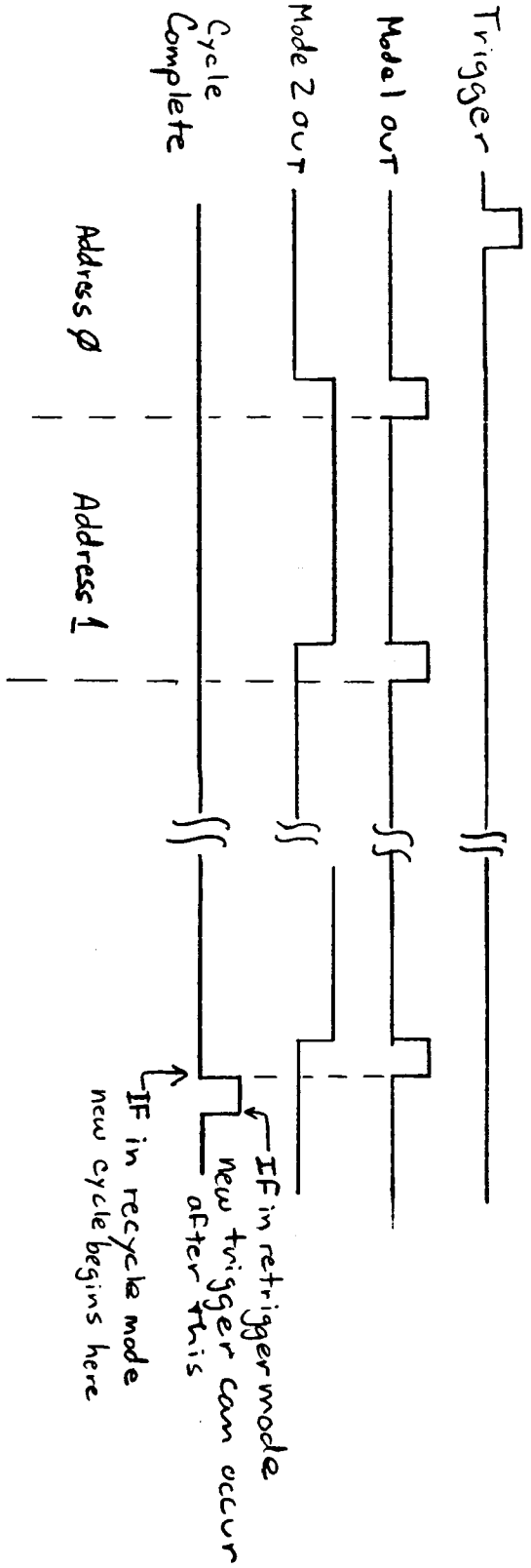
Typical Output Stage

11.3 Typical Input Stage





11.4 Timing Diagram



Princeton University: DEPARTMENT - Computer Division -

To R. Daniels

DATE 8 May 1984

SUBJECT H412 Timing and Sequenceing Module

FROM H. Feng

H. Feng

We have discovered that the H412 Timing and Sequencing Module address lines on the auxiliary connector have the opposite polarity output with respect to the CICADA tradition. In addition, the outputs are differential type. All users be aware of this. Meanwhile, the document TFTR-10B4-H412 should be clarified.

	Auxiliary Connector	
Output	"A" Side	"B" Side
"One"	H	L
"Zero"	L	H

HF/plm

cc: D. Shuster
All CICADA Hardware Engineers
All CICADA Technicians

INTER-OFFICE CORRESPONDENCE

P2 GLITCH PROBLEM

John Wertenbaker 3/17/00

It was discovered that the P2 line on the CAMAC dataway can contain glitches that are caused by the capacitive coupling of the 1Mhz P2 line and the function (F) lines. The F(16) line, which is just opposite of P2 has the greatest coupling, but the more F lines that are active, the larger the glitch will be on P2. This glitch can vary from crate to crate, and from slot to slot, but, in one case it was measured at 2 volts.

The glitch can cause any module that uses the P2 line, like the 408, 409, 412, 413, and 908 modules, to count an extra clock pulse, causing timing errors in any system that uses those modules. Below is a list of the modules that derive their clock from the P2 line, and a description of the input circuitry in each module.

408 P2 input goes to a 74LS28, which is a NOR gate.
409 P2 input goes to a 74123 one-shot.
412 P2 input goes to a 74LS38, which is a NAND gate.
413 P2 input goes to a 74LS02.
904 P2 input goes to a 74LS14 Schmitt-trigger inverter.
908 P2 input goes to 3 74LS74's and 2 74LS08's.
910 P2 input goes to a 74LS14 Schmitt-trigger inverter.
912R P2 input goes to a 74LS14 Schmitt-trigger inverter.
914 does not use the P2 line.

The 409 Timed Gate module was the only module that was tested and proven to be susceptible to this glitch. The 408, 412, 413, and 908 modules are assumed to be susceptible, also, based on their input circuitry. The 904, 910, and 912R modules are much more tolerant of this glitch, due to the Schmitt-trigger inputs, and are probably not affected. The 914 module generates its own 1Mhz, and is independent of the P2 line.

This occurrence of this problem is rare due to the nature of clock cycles in NSTX, and its predecessor, TFTR. In those machines, most modules are set up and armed long before any trigger pulse starts the counting of P2 clock pulses. Very few CAMAC commands are performed after these arm and setup commands. In most cases, the only commands that come through during the counting times are read-back commands and L-2 crate controller wakeup commands. These happened every 2 seconds in TFTR, and even less often than that in NSTX. Also, most of the time, the 1Mhz P2 line is divided down to a much lower frequency, so a few microseconds of inaccuracy would not be noticed.

For the rare cases when the glitches can cause problems, such as the Facility Clock Generator crates, the recommended fix is to insert a P2 Capacitor Filter Module in the crate as close as possible to the module that uses the P2 line. This module contains a 1000pf capacitor from the P2 line to ground. This attenuates the high frequency of the glitch, without seriously rounding off the edges of the 1Mhz P2 signal.

It should be noted that the 404A had a similar problem with the P1 line. The BUSY line, which is an un-terminated line in the crate, was coupling a glitch over to the P1 line. The repair for that problem was to install a Schottky diode on the BUSY line to clamp the negative-going overshoot at the low-going transition of the BUSY pulse, and replace the 74LS04 with a Schmitt-trigger 74LS14 at the P1 input. However, it was not considered practical to modify every module that uses the P2 line because the problem is much more rare than the P1 problem, due to the nature of when the glitch occurs.

412 Recycle Times

John Wertenbaker 9/8/2000

When using the recycle mode, it was found that there is a delay between the end of the current cycle and the beginning of the next cycle. The delay depends on the selection of the clock divide jumpers. These delays are as follows:

Jumper	Delay
1µSec	5µSec
10µSec	20µSec
100µSec	200µSec