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	PAGE 1 OF 25
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SUBJECT: Time Base Module	PREPARED BY: H. Del Gatto

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DATE	DESCRIPTION
12/19/85	Revised to reflect as-built

Time Base Module

1. Abstract.

This specification, in conjunction with referenced documents, sets forth all characteristics of subject module. This specification shall take precedence where areas of overlap with referenced documents occur. The intended use of this document is to provide a minimum design goal for the module as well as a working document for subsequent users.

NOTE: Revisions from the previous issue of this document are identified by a vertical bar in the outer margin of the page.

2. Referenced Documents.

2.1. IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Std. 583-1975

2.2. Printed Circuit Board Fabrication and Assembly Specification, Document TFTR-10A2-H54B

2.3. Electronic Schematic Specification, Document TFTR-10A2-H55

2.4. Printed Circuit Artwork Specification, Document TFTR-10A2-H53A

2.5. Reliability, Quality Control, and Temperature Cycling, Document TFTR-10A2-H58

2.6. Standard Timing Pulse, Document TFTR-10A2-H57

2.7. Facility Clock Subsystem, Document TFTR-10B4-H401

3. Introduction.

The CAMAC module specified will be used as an interface between elements of the Tokamak Fusion Test Reactor (TFTR) and the Central Instrumentation Control and Data Acquisition (CICADA) computer system. The module will be housed in a CAMAC crate (Reference 2.1). The module will serve as a programmable clock generator that may be used to drive devices such as transient digitizers and function generators.

4.0 Basic Features

The module shall be a single width CAMAC module that shall provide a programmable clock output. The module will derive its output clock signal from the CICADA clock system available on Dataway line P2. It shall be capable of providing various sequences of clock frequencies and burst durations in response to CAMAC commands and to trigger signal inputs. A sequence of desired frequencies as well as a duration for each frequency shall be programmed into the module prior to its use. A desired frequency along with a related duration, control flags and recycle count shall constitute a "domain". The module shall be capable of storing sixteen (16) such domains for sequencing after being armed. Each domain shall have a commanded frequency and pulse count associated with it. Available frequencies shall follow a 1, 2, 5 sequence from 10Hz to 500KHz and shall also allow for zero frequency which essentially turns off the output during the corresponding domain. Available durations shall be from 1 to 16,777,215 clock pulses. In addition, the loading of a count of zero will be reserved to be used when a continuous pulse train is desired. Advance from domain to domain shall be programmed to occur either in response to trigger pulses or in response to the completion of the desired number of clock pulses. Each domain shall have two bits of data associated with it to establish the desired response to incoming trigger signals.

4.1 "Wait For Trigger" feature

Each domain shall have a "Wait For Trigger" (WFT) bit that shall be loaded into the module when the frequency for the domain is loaded by CAMAC command. The WFT bit shall be used to cause a given domain to wait for a trigger signal before commencing output. Upon the start of a specific domain this bit will be tested. If the bit for the domain is set to logic 1 then the frequency output associated with the domain will not commence output until a trigger signal is received. If the bit is set to logic 0 then the domain output shall commence immediately.

4.2 "Advance On Trigger" feature

Each domain shall have an "Advance On Trigger" (AOT) bit that shall be loaded at the same time as WFT bit. The AOT bit shall be used to cause the module to terminate the active domain and advance to the next domain in response to a trigger signal. If this bit for a given domain is set, then upon receipt of a trigger an active domain will immediately stop its frequency output and advance to the next commanded state. The AOT bit feature shall only be in effect after the domain is "active". If a given domain has both the WFT and the AOT bits set to 1, then the first trigger sensed will cause the domain to go active and commence output and the second trigger will cause the domain to terminate. It should also be noted that the AOT feature is logically "ORed" with the domain duration. A domain with a duration other than zero (continuous) will therefore advance upon the earliest occurrence of either completion of the commanded duration count OR the receipt of a trigger signal. If a domain is configured (loaded) with zero duration and with the AOT bit set to 0 then the domain will continue until terminated by CAMAC command.

4.3 Domain Cycling

Each domain shall be capable of recycling itself for up to fifteen (15) times to result in the same domain occuring up to sixteen (16) consecutive times. A four (4) bit data field associated with each domain will be used to control the number of times each domain will cycle within a sequence. The recycling or restarting of the domain will commence immediately as the domain ends its last active period. When a domain recycles it will function in an identical fashion as it initially functioned, subject to control by the same frequency, duration and flag (WFT and AOT) data.

4.4 Sequence Definition

The module may be configured to use any number of domains, from one (1) to sixteen (16), to make up a desired sequence. A sequence will therefore consist of some number of domains (1 to 16) with each domain capable of cycling up to sixteen (16) times. In addition, the module may be configured to cycle its entire sequence for from one (1) to sixteen times or it may be configured to recycle through its entire sequence continuously until stopped by a CAMAC "Disable" command or by a "Disable" input pulse.

4.5 Trigger Input

The module will provide a trigger input connector and a trigger inhibit connector on the module front panel. In addition, the module will be cabable of responding to a CAMAC trigger command in the same way as it responds to a trigger input pulse signal. The two trigger sources (CAMAC and pulse input) shall be logically ORed together within the module. The trigger inhibit input shall be a "driven" type input such that trigger signals will be enabled (not inhibited) when no connection is made to this port. All trigger signals (CAMAC and pulse) will be ignored when the trigger inhibit input is driven to the true state.

4.6 Clock Inhibit Input

The module will provide a clock inhibit connector on the front panel that may be used to inhibit the output clock signal. Like the trigger enable, this input will be a driven input so that the clock is enabled when no connection is made to this port. When this input is driven by an external signal the output clock will be inhibited and the domain count stopped.

4.7 Disable Module Input

The module will provide a connector on its front panel for the purpose of forcing the module into the disabled state. This input port shall accept a pulse signal which will cause the module to stop any pulse train output and will cause the module to go into the disabled or unarmed state. All domain data storage as well as the sequence identifier data will not be affected by this signal. After a module has been disabled by this input it may simply be reenabled by CAMAC command to restart an output sequence identical to the previous one. In addition, the module will respond to a "Disable" CAMAC command that will effect the module in an identical fashion.

4.8 Pulse Output Ports

In addition to the Clock output port, the module shall provide three output ports to facilitate time tagging or synchronization of external devices. The TRIG OUT port shall output a pulse whenever module receives a trigger signal (Dataway or external). The DOM STRT port shall output a single pulse when a new domain goes to the active state. A domain with the WFT set to 0 will output a DOM STRT pulse immediatly upon being entered while a domain with WFT set to 1 will not output a DOM STRT until a trigger is sensed to start the domain output frequency. The DOM STRT output shall be issued in an identical fashion each time a domain goes active, including each time the domain recycles. The EOS (End of Sequence) port shall output a single pulse at the end of domain sequence. This pulse shall occur immediately as the last domain in the commanded sequence is terminated. When the module is configured in the recycle mode then this pulse will be issued as the last domain is completed and the first domain entered, thus, serving as a "recycle" pulse output.

4.9 Auxiliary Connector Utilization

In addition to the front panel connectors, the module shall provide the same input/output connection points on the rear auxiliary connector. The rear connection points shall be electrically parallel with the front panel connection points.

5.0 Mechanical Characteristics

5.1 The module will conform to mechanical specifications as indicated in reference 2.1.

5.2 The module shall be a single width CAMAC module.

5.3 The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA Type FR-4 or equivalent. The circuit board shall be a two sided printed circuit board with etched conductors. The fabrication of the circuit board shall be in compliance with reference specification 2.3.

5.4 All components are to be identified with a standard manufacturer's part number or standard method of marking (e.g., resistor color coding) and shall have an exact replacement available from a second source manufacturer.

5.5 This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate. See reference specification 2.1.

5.6 All electrical components are to be mounted on only one side of the board.

5.7 The condition of this module is to be monitored by LED's located on the module front panel. See Figure 11.1 for the suggested front panel layout. All lettering on the front panel shall be either engraved or silkscreened. The front panel material shall be aluminum with an iridite finish with contrasting colored lettering.

5.8 All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part number on the electronic schematic associated with this module. See reference specifications 2.3 and 2.4.

5.9 The front panel connectors J1 through J8 shall be used for trigger input (TRIG IN), trigger enable (TRIG EN), clock input (CLK IN), disable input (DISAB), clock output (CLK OUT), trigger output (TRIG OUT), domain start (DOM STRT) and end of sequence (EOS). The connectors shall be 3 pin LEMO connectors and shall conform to the pin assignments given in Figure 11.2. Pins 2 and 3 shall be used for signal high and signal low, respectively. Pin 1 shall be connected to ground for output ports and shall have a .01 microfarad capacitor to ground available for input ports. The .01 uf capacitor may be selectively used by installing a printed circuit jumper.

5.10 The module shall provide interface points on the rear 36 pin auxiliary connector. Each front panel interface point shall have a corresponding point available on this connector wired in parallel with it. The pin assignment for the auxiliary connector shall conform to that given in Figure 11.4.

5.11 The module shall be equipped with grounded, conductive side panels.

6.0 Electrical Characteristics

6.1 Dataway Interface shall conform to specification as indicated in reference 2.1.

6.2 Input Power shall be derived from the standard +/- 6 volt and +/- 24 volt CAMAC supply voltages. Whenever possible, low power circuitry (such as the 74LS series) shall be used

6.3 The +6 and -6 supply voltages must be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages must be bypassed with electrolytic capacitors of at least 6.8 microfarads. In addition, at least half the integrated circuits must contain a ceramic bypass capacitor of at least .01 microfarads on their supply voltage lines. The .01 microfarad capacitors should be distributed on the circuit board and be located as close as possible to noise sensitive components.

6.4 The +5 volt and ground lines for TTL logic may be carried on insulated sandwich type busses which are located under the dual in-line IC packages.

6.5 All components on this module must have a MTBF rating as specified in reference 2.5.

6.6 Clock Source

The module will derive its output clock from a nominally 1MHz signal available on Dataway connector line P2. This signal shall be a TTL level compatible clock signal with a nominal 60/40 duty cycle. The module shall impose a maximum of one standard TTL load on this line and shall use it as a source for its internal clock dividers. The module shall use the high to low transition of this signal as the active edge for the module clock divider circuits.

6.7 Input Signals

All front panel input signals, TRIG 1, DISABL, Clock Inhibit, and Trig Inhibit shall utilize an optoisolator such as HCPL 2601 or equivalent. The required circuit configuration is given in Figure 11.3. The module shall use the low to high transition (transition of optoisolator not conducting to conducting) as the active edge.

6.8 Output Signal Characteristics

6.8.1 Type: Differential signal

6.8.2 Amplitude (line to line):
5 volts maximum
4 volts minimum

6.8.3 Drive Capability: 100 ohm resistive load for rated amplitude, capable of withstanding a line to line or line to ground short indefinitely without sustaining damage

6.8.4 Clock Output Signal: Nominal square wave maximum asymmetry 60/40.

6.8.5 Pulse Output Signals: Positive pulse 1 microsecond +/- 10%

6.8.6 Rise and Fall Time: 50 nanoseconds maximum into a 100 ohm resistive load

6.8.7 Timing for pulse output signals is shown in Figures 11.5 and 11.6.

6.9 Available Frequencies

Each of the sixteen (16) domains shall have a clock frequency associated with it. The following frequencies shall be available:

500KHz
200KHz
100KHz
50KHz
20KHz
10KHz
5KHz
2KHz
1KHz
500Hz
200Hz
100Hz
50Hz
20Hz
10Hz

In addition, any domain may be assigned the frequency zero (0) which will cause a domain to exist with no output clock. When the zero clock is selected the count number of the domain has no significance and the domain must be terminated by a trigger signal.

6.10 Count Duration

Each of the sixteen (16) domains shall have a frequency duration data word associated with it. Each domain may be set up for a duration of from one to over 16 million (16,777,215, FFFFFF hex) clock counts. The time of the domain will, thus, be the commanded count multiplied by the commanded period.

In addition, the module shall be capable of responding to a count command of zero. The module will respond to a count of zero by causing the domain to exist continuously until triggered. Upon receipt of a trigger the module will advance to the next commanded domain.

6.11 Sequence Identifier

The module shall maintain a sequence identifier word for the purpose of controlling the number of different domains to be used for the desired sequence as well as the number of times the entire sequence is to be cycled. The sequence identifier word shall be loaded by CAMAC command. This word shall consist of a four (4) bit field to control the number of domains to be used, a four (4) bit field to control the number of times the sequence is to be cycled and a single "Recycle" bit that shall be set if continuous recycle is desired. It should be noted that the sequence consists of a quantity of domains that are each defined by frequency, duration, flag and recycle data. The quantity of domains desired controls different domains to be used. The total number of domains that will execute is dependent upon the number of different domains used and the number of times each domain recycles. When the "Recycle" bit is set then the four (4) bit field indicating the number of times the sequence is to be cycled shall be ignored and the sequence will continue to recycle until the module is disabled by CAMAC command or by a DISAB input pulse.

6.12 Operating Sequence

6.12.1 Set Up

After power up or after CAMAC signals Z or C, the module will be configured in the disabled mode with all domain data words (16 frequency and 16 duration) as well as the module sequence identifier word set to zero. Through CAMAC commands the sixteen domains may be set up by loading the desired frequency and duration for each desired domain. In addition, the sequence identifier must be loaded to define the desired length of the sequence (from 1 to 16 domains) as well as the desired recycle option. At the same time frequency data for each word is loaded the WFT (wait for trigger) bit, the AOT (advance on trigger) bit and the four bit quantity indicating domain recycle iterations shall also be loaded. When a frequency of zero (no output) is specified the WFT bit and the AOT bit must also be specified to achieve the desired mode of operation. The following table is given to delineate the module response to the WFT and AOT bits when zero frequency is specified.

WFT	AOT	RESULTING OPERATIONAL RESPONSE
0	0	Once entered the domain will continue indefinitely until terminated by CAMAC command.
0	1	The module will advance to the next domain upon receipt of the first trigger signal.
1	0	Once entered the domain will continue indefinitely until terminated by CAMAC command.
1	1	The module will advance to the next domain upon receipt of the second trigger signal. The first trigger will have no effect on the module clock output but will cause a DOM STRT pulse output.

6.12.2 Enable Module

The module shall be enabled by CAMAC command. Upon receipt of the enable command the module shall immediately enter the first domain. If the WFT bit of the first domain is set to 0 then the module will immediatly commence the clock output for the domain at the pre-set frequency. If the WFT bit of the domain is set to 1 then the module will not commence output until a trigger pulse is received.

6.12.3 Domain Sequencing

Upon entering a domain the module will immediately drive its output clock to the zero state (LEMO pin 2 low and pin 3 high) for a minimum time of one microsecond. In addition, the module will test the WFT bit for that domain to determine whether the module clock output should await a trigger signal. If the WFT bit is set to zero then the first active edge of the clock output shall occur between one and two microseconds from the time the domain is entered. If the WFT bit is set to one then the first active edge of the module clock output shall occur between one and two microseconds from the leading edge of a sensed trigger.

After a clock output for a domain is started the module shall begin a count of output clock edges. The accumulated count will be compared to the duration data for the domain to accommodate domain advance in response to the completion of the desired duration. When the required number of clock output periods is satisfied then the current domain shall be terminated. At the conclusion of the domain activity the module will either recycle the last domain, advance to the next domain, recycle to the first domain (sequence recycle) or stop all output and disable the module, as a function of the defined sequence.

The timing for domain transition in response to satisfying the required duration is given in Figure 11.5.

In addition to domain termination due to satisfying the required duration, the domain may be terminated in response to a received trigger input signal. The domain will terminate in the same way as indicated above if a trigger signal is received during an active domain if the AOT bit is set to one. The timing for domain transition in response to an AOT and trigger is given by Figure 11.6.

As the domain sequencing continues the module circuitry will compare the active domain to the last domain number as indicated by the sequence identifier. When the last domain is active, then upon satisfying the required number of domain recyles for the last domain the module will then either stop output and disable itself or recycle to the first domain. The determination of whether or not the recycle option is exercised shall be in response either to the "Recycle" bit (if set) or to satisfying the desired number sequence cycles as indicated by the sequence identifier word.

Time Base Module

6.13. CAMAC Commands.

6.13.1. Command #1 Read Frequency [F(0).A(n).(Data Returned)]

This command gates last commanded frequency and flag data for domain n (n = 0 to 15) onto the Dataway read lines. The data returned shall be formatted as follows:

R1-R4 Commanded Frequency

0 = No Output Clock
1 = 500KHz
2 = 200KHz
3 = 100KHz
4 = 50KHz
5 = 20KHz
6 = 10KHz
7 = 5KHz
8 = 2KHz
9 = 1KHz
10 = 500KHZ
11 = 200KHz
12 = 100KHz
13 = 50KHz
14 = 20KHz
15 = 10KHz

R5-R7 Always Zero

R8 Wait For Trigger (WFT) Bit

This bit is set to 1 if it is desired to have this domain await a trigger signal before starting its frequency output.

R9 Advance On Trigger (AOT) Bit

This bit is set to 1 whenever it is desired to have this domain respond to a trigger pulse or command for the purpose of terminating the domain and advancing to the next domain.

R10-R13 Domain Recycle Quantity

A binary quantity indicating the number of times the domain is set to recycle. A quantity of zero (0) will indicate no Recycle so that the domain will be set to cycle one (1) time. A quantity of fifteen (15 decimal F hexidecimal) will indicate fifteen recycles, thus, sixteen (16) domain cycles.

R14-R24 Always zero

The module will respond to this command and return Q=1 and X=1 during all modes of operation. It should be noted that when frequency zero is in use the module will require that the AOT bit be set if it is desired that the domain be terminated through use of a trigger pulse or CAMAC trigger command.

6.13.2 Command #2 Read Duration [F(1).A(n).(Data Returned)]

This command gates the last commanded duration (count) for domain n (n=0 to 15) onto the Dataway read lines. The data returned shall be formatted as follows:

R1-R24 A binary quantity indicating the number of clock periods (also clock pulses) for the requested domain. A value of all zeros shall be interpreted to mean that the domain shall exist indefinitely until a new trigger is received.

The module will respond to this command and return Q=1 and X=1 during all modes of operation.

6.13.3 Command #3 Read Module Status [F(3).A(0).(Data Returned)]

This command gates the module status data as well as the contents of the sequence identifier word onto the dataway read lines. The data returned shall be formatted as follows.

R1-R4 Sequence Length

This field shall be used to indicate the number of domains commanded to be used for the sequence. (Loaded by F(18).A(0)). The quantity returned shall be from 0 to 15 corresponding to sequence lengths of 1 to 16.

R5-R8 Sequence Recycle Quantity

This field shall be used to indicate the number of times the entire sequence of domains is to be recycled. A quantity of zero thus indicates one sequence cycle and quantity of fifteen thus indicates sixteen sequence cycles. This field will be ignored if the Continuous Recycle bit is set to one.

R9 Continuous Recycle

0 = Recycle quantity as indicated by R5-R8
1 = Recycle continuously

R10-R14 Current Domain

This field shall be used to indicate the domain currently in use (0 to 15, 16 to 31 not used). The number will indicate the domain number that was last entered. This field shall be set to zero whenever the module is in the disabled state.

R15 Domain Active

0 = Current domain not active

1 = Current domain active

This bit shall be set to zero whenever the module is disabled or whenever the current domain has its WFT flag set and has not yet been triggered.

R16 Enabled

This bit shall be set to one whenever the module is enabled and set to zero whenever the module is disabled either by virtue of completing the commanded sequence or by virtue of response to CAMAC command or to a DISAB input pulse signal.

R17-R24 Always Zero

The module will respond to this command and return Q=1 and X=1 during all modes of operation.

6.13.4 Command #4 Read Module Number
[F(6).A(0).A(Data Returned)]

This command gates the module identification number (decimal 904, hexadecimal 388) onto the dataway read lines R1 through R12 with the LSB on line R1. The data returned shall be formatted as follows:

R1-R12 Module ID

A binary equivalent to the module identification number hexadecimal 388.

R13-R24 Always Zero

The module will respond to this command and return Q=1 and X=1 during all modes of operation.

6.13.5 Command #5 Load Frequency [F(16).A(n).D(XXXXXX)]

This command utilizes the CAMAC write lines to load the desired frequency and flag status into the module for domain n (n=0 to 15). The utilization of CAMAC write lines shall correspond to the utilization of the CAMAC read lines for Command #1.

The module will respond to this command and return Q=1, X=1 during all modes of operation. It should be noted that this command will always update the data in the module domain memory but it will not effect a domain that is active at the time of receipt of the command. The next activation of the domain, however, will use the latest data.

When frequency zero (no output) is selected for this domain (Command #5) then the duration loaded by this command has no significance.

6.13.6 Command #6 Load Duration [F(17).A(n).D(XXXXXX)]

This command utilizes the CAMAC write lines to load the desired duration (also clock count) for domain n (n=0 to 15). The utilization of the CAMAC write lines shall correspond to the utilization of the CAMAC read lines for Command #2.

The module will respond to this command and return Q=1 and X=1 during all modes of operation. When the command is issued to a module while the module is active its effect will be the same as is Command #4 (i.e., active domain completes as started). When duration zero is commanded the module will remain in the domain indefinitely until a trigger signal is received. The duration field for a domain loaded for zero frequency will have no significance and will be ignored by the module circuitry.

6.13.7 Command #7 Load Sequence Identifier [F(18).A(0).D(XXXXXX)]

This command utilizes the CAMAC write lines to load into the module the number of domains desired to be used during the commanded sequence as well as whether the recycle option is desired. The Dataway write lines shall be utilized as follows:

W1-W4 A quantity from 0 to 15 coresponding to a desired domain count of 1 to 16.

W5-W8 Sequence Recycle Quantity

This field shall be used to control the number of times the entire sequence of domains is to be recycled as described in Section 6.13.3.

W9 Continuous Recycle

0 = Recycle as set by W5-W8. Terminate and disable module after last domain.

1 = Recycle continuously and ignore bits W5-W8.

W10-W24 Not Used

The module will respond to this command and return Q=1 and X=1 if the command is received while the module is disabled. The module will ignore this command and return Q=0 and X=1 if the command is received while the module is enabled.

6.13.8 Command #8 Disable Module [F(24).A(0)]

This command shall be used to disable the module and inhibit the module from responding to any trigger signals. In addition, if this command is received while the module is active the output pulse train will be stopped and the clock output set to zero volts. Operational parameters stored within the module shall not be affected by this command so that the module may be simply re-Enabled to start a new and identical output sequence.

The module will respond to this command and return Q=1 and X=1 during all modes of operation.

6.13.9 Command #9 Trigger Module [F(25).A(0)]

This command causes a trigger single to be generated internally to the module circuitry. The module will respond to this command in the same way as it would respond to an incoming trigger from its front panel connectors.

The module will respond to this command and return Q=1 and X=1 during all modes of operation.

6.13.10 Command #10 Enable Module [F(26).A(0)]

This command shall be used to enable the module to start output, as defined for the first domain, subject to the status of the first domain WFT bit. If this command is received while the module is active then the active domain will be terminated and the first domain entered.

This command is required prior to the start of an output sequence. The sequence data (domain data and sequence identifier) that will determine the characteristics of the sequence will be the data most recently loaded. In applications where the same sequence is desired for consecutive operations then this is the only command needed between output sequences.

The module will respond to this command and return Q=1 and X=1 during all modes of operation.

6.13.11 Dataway Responses Q and X

The module will return X=1 for all addressed commands that are recognized as commands the module is equipped to respond to. It will return Q=0 or 1 conditionally as defined for commands 1 through 10. It will return Q=0 and X=0 for any other addressed command.

6.13.12 Initialize, Clear or Power Up.

The module will respond to either of these signals by clearing all internal registers and/or memories and place the module in a disabled state with all outputs set to zero.

6.14 Front Panel Indicators

The module shall provide seven (7) LED indicators mounted for visibility from the front panel. The indicators shall function as follows:

LED #1	"N" shall illuminate for approximately 100 milliseconds whenever N is received.
LED #2	"ENAB" shall illuminate whenever the module is enabled.
LED #3	"ACT" shall illuminate whenever the current domain is active as defined by 6.13.3 Read Status command.
LED #4	"TRIG" shall illuminate for approximately 100 milliseconds whenever a trigger signal is received (Dataway or front panel).
LED #5 through LED #8	Shall illuminate the binary equivalent to the currently active domain.

7.0 Environmental Data

7.1 The module must operate, as defined, over an ambient temperature range of 0 to +50oC.

7.2 The module must operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must operate, as defined, in the presence of an external magnetic field changing at a maximum rate of 200 gauss per second with a peak magnitude of 100 gauss in any direction.

7.4 The module must operate, as defined, in a radiation environment as follows:

Neutrons:	2 x 10 7 N/CM2/sec
Rad-Dose:	5 x 10 -2 rad (Si)/sec
Integrated Dose:	200 rad (Si)

8.0 Safety

All components of this module must be of flame retardant material.

9.0 Testing

All modules shall be subjected to a temperature cycling period followed by a functional test prior to shipment equivalent to tests delineated in reference 2.5. A description of all tests to be performed shall be submitted by the bidder for incorporation into this specification.

10.0 Reliability and Quality Control

The module shall meet all applicable requirements specified in reference 2.5.

3 Pin LEMO Key Location Toward Top

Suggested Front Panel Layout

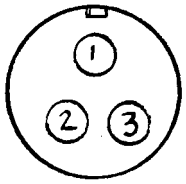
Figure 11.1

LEMO Type RG0B303 CA22

PIN	TYPE	USE
1	female	*
2	female	signal high
3	female	signal low

Alignment Key

View from solder cup (or crimp) side



Typical Connector Circuitry

* Chassis ground for Trigger Output, Clock Output, Domain Start, and EOS. A .01 microfarad capacitor to ground available for others by installing jumpers on the printed circuit board. The modules are initially manufactured and delivered without the jumpers installed.

FRONT PANEL CONNECTOR

PIN ASSIGNMENT

FIGURE 11.2

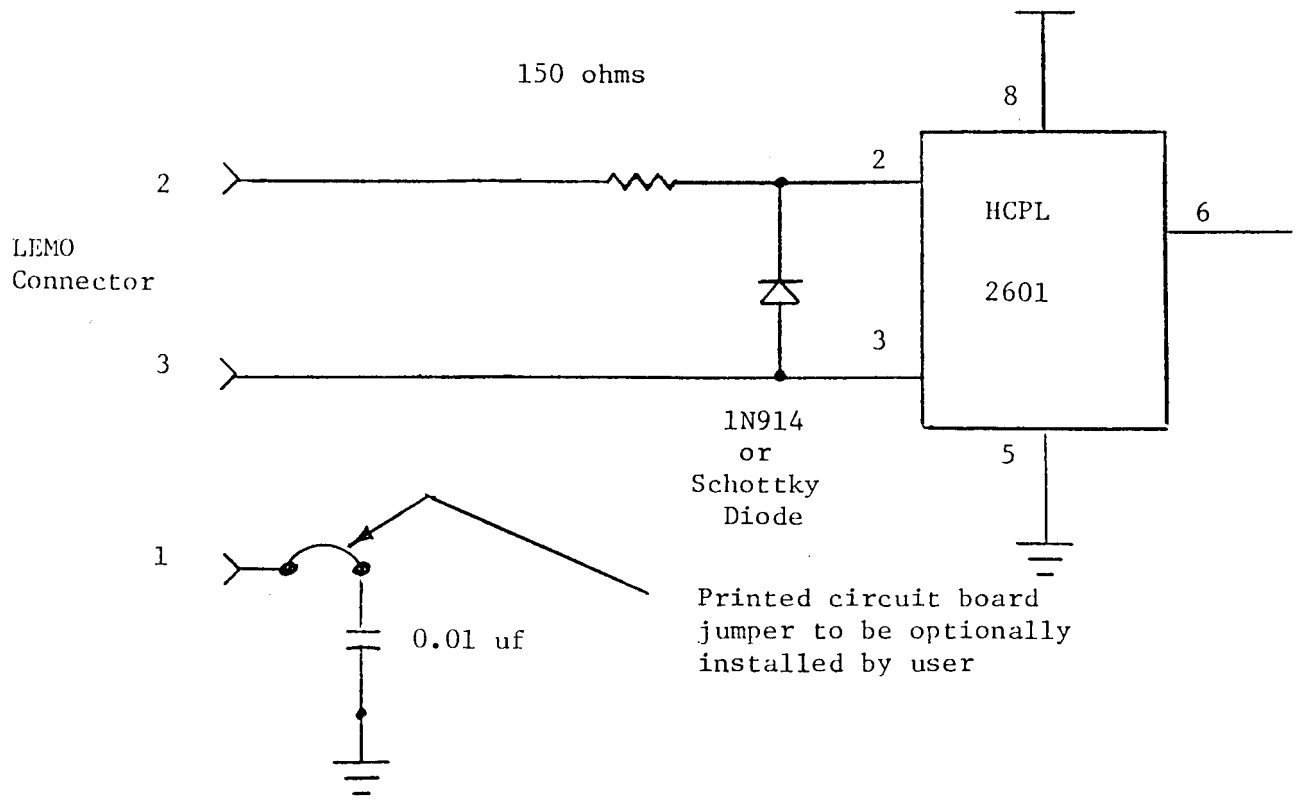


Figure 11.3

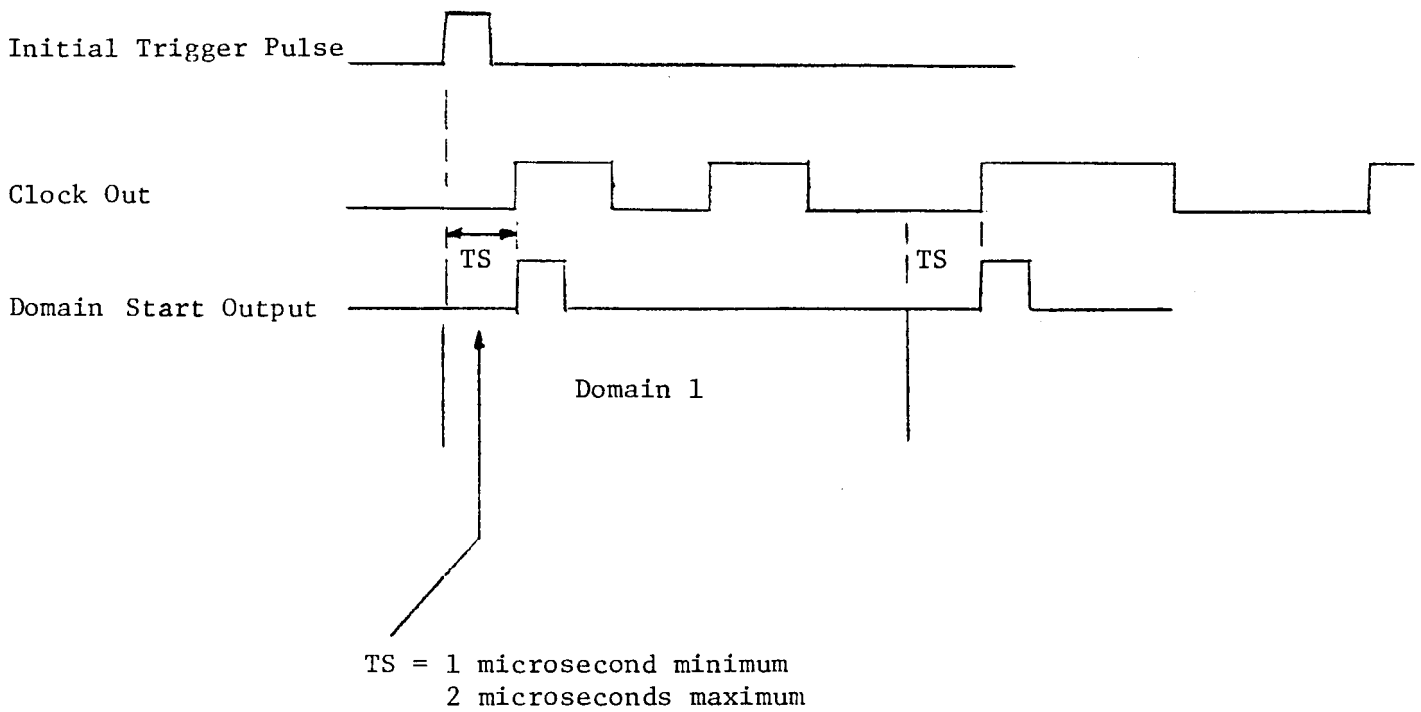
Typical Trigger and Clock Input Circuit

AUXILIARY CONNECTOR

PIN ASSIGNMENT

COMPONENT SIDE		SOLDER SIDE	
PIN	USE	PIN	USE
1B	Clock Output High	1A	Clock Output Low
2B	GND	2A	GND
3B	Clock Enable High	3A	Clock Enable Low
4B	GND	4A	GND
5B	Trigger 1 High	5A	Trigger 1 Low
6B	GND	6A	GND
7B	Disable module high	7A	Disable mod. Low
8B	GND	8A	GND
9B	Trigger Enable High	9A	Trigger Enable Low
10B	GND	10A	GND
11B	Trigger Output High	11A	Trigger Output Low
12B	GND	12A	GND
13B	Domain Start High	13A	Domain Start Low
14B	GND	14A	GND
15B	End of Sequence High	15A	End of Sequence Low

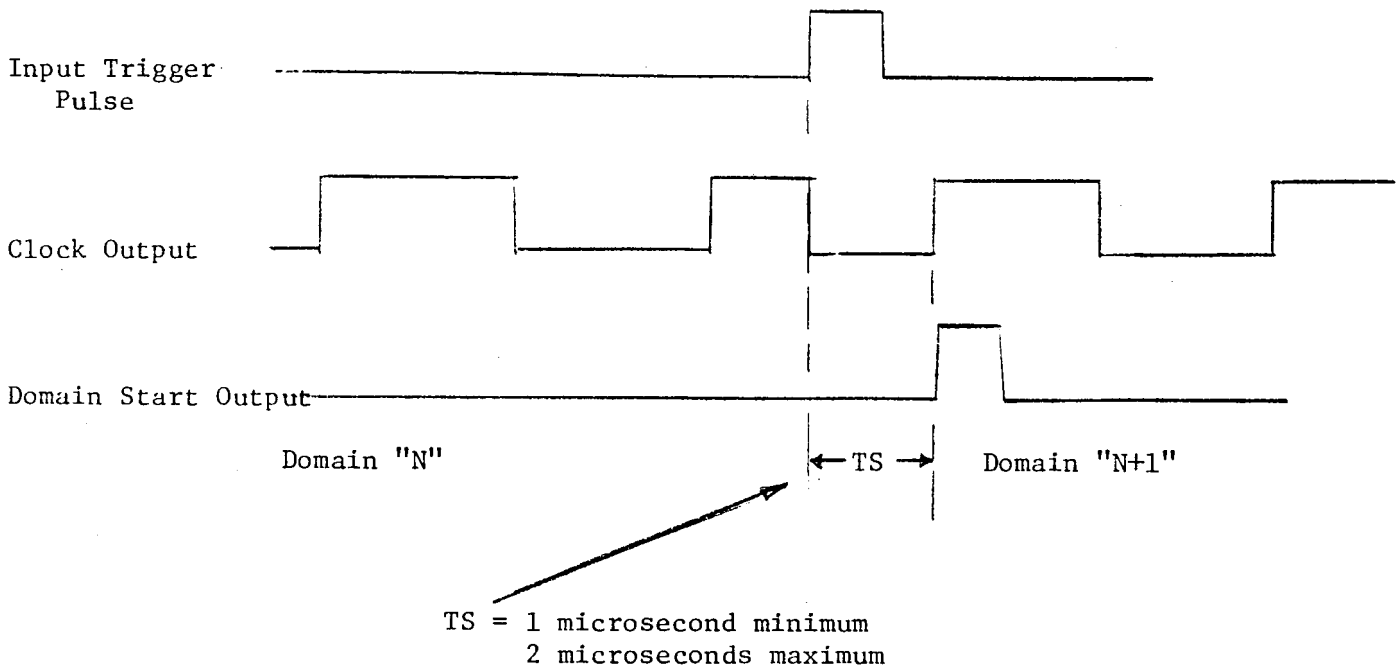
FIGURE 11.4



Example of domain advance caused by completing the required number of output clock periods.

Domain 1 set for 2 periods.

Figure 11.5



Example of domain advance in response to an asynchronous trigger. Note that the clock output is driven low for from 1 to 2 microseconds. The 1 microsecond uncertainty is to resynchronize the divider circuits to the source clock and Dataway line P2.

Figure 11.6