Power Supply Real Time Controller

PSRTC

Operations Guide

Rev. 2

4/4/5

1.0 Introduction

The purpose of the NSTX Power Supply Real Time Controller (PSRTC) is to provide a means for real time control of the AC/DC converter system which supplies controlled DC power to the NSTX magnet systems.

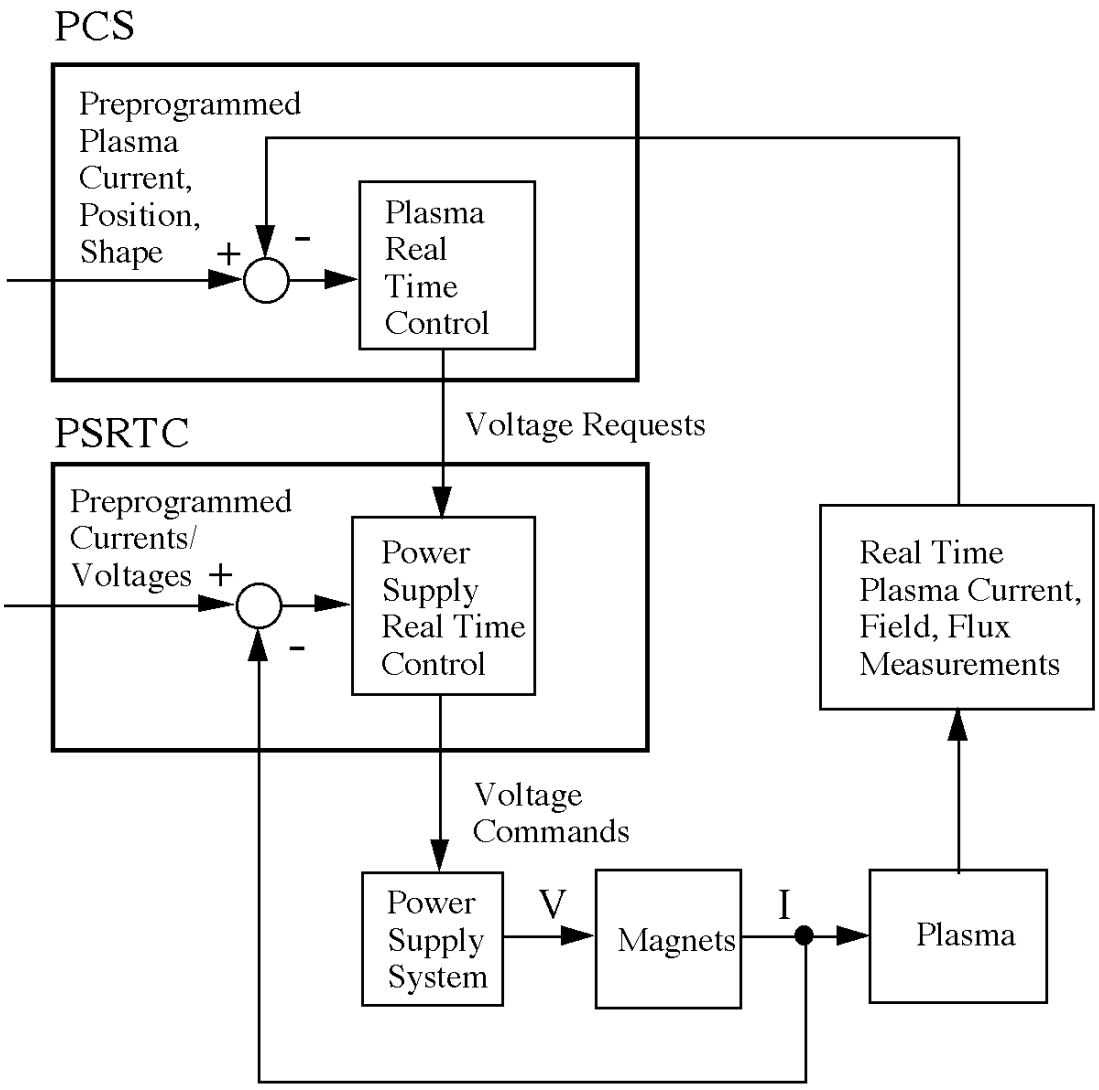


Figure 1: Conceptual Block Diagram of Control System

The PSRTC supports two modes of operation:

- "Test" Mode

  - All NSTX circuits are driven by the PSRTC in closed loop current control or open loop voltage control, unless locked out, in a fully stand-alone fashion

- "Operations" Mode

  - One or more circuits are driven by the Plasma Control System (PCS), via real time voltage commands to the PSRTC, during a specified time interval during a pulse, with full control by the PSRTC outside that interval

  - Other circuits are driven by the PSRTC in closed loop current control or open loop voltage control, unless locked out, in a fully stand-alone fashion

  - PSRTC (or PCS) performs closed loop current control to initiate the TF coil current, precharge the OH coil, and pre-bias other PF coils

  - at the start of a pre-programmed time window, the PCS initiates the plasma and controls plasma current, position, shape, etc. via voltage requests to the PSRTC

  - Upon termination of the plasma current the PSRTC (or PCS) extinguishes the current in all coil systems according to pre-programmed current derivatives.

2.0 System to be Controlled

2.1 Power Supplies

NSTX utilizes the PPPL "Power Supply" (PS) facility originally built for the Tokamak Fusion Test Reactor (TFTR) project, consisting of thirty-nine (39) modular 12-pulse phase controlled thyristor rectifiers.

• Each PS consists of two 6-pulse "Power Supply Sections" (PSS) which are electrically isolated from each other but subject to the same "Firing Generator" (FG).

• Each PSS is equipped with a full rated bypass module which can carry the load current when the rectifiers are suppressed.

• Each PSS is rated to produce a maximum average DC output voltage of 1012.85VDC (≈1kV), no load, with 13.8kV AC input voltage applied to the converter transformer primary.

• Nominal pulse current rating of each PSS is 24kA-6sec/300sec.

• The FG of each PS controls, in effect, the voltage produced by its two PSS by phase controlling the thyristor firing pulses in accordance with a Control Word received as an input from the PSRTC. The Control Word is an 11 bit digital command.

Power Supply Control Word

Bits 1 through 8:

Firing angle, a.k.a. "alpha" command, 0 = 0^{o}, 255 = 165^{o}

Bit 9:

"Convert" command, 1= rectifier thyristors gated, a.k.a. "fired",
0 = rectifier thyristors gate blocked, a.k.a. "suppressed"

Bit 10:

Unused

Bit 11:

"Block Bypass" command, 1 = bypass thyristors gate blocked,
0 = bypass thyristors gated

2.2 Switching Power Amplifiers

The Resistive Wall Mode (RWM) coils are powered by switching power amplifiers (SPAs). These are 4-quadrant choppers which can switch a DC source capacitor bank on to the terminals of the RWM coils in a pulse width modulation (PWM) fashion.

The SPAs are controlled by a +/- 10V signal generated in the PSRTC which corresponds to the PWM duty cycle +/-100%.

The DC source capacitor bank is charged by a Transrex power supply called P13. The charging voltage is set by a parameter in the PSRTC input data file VP13SPA which can be up to 1012.85 volts (the max available Transrex output voltage).

There are three SPA sub-units each rated 1kV/3.333kA-6seconds, once every 300 seconds.

2.3 Circuits

Circuit types to be controlled are as depicted in Figure 2, where the boxed thyristor symbol represents one or more PSS connected in series/parallel combination. The lines connecting the circles represent removable bus links.

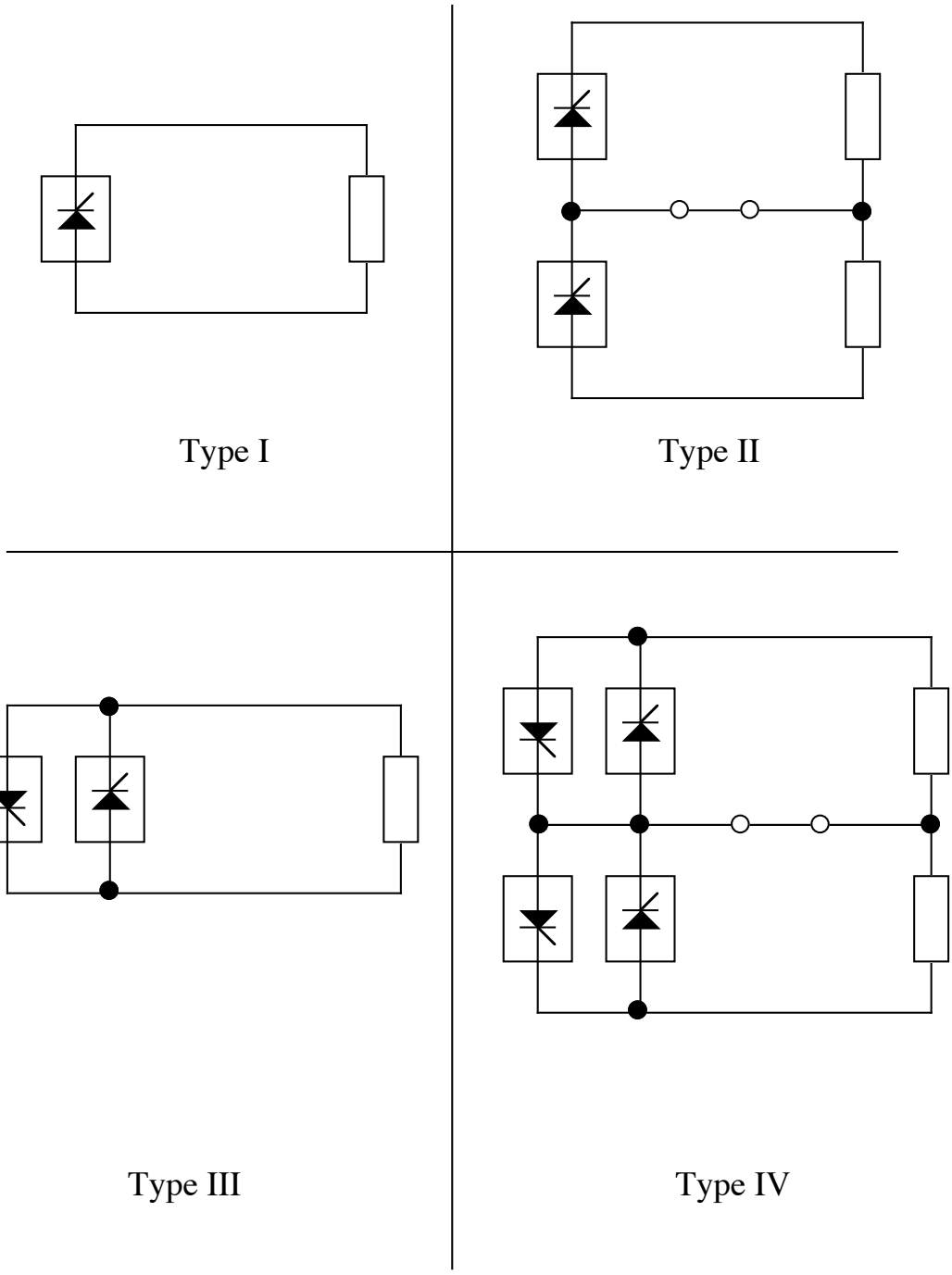


Figure 2: NSTX Circuit Configurations

a. Type I is a "Unipolar", "2-Wire" circuit. Current flows in one direction through one load coil group.

b. Type II is a "Unipolar", "3-Wire" circuit. Current flows in one direction through two load coil groups; the magnitude of the current may be different in the two "twin" load coil groups.

c. Type III is a "Bipolar", "2-Wire" circuit. Current flows in either direction through one load coil group.

d. Type IV is a "Bipolar", "3-Wire" circuit. Current flows in either direction through two load coil groups; the magnitude and polarity of the current may be different in the two "twin" load coil groups.

e. Type V is the RWM-style circuit consisting of a 4-quadrant chopper as depicted in figure 3.

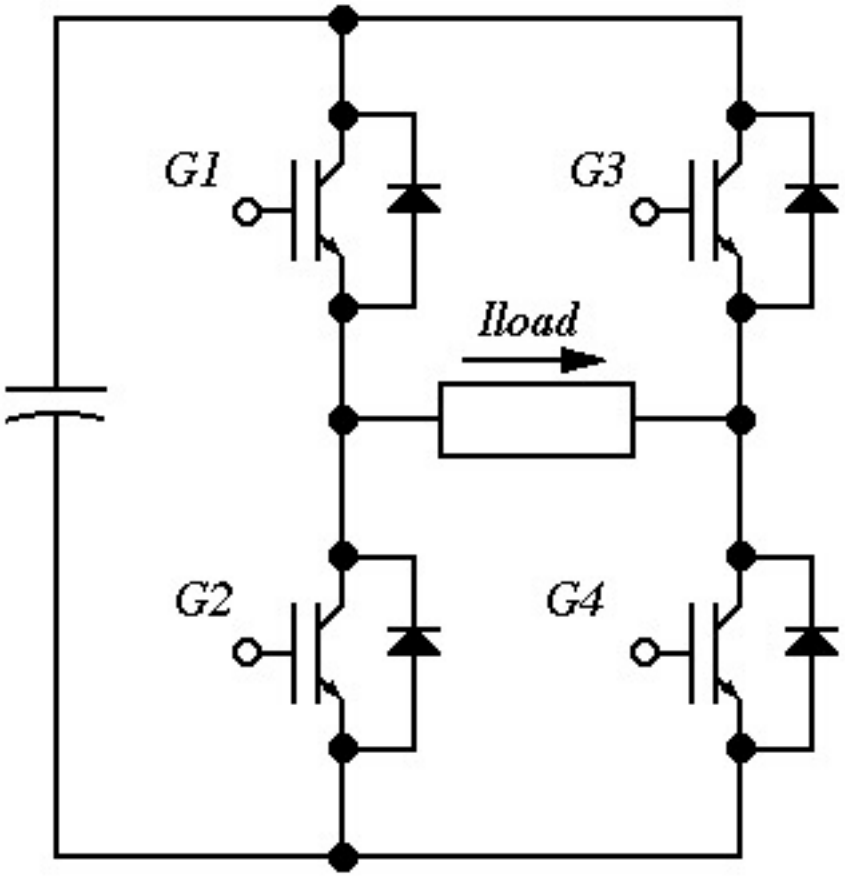


Figure 3: RWM Circuit Configuration

A listing of the NSTX circuits along with type, number of DC poles, number of PSS, and V/I rating is given in Table 1.

Table 1: NSTX Circuit Types, Poles, PSS, and Ratings

Circuit	Type	DC Poles	Series/ Parallel PSS	Volts (+/-kV)	Peak Amps (kA)	ESW@ Peak Amps (sec)
TF	I	2	1/4	1	35.6	5.3
OH	III	2	6/2	6	+/-24	0.525
PF1a Upper	IV	3	2/2	2	-5/+15	5
PF1a Lower			2/2	2	-5/+15	5
PF1b	I	2	2/1	2	20	1
PF2 Upper	II	3	2/1	2	20	5
PF2 Lower			2/1	2	20	5
PF3 Upper	IV	3	2/1	2	-5/+20	5
PF3 Lower			2/1	2	-5/+20	5
PF4	I	2	2/1	2	20	5
PF5	I	2	3/1	3	20	5
CHI	I	2	2/2	2	50	0.8
RWM1	V	2	2	1	3.333	6
RWM2	V	2		1	3.333	6
RWM3	V	2		1	3.333	6
Total	15 ckt	27 pole	45 PSS			

• Layout of the PF coils is given in Figure 4. Typical test shot waveforms, which set the envelope for coil currents during plasma operation, are given in Figure 5. All current and field directions are defined to be (+) when Clockwise (CW) viewed from above. For nominal plasma current direction (CCW)...

- initial Ioh is (-)

- initial PF1A is (+), then swings (-) while Ip is present to increase triangularity

- PF1B (-) for CHI X-point formation

- PF2 usually (-) to increase plasma elongation

- initial PF3 is (-) to cancel OH stray fields at R_o as required to produce field null for plasma initiation, but later (+) to provide vertical field for radial position control, difference between PF3U and PF3L provides radial field for vertical position control

- PF4 not typically used

- PF5 (+) to provide vertical field for equilibrium in radial position, and to assist PF3 in creating initial field null at R_o

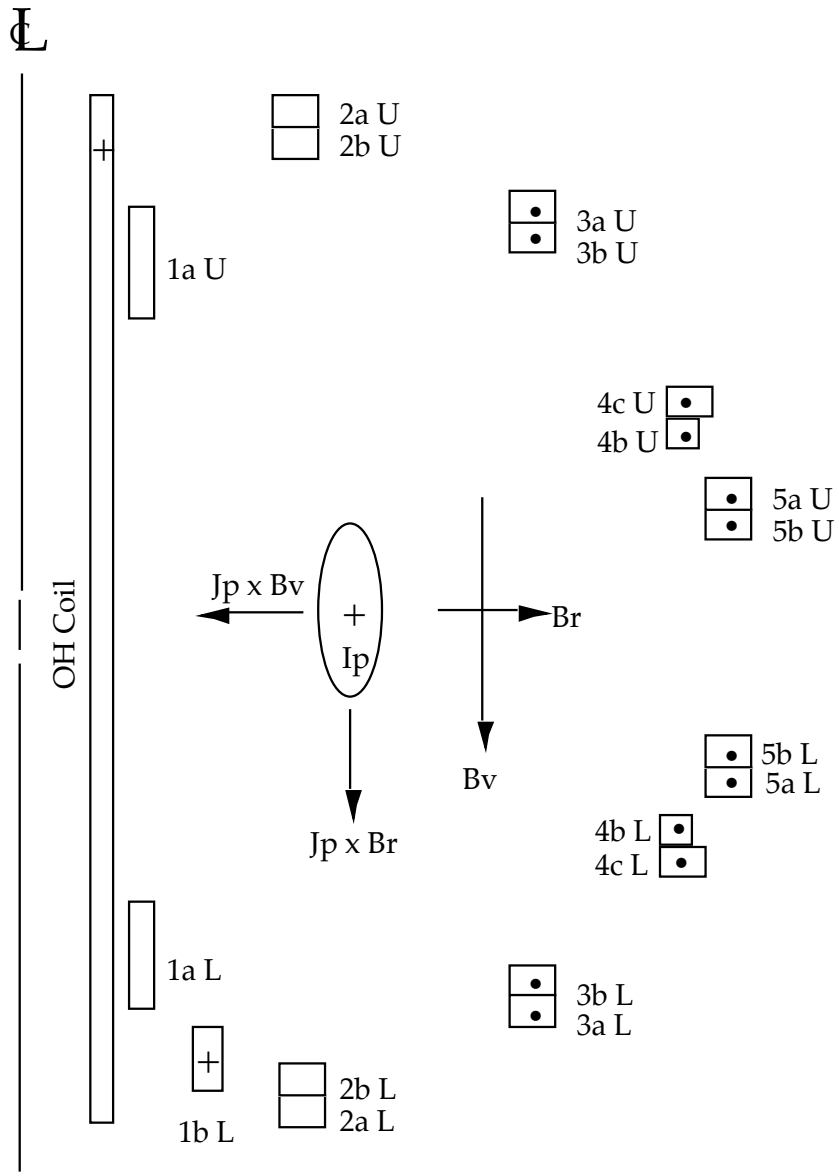


Figure 5: PF Coil Utilization

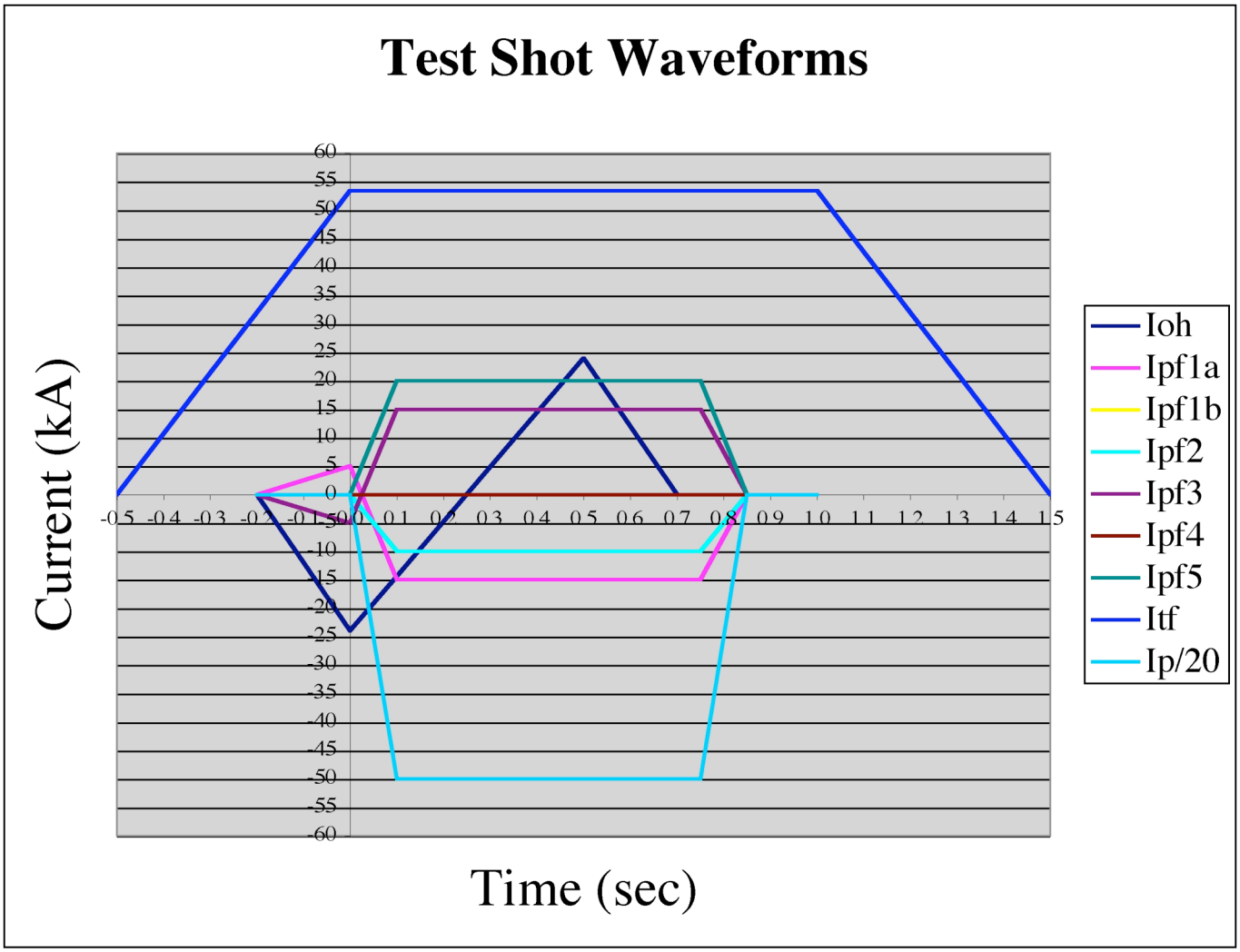


Figure 6: Test Shot Waveforms

• A listing of the Power Supplies connected in the circuits is given in Table 2. In the NSTX naming, the x in "xS" refers to the series connection sequence where x=1 corresponds to the power supply section into which current first enters, and the y in "yP" refers to the parallel number. For anti-parallel circuits, "1P" is the (+) branch, and "2P" is the (-) branch.

Table 2: PSS Utilization

Ckt.#	Coil	NSTX Name	TFTR Name
P1	TF	TF-PSS-1S-1P	ETF1-PSS-1A
		TF-PSS-1S-2P	ETF1-PSS-1B
	TF Spare	TF-PSS-2S-1P	ETF1-PSS-3A
		TF-PSS-2S-2P	ETF1-PSS-3B
P1	TF	TF-PSS-1S-3P	ETF1-PSS-2A
		TF-PSS-1S-4P	ETF1-PSS-2B
P1	TF Spare	TF-PSS-2S-3P	ETF1-PSS-4A
		TF-PSS-2S-4P	ETF1-PSS-4B
		TF-PSS-3S-1P	ETF1-PSS-5B
		TF-PSS-3S-2P	ETF1-PSS-5A
		TF-PSS-4S-1P	ETF1-PSS-7B
		TF-PSS-4S-2P	ETF1-PSS-7A
		TF-PSS-5S-1P	ETF1-PSS-9B
		TF-PSS-5S-2P	ETF1-PSS-9A
		TF-PSS-3S-3P	ETF1-PSS-6B
		TF-PSS-3S-4P	ETF1-PSS-6A
		TF-PSS-4S-3P	ETF1-PSS-8B
		TF-PSS-4S-4P	ETF1-PSS-8A
		TF-PSS-5S-3P	ETF1-PSS-AB
		TF-PSS-5S-4P	ETF1-PSS-AA
P2	OH	OH-PSS-1S-1P	ETF2-PSS-7B
		OH-PSS-2S-1P	ETF2-PSS-7A
		OH-PSS-3S-1P	ETF2-PSS-5B
		OH-PSS-4S-1P	ETF2-PSS-5A
		OH-PSS-8S-2P	ETF2-PSS-2A
		OH-PSS-7S-2P	ETF2-PSS-2B
		OH-PSS-6S-2P	ETF2-PSS-4A
		OH-PSS-5S-2P	ETF2-PSS-4B
		OH-PSS-5S-1P	ETF2-PSS-3B
		OH-PSS-6S-1P	ETF2-PSS-3A
		OH-PSS-7S-1P	ETF2-PSS-1B
		OH-PSS-8S-1P	ETF2-PSS-1A
		OH-PSS-4S-2P	ETF2-PSS-6A
		OH-PSS-3S-2P	ETF2-PSS-6B
		OH-PSS-2S-2P	ETF2-PSS-8A
		OH-PSS-1S-2P	ETF2-PSS-8B
		SPARE	ETF2-PSS-9A

		SPARE	ETF2-PSS-9B
		SPARE	ETF2-PSS-AA
		SPARE	ETF2-PSS-AB
P3	PF1aU	PF1AU-PSS-1S-1P	EEF4-PSS-2B
		PF1AU-PSS-2S-1P	EEF4-PSS-2A
		PF1AU-PSS-1S-2P	EOH3-PSS-2B
		PF1AU-PSS-2S-2P	EOH3-PSS-2A
P4	PF1aL	PF1AL-PSS-1S-1P	EEF3-PSS-1B
		PF1AL-PSS-2S-1P	EEF3-PSS-1A
		PF1AL-PSS-1S-2P	EEF3-PSS-2B
		PF1AL-PSS-2S-2P	EEF3-PSS-2A
P5	PF1b	PF1B-PSS-1S	EEF4-PSS-1B
		PF1B-PSS-2S	EEF4-PSS-1A
P6	PF2U	PF2U-PSS-1S	EOH5-PSS-1B
		PF2U-PSS-2S	EOH5-PSS-1A
P7	PF2L	PF2L-PSS-1S	EOH3-PSS-1B
		PF2L-PSS-2S	EOH3-PSS-1A
P8	PF3U	PF3U-PSS-1S-1P	EOH2-PSS-1B
		PF3U-PSS-2S-1P	EOH2-PSS-1A
		PF3U-PSS-1S-2P	EEF1-PSS-1B
		PF3U-PSS-2S-2P	EEF1-PSS-1A
P9	PF3L	PF3L-PSS-1S-1P	EOH4-PSS-1B
		PF3L-PSS-2S-1P	EOH4-PSS-1A
		PF3L-PSS-1S-2P	EEF1-PSS-2B
		PF3L-PSS-2S-2P	EEF1-PSS-2A
P10	PF5	PF5-PSS-1S	EOH6-PSS-1B
		PF5-PSS-3S	EOH6-PSS-1A
		PF5-PSS-2S	EOH5-PSS-2B
P11	CHI	CHI-PSS-1S-1P	EOH1-PSS-1B
		CHI-PSS-1S-2P	EOH1-PSS-2B
		CHI-PSS-2S-1P	EOH1-PSS-2A
		CHI-PSS-2S-2P	EOH1-PSS-1A
P12	PF4	PF4-PSS-1S	EEF2-PSS-1B
		PF4-PSS-2S	EEF2-PSS-1A
P13	RWM	P13-PSS-1S	EEF2-PSS-2B
		P13-PSS-2S	EEF2-PSS-2A

It is noted that:

- a total of 20 PS Groups are explicitly controlled

- The voltage applied to, or the current produced in, each of the circuits must be explicitly controlled. Therefore, eleven (15) separate circuit control loops are required.

- However, if the bus links are not installed in the Type II and Type IV circuits, then they reduce to Type I and Type III, respectively. In this case, either the U or L part shall be locked out in the control data file and the remaining part used to control the circuit.

e.g. if no link in midpoint of PF1AU and PF1AL, lock out PF1AL and refer all control to PF1AU

3.0 PSRTC Control Algorithms

3.1 Power Supply Control Function

The Power Supply Control Function is depicted in Figure 7.

- The same basic function is applied to all of the circuits via "do loops". A minor difference is that the final output to the thyristor rectifiers is the firing angle (α), whereas the final output to the SPAs is the PWM duty factor (d).

• The output of the control function consists of the firing angle (α) or duty factor (d) and convert bit commands which are delivered to the PS in the form of the PS Control Words. Since these commands are related to the voltage they are, essentially, voltage commands.

• The voltage commands are derived either from closed loop proportional - integral (PI) current control against a programmable reference, or from a direct voltage request.

• The direct voltage request is obtained from either a programmable reference, or a signal supplied in real time by the PRTC.

• When in the voltage control mode, a current clamp feature is applied if the current approaches a programmable limit. Additional features include rate limiting, and control of anti-parallel rectifiers, including the required α limiting.

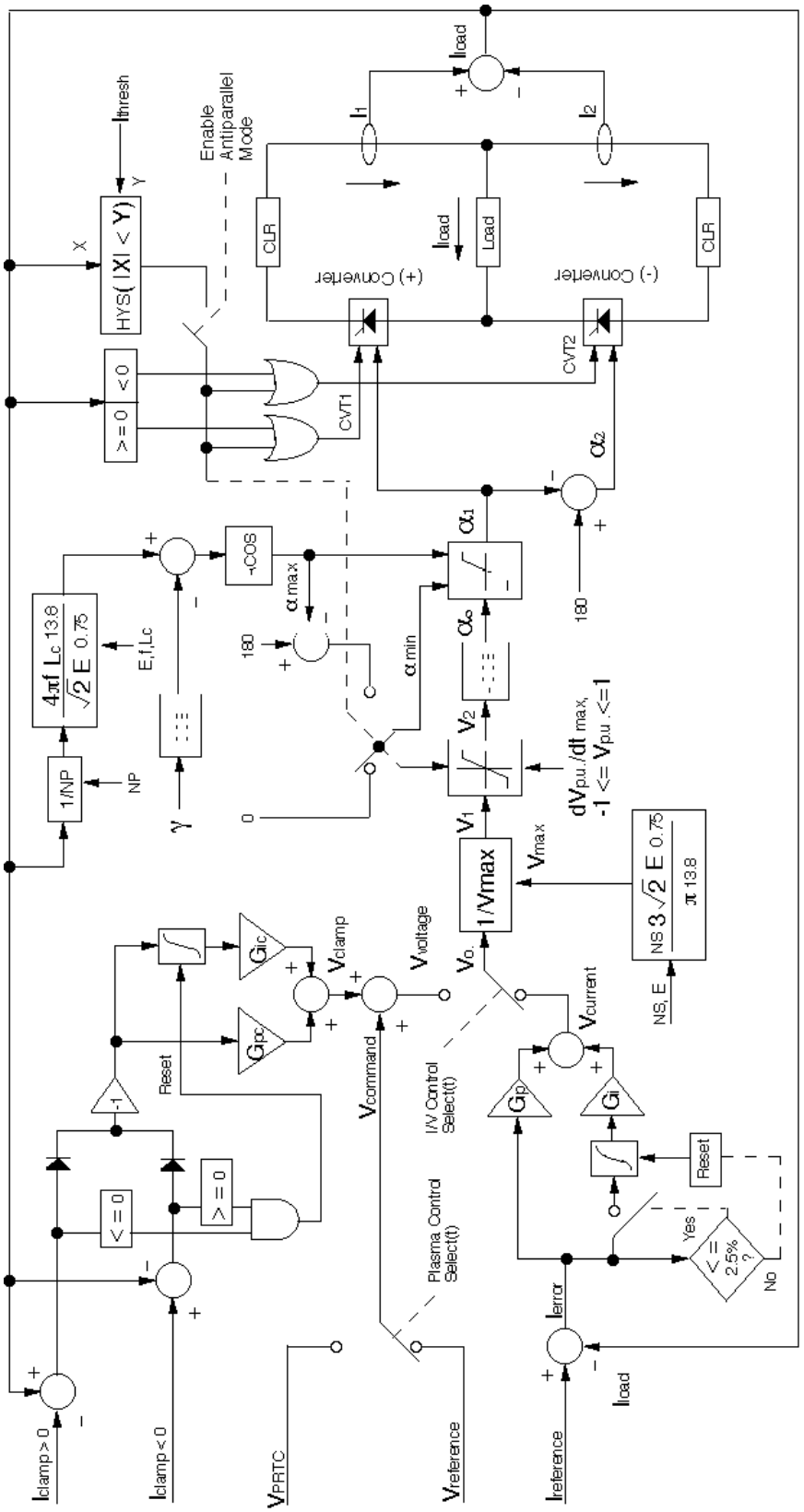


Figure 7: Power Supply Control Function

3.1.1 Closed Loop Current Control

• I_{load} is subtracted from pre-programmed $I_{reference}$. The difference is the error I_{error}.

• I_{error} is multiplied by proportional gain G_p, and is integrated and multiplied by integral gain G_i. The sum of these two terms is the voltage requested by current control $V_{current}$.

• Integral term is only applied when $|I_{error}|$ falls below 2.5% of the reference and is reset each time $|I_{error}|$ exceeds 2.5%

3.1.2 Voltage Control & Current Clamp

• $V_{command}$ can be either the programmable reference $V_{reference}$ or a real time signal provided by the PRTC (V_{PRTC}).

• Time window for V_{PRTC} is set by preprogrammed plasma start and end times.

• Two types of current clamping are imposed when in voltage control mode.

1) The first type is based on PI control which generates a voltage V_{clamp} whenever the load current I_{load} passes outside input values $I_{clamp}>0$ and $I_{clamp}<0$

a. When the current returns to the allowable range the clamp integrator is reset

b. The net voltage request based on voltage control $V_{voltage}$ is the result of the addition of $V_{command}$ and V_{clamp}

2) The second type takes effect when the load current comes within ~2% of the circuit overcurrent setting. In this case a voltage limit $V0_{max}$ is calculated each time step such that the current after the next time step I^{i+1} can reach no more than 98% or the overcurrent setting, based on $0.98*I_{oc}= I^{i}*\exp(-dt/tau)+ V0_{max}/R*(1-\exp(-dt/tau))$

3.1.3 Voltage to Alpha Conversion

• selection of the source of the voltage request V_0 from either voltage control $V_{voltage}$ or current control $V_{current}$ is a function of time.

• V_1 is the per unit version of V_0 based on $V_1=V_0/V_{max}$, where V_{max} is the maximum no-load voltage available for the circuit in question. V_{max} is based on the programmable number of series PSS (NS), and the primary side AC rms line-to-line source voltage E (nominally 13.8kV at D-site).

• V_2 is a rate and magnitude limited version of V_1, where the rate limit is programmable for each circuit and the magnitude limit is -1 to 1 per unit. The rate limit is only applied when the antiparallel mode is in effect (see next section).

• α_0 is the firing angle request, and α_1 is the firing angle after limiting. If antiparallel operation is not in effect, then the allowable range of α_1 is 0 to α_{max} , where α_{max} is the maximum permissible delay angle. It is calculated based on the load current per PSS, equal to I_{load}/NP where NP is the number of parallel PSS branches in the circuit being controlled, the AC source frequency ω, the commutating inductance L_c, and the AC source voltage E, along with a programmable inversion margin angle γ.

• If antiparallel operation is in effect, then the minimum permissible delay angle α_{min} is set equal to 180 - α_{max} , so that the allowable range of alpha is therefore $\alpha_{min} \leq \alpha_1 \leq \alpha_{max}$ in the antiparallel mode.

• In the case of the RWM/SPA circuits, α_1 is set directly equal to V_2 which is equivalent to the PWM duty cycle "d". Furthermore, the RWM1 α_2 storage location is used for the SPA DC source P13 firing angle, and RWM1 ncvt2 for the convert bit.

3.1.4 Antiparallel Operation

• permits bipolar current flow in the load without delay around current zero

• antiparallel converters (a.k.a. the (#1) and (#2) converters) must be operated at symmetric (about 90 degrees) delay angles α_{min} and α_{max}, i.e.

$$\alpha_2 = 180 - \alpha_1$$

• this is required to minimize the circulating current which is impeded only by the Current Limiting Reactors (CLRs).

• the antiparallel mode is declared when the magnitude of the load current I_{load} falls below a threshold I_{thresh}

• conditioned by a hysteresis function which only declares the mode to be true if the previous magnitude exceeded the threshold

• switch is provided to enable/disable antiparallel operation for each circuit.

4.0 Load Current Measurements

• PSS branch currents are measured by two types of DC current transducers

- Halmar "zero flux" type

- high accuracy (0.1%) if well calibrated and installed
- excellent frequency response

- Shunt "leaf" type

- Simple and reliable
- good accuracy (0.5%)
- moderate frequency response

• Redundant measurements are (ideally) provided in each branch

- except PF1A and PF3, which are lacking a complete set of branch currents

- via control input data, PF1A and PF3 the total current is substituted for the branch current with scaling factor reduced by 1/2

- in some cases (low inductance circuits) it has been found necessary to drop the shunt measurement due to amplification of power supply ripple (L_{shunt} * dI_{load}/dt, and consequential control loop response), and substitute the Halmar (loss of redundancy)

• RWM currents are measured by tranducers built into the SPA units

• Signal processing (buffer and fan out) by "Halmar Signal Conditioner" (HSC)

• Interface with control computer via "Data Acquisition System" (DAS)

• Interface with EPICs (and MDS+) via CAMAC digitizers

• List of DCCT signals is given in Table 4

Table 4: Current Measurements

Imeas	Ckt/Sys	kA	D-site Identifier	SKY Ch.	Dig.	Comment
1	OH (+) Branch	25	ETF2-MN1-MH1-I	5	pc_oh_br_1_cur_1	
2	OH (-) Branch	25	ETF2-MN3-MH1-I	6	pc_oh_br_2_cur_1	
3	PF1a Upper (+) Branch	25	PF1AU-CTD-MH1	8	pc_pf1au_cur_1	∑Current substituting for PSRTC branch current
4	PF1a Upper (-) Branch	na	na	na	na	
5	PF1a Lower (+) Branch	50	EFVC-MN2-MH1-I	7	pc_pf1al_cur_1	∑Current substituting for PSRTC branch current
6	PF1a Lower (-) Branch	na	na	na	na	
7	PF1b	25	EEF1-MN1-MH1-I	9	pc_pf1b_cur_1	
8	PF2 Upper	50	EOH5-CTD-MH1-I	27	pc_pf2u_cur_1	
9	PF2 Lower	50	EOH3-CTD-MH1-I	26	pc_pf2l_cur_1	
10	PF3 Upper (+) Branch	50	EOH2-CTD-MH1-I	29	pc_pf3u_cur_1	∑Current substituting for PSRTC branch current
11	PF3 Upper (-) Branch	25	EOH2-MN2-MH1-I	34	pc_pf3u_br_2_cur_1	
12	PF3 Lower (+) Branch	25	EOH4-CTD-MH1-I	28	pc_pf3l_cur_1	∑Current substituting for PSRTC branch current
13	PF3 Lower (-) Branch	25	EOH4-MN2-MH1-I	33	pc_pf3l_br_2_cur_1	
14	PF5	50	EOH6-CTD-MH1-I	30	pc_pf5_cur_1	
15	CHI Branch 1	25	EOH1-MN2-MH1-I	36	pc_chi_br_1_cur_1	
16	CHI Branch 2	25	EOH1-MN3-MH1-I	35	pc_chi_br_2_cur_1	
17	TF Branch 1	25	ETF1-MN1-MH1-I	1	pc_tf_br_1_cur_1	
18	TF Branch 2	25	ETF1-MN2-MH1-I	2	pc_tf_br_2_cur_1	
19	TF Branch 3	25	ETF1-MN3-MH1-I	3	pc_tf_br_3_cur_1	
20	TF Branch 4	25	ETF1-MN4-MH1-I	4	pc_tf_br_4_cur_1	
21	PF4	30	PF4-MN1	16	pc_pf4_cur_1	
22	SPA1	3.333		65		
23	SPA2	3.333		67		
24	SPA3	3.333		69		
1	OH (+) Branch	25	ETF2-CTD-MH1-I	21	pc_oh_br_1_cur_2	
2	OH (-) Branch	25	ETF2-CTD-MH2-I	22	pc_oh_br_2_cur_2	
3	PF1a Upper (+) Branch	25	PF1AU-CTD-MH2	24	pc_pf1au_cur_2	∑Current substituting for PSRTC branch current
4	PF1a Upper (-) Branch					

5	PF1a Lower (+) Branch	50	EFVC-CTD-MH1-I	23	pc_pf1al_cur_2	∑Current substituting for PSRTC branch current
6	PF1a Lower (-) Branch					
7	PF1b	25	EEF1-CTD-MH1-I	25	pc_pf1b_cur_2	
8	PF2 Upper	25	ESHUNT-OH5	11	pc_pf2u_cur_2	
9	PF2 Lower	25	ESHUNT-OH3	10	pc_pf2l_cur_2	
10	PF3 Upper (+) Branch	25	ESHUNT-OH2	13	pc_pf3u_cur_2	∑Current substituting for PSRTC branch current
11	PF3 Upper (-) Branch	25	Future			
12	PF3 Upper (+) Branch	25	ESHUNT-OH4	12	pc_pf3l_cur_2	∑Current substituting for PSRTC branch current
13	PF3 Lower (-) Branch	25	Future			
14	PF5	25	ESHUNT-OH6	14	pc_pf5_cur_2	
15	CHI Branch 1	50	Future			
16	CHI Branch 2	25	Future			
17	TF Branch 1	25	ETF1-CTD-MH1-I	17	pc_tf_br_1_cur_2	
18	TF Branch 2	25	ETF1-CTD-MH2-I	18	pc_tf_br_2_cur_2	
19	TF Branch 3	25	ETF1-CTD-MH3-I	19	pc_tf_br_3_cur_2	
20	TF Branch 4	25	ETF1-CTD-MH4-I	20	pc_tf_br_4_cur_2	
21	PF4	30	PF4-MN2	32	pc_pf4_cur_2	
22	SPA1	3.333		66		
23	SPA2	3.333		68		
24	SPA3	3.333		70		
	CHI ∑ Current	50	EOH1-MN1-XT1-I	15	pc_chi_tot_cur_1	
	CHI ∑ Current	50	EOH1-CTD-MH1-I	31	pc_chi_tot_cur_1	

- Polarity considerations

- all coil currents defined as (+) when clockwise viewed from above

- some DCCTs are installed backwards, but inverted via a control input variable
- some DCCTs are on coil side of the bus links, others on power supply side (and subject to polarity reversal (w.r.t. coil) when links are reversed; the software accounts for this

• Offset subtraction

- just prior to each pulse, average of last 100 samples of current is taken as the offset and subtracted from measurements during pulse

• During pulse, at each time step, the difference between the magnitude of the two redundant measurements is calculated and compared to a programmable allowable as a check for the validity of the measurements.

- The measurement with the larger magnitude taken as the branch current, corrected for polarity, and used for further processing.

• The coil currents I_{load} are obtained from the sum of the individual branch measurements, and are always handled with respect to the formal definition of current direction

5.0 Protection Features

Following protection features are provided in the PSRTC:

• instantaneous overcurrent protection
  - branch (during standby and pulse modes)
  - load (pulse mode only)

• single pulse $\int i2(t)dt$ protection

• adiabatic coil temperature rise

• axial force protection for PF coils

• axial force protection for PF coils

Table 5: Coil Parameters

Coil	R (center)	ΔR	Z (center)	ΔZ	Turns	Fill	Turn CSA	R(12C)
	(in)	(in)	(in)	(in)			(in^2)	(mOhm)
OH	5.2088	1.7335	41.7490	83.4980	482	0.7403	0.2223	93.17
PF1a	7.2403	1.6265	62.6215	9.1820	20	0.6956	0.9987	1.15
PF1b	11.9768	3.3055	71.8570	7.5030	32	0.6702	0.5195	3.04
PF2a	31.4634	6.4060	76.1225	2.6760	14	0.7409	0.5195	4.01
PF2b	31.4634	6.4060	72.9385	2.6760	14	0.7409	0.9072	
PF3a	58.8370	7.3400	64.3114	2.6760	15	0.6928	0.9072	8.03
PF3b	58.8370	7.3400	61.1274	2.6760	15	0.6928	0.9072	
PF4b	70.6540	3.6040	31.7800	2.6760	8	0.7525	0.9072	10.96
PF4c	71.1210	4.5380	34.9640	2.6760	9	0.6723	0.9072	
PF5a	78.5280	5.3500	25.6840	2.6980	12	0.7689	0.9072	16.81
PF5b	78.5280	5.3500	22.7440	2.6980	12	0.7689	0.9248	
TF Inner	1.1090	2.2180	55.7500	111.5000	12		1.0540	6.32
TF Outer	3.0750	1.5460	49.6875	99.3750	24		1.0530	

Table 6: Coil Ratings

Circuit	Iesw	Tesw	I2T
	(kA)	(sec)	(ka^2-sec)
OH	24.0	0.53	302
PF1aU,L	24.0	2.50	1440
PF1b	20.0	1.00	400
PF2U,L	20.0	5.00	2000
PF3U,L	20.0	5.00	2000
PF4	20.0	5.00	2000
PF5	20.0	5.00	2000
RWM1,2,3	5.0	2.50	63
TF	71.2	1.32	6700
CHI	50.0	1.0	2400

Table 7: Coil Thermal Parameters

Circuit	Thermal Res	Heat Cap	Thermal Tau
	(degC/kW)	(kJ/degC)	(sec)
OH	0.65	397	258
PF1aU,L	1.23	27	33
PF1b	1.22	71	86
PF2U,L	0.70	284	200
PF3U,L	1.05	569	596
PF4	0.81	364	296
PF5	0.18	1239	220
RWM1,2,3	293.33	15	4288
TF	0.054	486	26

• RMS current checks (based on continuous simulation of heating (during pulse) and cooling (between pulses) of DC cable systems. Cable parameters are given in Table 8.

Table 8: DC Cable Parameters

System	Cable Size	#Parallel	Resistance	Cp	Tr	Tau
	MCM		$\mu\Omega$/in	J/degC-in	degC/W-in	minute
OH	1000	1	0.866	44.2	39.0	28.6
PF1a U &L	1000	2	0.433	88.3	19.4	28.6
PF1a Midpoint	1000	2	0.433	88.3	19.4	28.6
PF1b	750	2	0.577	66.2	20.8	23.0
PF2 U&L	1000	3	0.289	132.5	12.9	28.6
PF2 Midpoint	1000	3	0.289	132.5	12.9	28.6
PF3 U&L (+)	750	1	1.155	33.1	68.6	37.9
PF3 U&L (-)	1000	3	0.289	132.5	12.9	28.6
PF3 U&L Midpoint	1000	3	0.289	132.5	12.9	28.6
PF4						
PF5	1000	3	0.289	132.5	12.9	28.6
RWM	500	1	2.16	22.1	22.9	17.2
TF	1000	5	0.173	220.8	7.8	28.6

CHI	750	3	0.385	99.4	22.9	37.9

• Launching load (product of Ioh and Ipf1b shall be ≥ preprogrammed level) (Note: this interlock is still present but not used)

• CHI/TF Interlock (CHI suppressed unless |Itf| ≥ preprogrammed level)

Axial Loads

Influence coefficients given in are used to calculate the force on PF coil x due to its current and the forces in the other y coils as follows…

$$F_x = \sum_y C_{xy} I_x I_y$$

This calculation is performed once each time step for each of the PF coils, namely OH, PF1aU, PF1aL, PF1b, PF2U, PF2L, PF3U, PF3L, PF4, PF5. Limits are included in the PSRTC c.d file for each coil. If the sign of the limit is positive, then a positive force greater than the limit causes a trip, and if the sign of the limit is negative, then a negative force less than the limit causes a trip. The influence coefficients are hard coded into the "rtc_init.f" program. The data generated for the forces on each coil is available as an output which can be selected in the "o.d" file and viewed after each pulse via "readrtc".

Peak Pressure on TF Joint

The first step in calculating the pressure is to calculate the prospective moments in-plane (IP) and out-of-plane (OOP). The in-plane moment is assumed proportional to the square of the TF current. A moment of 70653 in-lbf is generated on the outer layer flags and links at 6kG (71.166kA). So the applied EM moment at any value of current is…

$$M_{EM\_IP} = \left(\frac{I_{TF}}{71167} \right)^2 * 70653$$

The amount of moment which ends up a the joint depends on how much is reacted by the structure. Structural coefficients are based on analysis of field measurements. These are used to estimate the amount of the moment which is reacted by the joint…

$$M_{Joint\_IP} = C_{Structure\_IP} * M_{EM\_IP}$$

Similar calculations are performed for the out-of-plane moment based on the influence matrix given for the our-of-plane moment, and on structural coefficients based on analysis of field measurements. These take the following form…

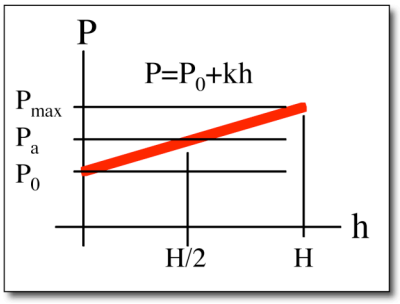
$$M_{Joint\_OOP} = \sum_x C_{x\_OOP} I_x I_{TF}$$

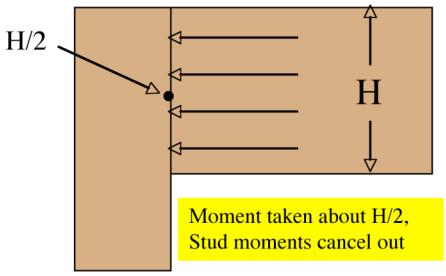
The coefficients C_{x_OOP} are the product of the aforementioned influence matrix coefficients and the structural coefficients, and are hard coded into “rtc_init.f”

The data generated for the in-plane and out-of-plane moments is available as an output which can be selected in the “o.d” file and viewed after each pulse via “readrtc”..

Once the moments are known then peak pressure at the joint can be calculated based on the linear pressure distribution model shown in figures 8 and 9 .

Linear Pressure Model w/o Liftoff





$$F = \int PdA = w\int_0^H Pdh = \frac{A}{H}\int_0^H (P_0 + kh)dh$$

$$k = \frac{2(F - AP_0)}{AH} \qquad A = HW$$

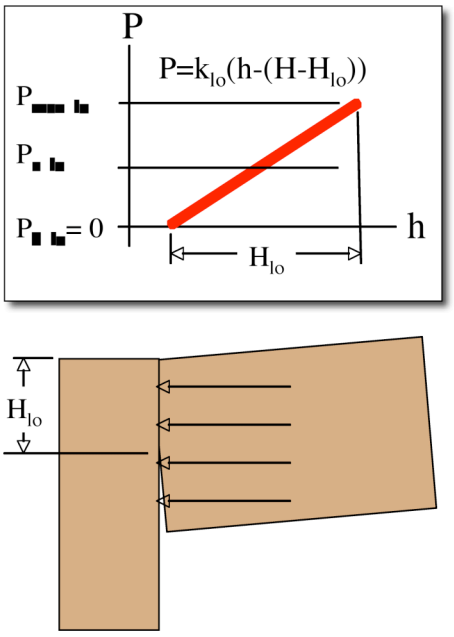
$$M = 2\int_0^{H/2} (P_a - P)(h - H/2)dA$$

$$P_0 = \frac{6M}{AH} - \frac{F}{A} \qquad P_{max} = \frac{6M}{AH} + \frac{F}{A}$$

$$M_{liftoff} = \frac{FH}{6}$$

Figure 8

Linear Pressure Model w/Liftoff



$$H_{lo} = \frac{H}{2} - \frac{3M}{F} \qquad P_{0\_lo} = 0$$

$$A_{lo} = H_{lo}W \qquad k_{lo} = \frac{2F}{A_{lo}H_{lo}}$$

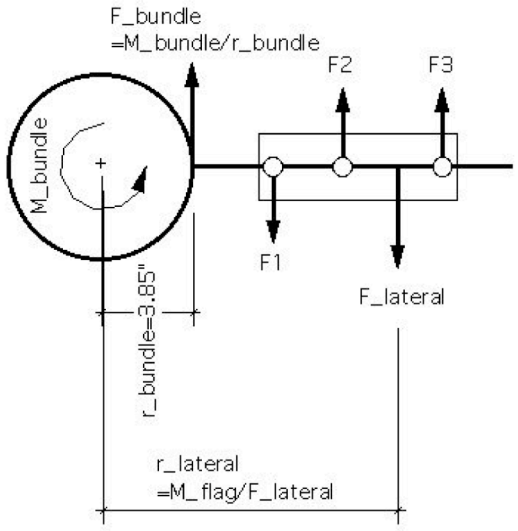
$$P_{max\_lo} = \frac{2F}{3W\left[\frac{H}{2} - \frac{M}{F}\right]}$$

Figure 9

The maximum pressure is compared each time step to an allowable value which is entered in the “c.d” file.

<u>Force On Friction Interface Between Flag Box and Hub</u>

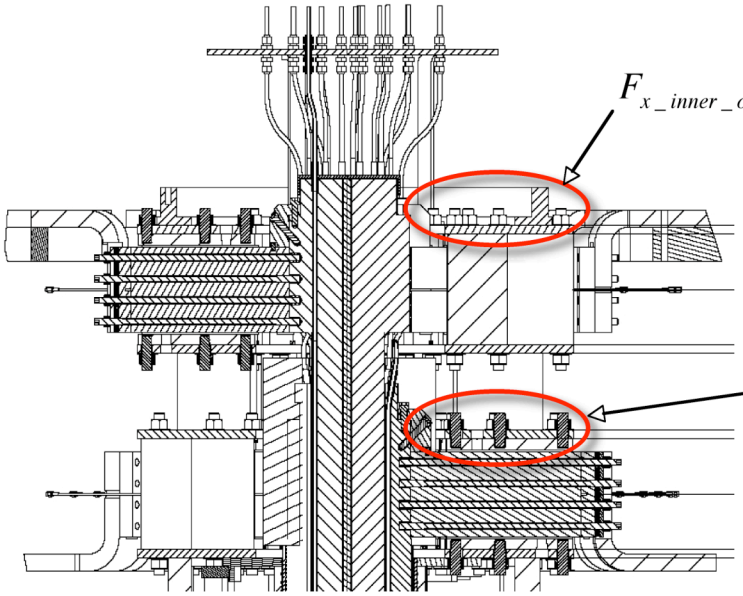
A simplified model is used to estimate the friction shear load on the TF flag box-to-hub interface as shown in figure 10.



$$F_3 = \frac{\left[\frac{(F_b * r_b + F_l * r_l)(r_3 - r_1)}{(r_1(r_3 - r_1) + r_2(r_3 - r_2))} - \frac{(F_b + F_l)(r_3 - r_1)}{(2r_3 - r_1 - r_2)}\right]}{\left[\frac{(r_3 - 2 * r_1 + r_2)}{(2r_3 - r_1 - r_2)} - \frac{(r_3 * (r_3 - r_1) + r_2 * (r_2 - r_1))}{(r_1(r_3 - r_1) + r_2(r_3 - r_2))}\right]}$$

$$F_1 = \frac{-\left[F_3(r_3 - 2r_1 + r_2) + (F_b + F_l)(r_3 - r_1)\right]}{(2r_3 - r_1 - r_2)}$$

$$F_2 = F_1 - \frac{(F_1 - F_3)(r_2 - r_1)}{(r_3 - r_1)}$$



$$F_{x\_inner\_oop} = \frac{F_{x\_inner}}{2} + \frac{\sum F_{x\_inner}}{3} + \frac{\sum F_{x\_outer}}{3}$$

$$F_{x\_outer\_oop} = \frac{F_{x\_outer}}{2} + \frac{\sum F_{x\_outer}}{3}$$

Figure 10

Prior analysis showed that the innermost stud location (F1) on the outer layer flag box interface with the middle hub disk is the one most highly stressed. For this case the PSRTC calculations for the out-of-plane shear load are as follows…

$K_1 = R_{bundle} = 3.848$

$$K_2 = R_3 - R_1 = 6.375$$

$$K_3 = \frac{(R_1(R_3 - R_1) + R_2(R_3 - R_2))(R_3 - 2R_1 + R_2)/(2R_3 - R_1 - R_2) - (R_3(R_3 - R_1) + R_2(R_2 - R_1))}{(R_1(R_3 - R_1) + R_2(R_3 - R_1))} = -38.781$$

$$K_4 = \frac{(2R_3 - R_1 - R_2)(R_3 - 2R_1 + R_2)/(2R_3 - R_1 - R_2) - (R_3(R_3 - R_1) + R_2(R_2 - R_1))}{(R_1(R_3 - R_1) + R_2(R_3 - R_1))} = -5.180$$

$$K_5 = -(R_3 - 2R_1 + R_2) = -9.000$$

$$K_6 = 2R_3 - R_1 - R_2 = 10.125$$

$$K_7 = \frac{R_2 - R_1}{R_3 - R_1} = 0.412$$

$$F_3 = \frac{(F_{bundle} * K_1 + M_{lateral}) * K_2}{K_3} - \frac{(F_{bundle} + F_{lateral}) * K_2}{K_4}$$

$$F_1 = \frac{\left(F_3 * K_5 - \left(F_{bundle} + F_{lateral}\right)\right) * K_2}{K_6}$$

$$F_2 = \left(F_1 - \left(F_1 - F_3\right)\right) * K_7$$

$$F_{1\_OOP} = \frac{F_1}{2} + \frac{\left(F_1 + F_2 + F\right)_3}{3}$$

…where F_{bundle}, $F_{lateral}$,and $M_{lateral}$ are forces and moments calculated via the influence matricies given in [1].

The in-plane shear load is based on the shear load calculated per square ampere of TF current at 6kG…

$$K_8 = 3.002E-7$$

$$F_{1\_IP} = K_8 * I_{TF}^2$$

Finally the net load is the vector sum of the in-plane and out-of-plane loads…

$$F_{1\_NET} = \sqrt{F_{1\_IP}^2 + F_{1\_OOP}^2}$$

The calculated force is compared to a limit value set in the “c.d” file. The data generated for the force is available as an output which can be selected in the “o.d” file and viewed after each pulse via “readrtc”.

6.0 Simulation Mode

In order to test the PSRTC, a simulation package is included which interfaces with the real time control code at the same points of input and output as in normal operation (the inputs being the PSS branch currents and the outputs being the a commands to the power supplies.

PPPL's LRSIM code is used.

Following features are included:

- Transient solution of mutually coupled L/R circuits
  - at present, only the coils are included
  - a more extensive filament model of passive structure may be added in the future
- 10 simulation time steps per control system time step
- Simulation of latency of input data by utilization of simulation results obtained midway between control system time steps as inputs to control algorithm
- Simulation of transient heating of coils and its effect on ohmic resistance
- Simulation of delays and limits of power supplies; however individual thyristor commutations are not modeled

Nominal mutual inductance matrix, and resistance vector, is given in Table 8.

Table 8: Mutual Inductances (mH) and Resistances (mΩ)

	OH	1aU	1aL	1b	2U	2L	3U	3L	5	CHI	TF
OH	13.000	3.511	3.511	0.374	0.276	0.276	0.295	0.295	0.527	0.000	0.000
1aU	3.511	4.470	0.000	0.000	0.072	0.001	0.060	0.005	0.042	0.000	0.000
1aL	3.511	0.000	4.470	0.090	0.001	0.072	0.005	0.060	0.042	0.000	0.000
1b	0.374	0.000	0.090	0.536	0.002	0.186	0.007	0.101	0.054	0.000	0.000
2U	0.276	0.072	0.001	0.002	1.980	0.010	0.731	0.041	0.346	0.000	0.000
2L	0.276	0.001	0.072	0.186	0.010	1.980	0.041	0.731	0.346	0.000	0.000
3U	0.295	0.060	0.005	0.007	0.731	0.041	5.180	0.166	1.490	0.000	0.000
3L	0.295	0.005	0.060	0.101	0.041	0.731	0.166	5.180	1.490	0.000	0.000
5	0.527	0.042	0.042	0.054	0.346	0.346	1.490	1.490	12.300	0.000	0.000
CHI	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.080	0.000
TF	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	4.180
Resist	97.400	2.800	2.800	2.760	4.170	4.170	8.340	8.340	17.400	7.000	4.690

Note: PF1A smoothing reactor inductances are included in the above.

• External Circuit Resistances (ECR in c.d file), due to the cabling within the power supply building, and that from the power supply building, as measured by PTP-ECS-029, is listed in Table 9.

Table 9: External Circuit Resistances

Circuit	Resistance (mOhm)
OH	3.32
1aU	10.0
1aL	10.0
1b	5.86
2U	2.61
2L	2.35
3U	4.85
3L	4.84
5	2.82
CHI	3.76
TF (2 parallels)	1.21
TF (4 parallels)	1.02

Note: PF1A smoothing reactor resistances are included in the above.

7.0 Implementation

The PSRTC is written primarily in FORTRAN. Some hardware specific adjuncts required for real time execution are written in C. The FORTRAN part can run on any platform.

System consists of…..

- Force host computer
  - ethernet connectivity
  - user interface

- Skybolt II real time computer

- four parallel G4 processors on motherboard with Front Panel Data Port (FPDP)

- VME based acquisition system (DAS)
  - two crates in NSTX Test Cell
  - one crate in junction area
  - Fiber Optic Interface Boards (FOIBS) connecting the crates

- Power Conversion (PC) Link driver
  - interface to serial command link which distributes commands to power supplies

• The PSRTC occupies one of the four parallel processors; the other three are available to the PRTC.

• The control system update rate is 1kHz (once per millisecond).

8.0 Input/Output

8.1 Inputs

PSRTC requires the following input files:

c.d – contains control data (Table 10)

t.d – contains timing data (Table 11)

s.d – contains simulation data (Table 12)

o.d – contains selection of variables to be stored in output file (maximum of 50 may be saved during any particular shot). For each variable listed, a “1” indicates save, a “0” indicates do not save

cntmtx.d – contains mutual inductance matrix and resistance vector (see Table 8 in prior section of this document)

Table 10: Input File c.d

Name	i	j	k	Description
NMODE				Mode (0=norm, 1=test)
NSUBMODE				Submode (0=ops, 1=simulation)
NLOCK	1-12			Lockout (0=in, 1=out); locked out circuits not controlled, only suppress/bypass command is given
NPC	1-12			Plasma Control Enable (0=disabled, 1=enabled); this controls whether or not a circuit will accept voltage reference from plasma control
GAIN	1-12	1-2	1	Proportional Gain during a pulse, in ohms (volts per amp error)
GAIN	1-12	1-2	1	Integral Gain during a pulse, in farads (volts per amp-sec error)
GAIN	1-12	1-2	2	Prop Gain, Clamp
GAIN	1-12	1-2	2	Int Gain, Clamp
NMEAS	1-19	1-2		Measurement #'s (1 to 38) of two redundant branch current measurements)
NPMEAS	1-19	1-2		Measurement Polarity w.r.t Coil with bus links in normal position
NLMEAS	1-19	1-2		Measurement Location 1=SDS side (does not change polarity with link reversal), -1=PS Side (changes polarity with link reversal)
FSMEAS	1-19	1-2		Full Scale of Measurement in kA
NCB	1-19	1-2		Circuit # of in which branch is located
KPB	1-19			Branch Polarity & Multiplier, used in simulation only; if KPB>0, current can only be positive in branch, if KPB<0, current can only be negative in branch; current in branch = KPB*ILOAD/NP
DIMAX	1-19			Allowable DCCT Discrepancy (difference between redundant measurements) in kA
NPLINK	1-12			Bus Link Polarity (1=normal, -1=reverse)
NP	1-12			# Parallel branches feeding circuit
NS	1-12			# Series power supply sections feeding circuit
ICLP	1-12			(+) Current Clamp Level in kA
ICLN	1-12			(-) Current Clamp Level in kA
VAC				AC Source Voltage (13.8kV Level) in kV
FAC				AC Source Frequency in Hz
GAMMA	1-12			Margin angle gamma (max alpha = 180 - gamma - commutation angle) in degrees

Table 9: Input File c.d (con't)

Name	i	j	k	Description
LC	1-12			Commutating Inductance (nominal value = 22 microhenries) in microhenries
VDOTMAX	1-12			Maximum dVpu/radian for rate limiting; normal sine wave as maximum of 0.637 per unit per radian
NAP	1-12			Antiparallel Enable (0=disable, 1=enable)
NAPBLOCK	1-12			Antiparallel Initial State Block (0=no block, 1=block antiparallel until first zero crossing)
ITHRESH	1-12			Antiparallel Current Magnitude Threshold in kA
IBOC	1-19	1-2		Branch Overcurrent Standby State in kA
IBOC	1-19	1-2		Branch Overcurrent Pulse State in kA
ILOC	1-12			Load Overcurrent Pulse State in kA
I2TMAX	1-12			I2T Limit in kA^2-sec
NPSUM	1-22	1-2		Circuit # of ILOAD in to DC Pole
NPSUM	1-22	1-2		Circuit # of ILOAD out of DC Pole
R20POLE	1-22			Pole 20C Electrical Resistance in mircoohm/inch
TRPOLE	1-22			Pole Thermal Resistance in degC-inch/watt
TCPOLE	1-22			Pole Thermal Capacitance in Joule/degC-in
NPPOLE	1-22			Polarity Constraint on Pole (0=no constraint, 1=(+) only, -1=(-) only)
T0POLE				Ambient Temperature for Cables in degC
TMPOLE				Allowable Temperature for Cables in deg C
ALAUNCH				Allowable Ioh*Ipf1b in kA^2
ITFMIN				Minimum |Itf| for CHI in kA
ICHI0				Minimum |Ichi| for ITFMIN check in kA
SCD	1-12			Shutdown Current Derivative, takes effect after plasma control drops out (NPCON=0) in kA/mS
TCCOIL	1-12			Coil Thermal Capacity in kJoule/degC
COEFF				Copper Thermal Coefficient of Resistance, nominally 0.0041
T0COIL	1-12			Coil Water Inlet Temperature, nominally 10 deg C
FINV				Max invert voltage fraction, nominally -0.666
ECR	1-12			External Circuit Resistance, exc'l CLR, in mOhm
ECL	1-12			External Circuit Inductance, exc'l CLR, in microhenry

RPSS	1-12			Power Supply Section Equiv Resistance, nominally 16 mOhm

Table 10: Input File t.d

Name	Circuit	Description
TSOP		Time of SOP clock event, relative to t0
TPCSTART		Time to start plasma control, relative to t0
TPCEND		Time to end plasma control, relative to t0
TIRESET	1-12	No Longer Used
NBPOINT	1-12	Number of breakpoints to follow for each circuit
BPOINT		Time (relative to t0), data (kA or kV), and mode (0=current control, 1=voltage control)

Table 11: Input File s.d

Name	Description
NCHIDSO	Simulate bit which =1 if CHI SDS open, =0 if closed
NHCSTF	Simulate status of TF HCS, 0 = no fault, 1 = fault
NHCSOH	Simulate status of OH HCS, 0 = no fault, 1 = fault
NHCSPFCHI	Simulate status of PFCHI HCS, 0 = no fault, 1 = fault
FMG	Simulate status of MG frequency, in Hz
VMG	Simulate status of MG voltage, in volts
NPCREADY	Simulate status of ready flag from plasma control, 0 = not ready, 1 = ready
NOUTDT	No longer used

8.2 Outputs

PSRTC produces an output file called o_*.d, where * may be…

- a numeric sequence
- date and time
- shot number

o_*.d contains the data collected for the variables identified in o.d (up to 50), for each millisecond, followed by a list of alarms and faults which may have occurred, followed by a list of the names of the collected data