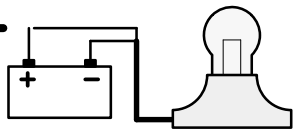
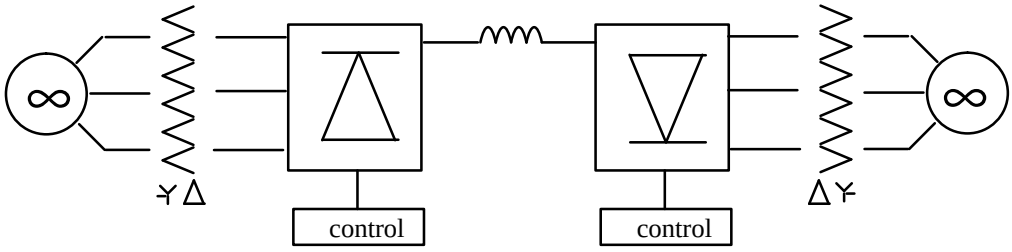
5 A SIMPLE HVDC SYSTEM



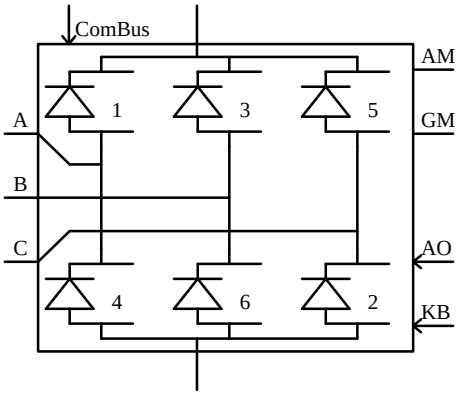
By using standard routines available from the PSCAD/DRAFT palette, the user can quickly assemble a power system model which includes HVDC transmission. As an example, the simple back to back HVDC system, shown below, is simulated.



The system is simplified as possible so as to highlight the very basics required to assemble a DC system. By using infinite sources at both the sending and receiving end commutating buses, no AC filters are required.

5.1 THE SIX PULSE HVDC VALVE GROUP MODEL

A Graetz bridge valve group icon is available from the DRAFT palette. The model includes the thyristor valves, snubber circuits, as well as internal pulse generation.



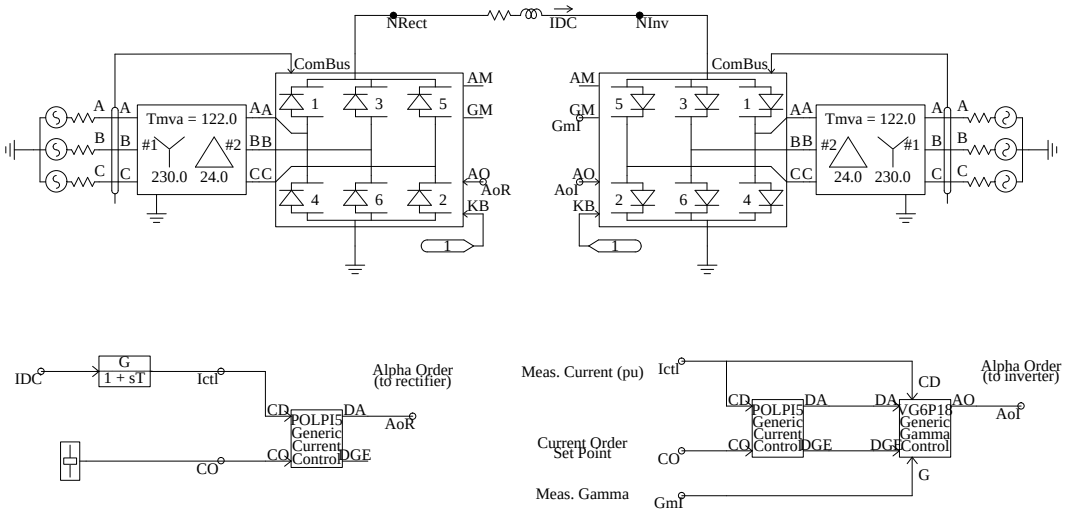
ComBus: Phased locked oscillator input signal
AM: Measured alpha signal
GM: Measured gamma signal
AO: Alpha order input (radians)
KB: Block/Deblock signal

The block/deblock input variable "KB" for the valve group icon can be assigned the following values:

- KB = 0: Block all pulses
- KB = 1: Deblock
- KB = –1 ... –6: Block only the firing pulse to valve #1 ... #6
- KB = –7: Block and bypass

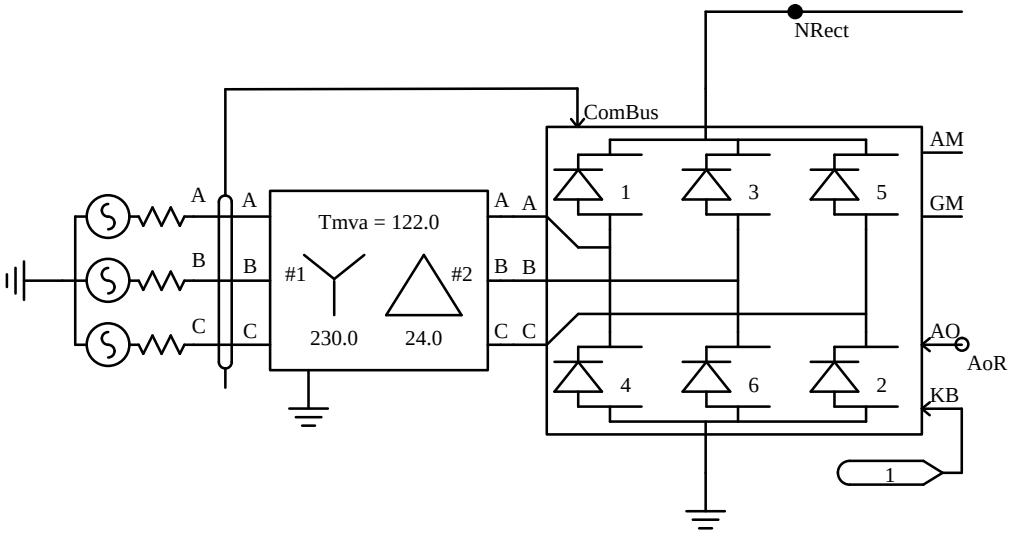
5.2 BUILDING THE SYSTEM MODEL

The system model used here is shown in its entirety below. The magnitude of the system equivalent, at both the rectifier and inverter ends, is set to 230.0 kV L–L. Both system equivalents are assigned an internal resistance of 0.1Ω, so as allow operation without AC side filter banks.

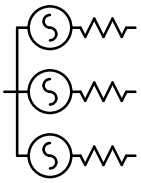


5.2.1 The Rectifier Circuit Portion

To build this circuit, it is best to work in stages. First, the rectifier portion, shown in greater detail below, should be created.

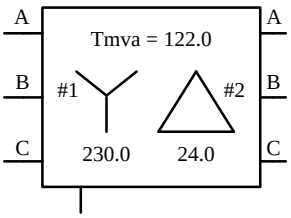


Parameters for the rectifier three phase source are shown here:



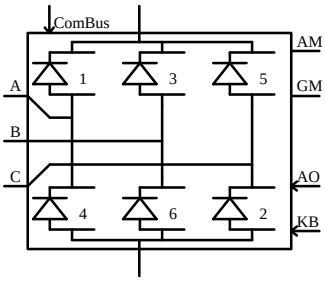
Section: CONFIGURATION		
Name	Source Name	: Rectifier
Type	Source Impedance Type:	: R
Ctrl	Source Control:	: RunTime
MVA	System Base MVA (3–phase)	: 100.0 MVA
Vm	Rated Volts (L–L, RMS)	: 230.0 kV
F	Base Frequency	: 60.0 Hz
Tc	Voltage Input Time Constant	: 0.05 sec
ZSeq	Zero Sequence Included	: No
Imp	Impedance Data Format:	: RRL Values
Section: POSITIVE SEQUENCE RRL		
R1s	Resistance (series)	: 0.1 Ohms
Section: SOURCE INITIAL VALUES		
Es	Initial Source Mag (L–L, RMS)	: 230.0 kV
F0	Initial Frequency	: 60.0 Hz
Ph	Initial Phase	: 0.0 deg
Section: INTERNAL OUTPUT VARIABLES		
	(Leave all entries blank)	
Section: REMOTE FAULTS		
Tf	Fault Duration	: 0.10 sec
Rf	Source Voltage During Fault	: 0.50 p.u.

Parameters for the rectifier three phase transformer are shown here:



Section: CONFIGURATION		
Name	Transformer Name	: Rectifier
Tmva	3 Phase Transformer MVA	: 122.0 MVA
f	Base operation frequency	: 60.0 Hz
YD1	Winding #1 (0=Y, 1=Delta)	: 0
YD2	Winding #2 (0=Y, 1=Delta)	: 1
Lead	Delta lags (1) or leads (2) Y	: 1
Xl	Positive sequence leakage reactance	: 0.1786 p.u.
Ideal	Ideal Xformer model (0=No,1=Yes)	: 0
NLL	No load losses	: 0.0 p.u.
Tap	Tap changer winding (0=None)	: 0
Section: WINDING #1		
V1	Line to line voltage (RMS)	: 230.0 kV
Im1	Magnetizing current	: 1.0 %
Section: WINDING #2		
V2	Line to line voltage (RMS)	: 24.0 kV
Im2	Magnetizing current	: 1.0 %
Section: SATURATION		
Enab	Saturation Enabled (0=No,1=Yes)	: 0
Sat	Saturation Placed on Winding	: 1
Xair	Air core reactance	: 0.2 p.u.
Tdc	In rush decay time constant	: 1.0 sec
Xknee	Knee voltage	: 1.25 p.u.
Txk	Time to release flux clipping	: 0 sec
Section: WINDING 1 LINE CURRENTS		
	(Leave all entries blank)	
Section: WINDING 2 LINE CURRENTS		
	(Leave all entries blank)	
Section: WINDING 2 DELTA CURRENTS		
	(Leave all entries blank)	
Section: MONITORING OF FLUX AND MAGN CURRENT		
	(Leave all entries blank)	

Parameters for the rectifier valve group are shown here:



Section: CONFIGURATION		
UP	Thryristor direction (1=Up,0=Dwn)	: 1
FR	Rated Frequency	: 60.0 Hz
KV	Transformer Configuration Var.	: –2
FP	Firing Pulses (0=PLO. 1=External)	: 0
Section: PHASED LOCKED OSCILLATOR		
GP	PLO Proportional Gain	: 10.0
GI	PLO Integral Gain	: 100.0
KP	PLO Input Reference Var.	: 1
Section: VALVE DATA		
RD	Snubber Resistance	: 5000.0 ohms
CD	Snubber Capacitance	: 0.05 uF
RON	Thyristor ON Resistance	: 0.01 ohms
ROFF	Thyristor OFF Resistance	: 1.0E6 ohms
EFVD	Forward Voltage Drop	: 0.001 kV
EBO	Forward Breakover Volts	: 1.0E5 kV
TEXT	Minimum Extinction Time	: 0.0 usec
Section: INTERNAL OUTPUT VARIABLES		
	(Leave all entries blank)	

The transformer configuration variable “KV” is used to determine a phase advance/ lag for the valve firing. It is set as follows:

KV = 1: Pulse firing in 30 deg. in phase advance with the volts of phase A
KV = 0: Pulse firing in sync with the volts of phase A
KV = –1: Pulse firing is 30 deg. lagging with the volts of phase A
KV = –2: Pulse firing is 60 deg. lagging of the volts of phase A

	Valve Side Winding		
AC Side Winding	Star	Delta (lead)	Delta (lag)
Star	KV= –1	KV= 0	KV= –2
Delta (lead)	KV= –2	KV= –1	N/A
Delta (lag)	KV= 0	N/A	KV= –1

The parameters for the rectifier node “NRect” are shown here:

Section: MAIN DATA		
Nname	Node Name	: NRect
VBase	Voltage Scaling Factor (L–G)	: 1 kV,peak
MonV	Plot Voltage in RunTime	: Yes
MeasV	Measure Voltage in Circuit	: No
PU	Scale Voltage	: No
Section: RUNTIME VOLTAGE PLOTTING		
DL	Description	: Node $NName
Max	Default Maximum Limit	: 40.0
Min	Default Minimum Limit	: 0.0
Units	Units	: kV

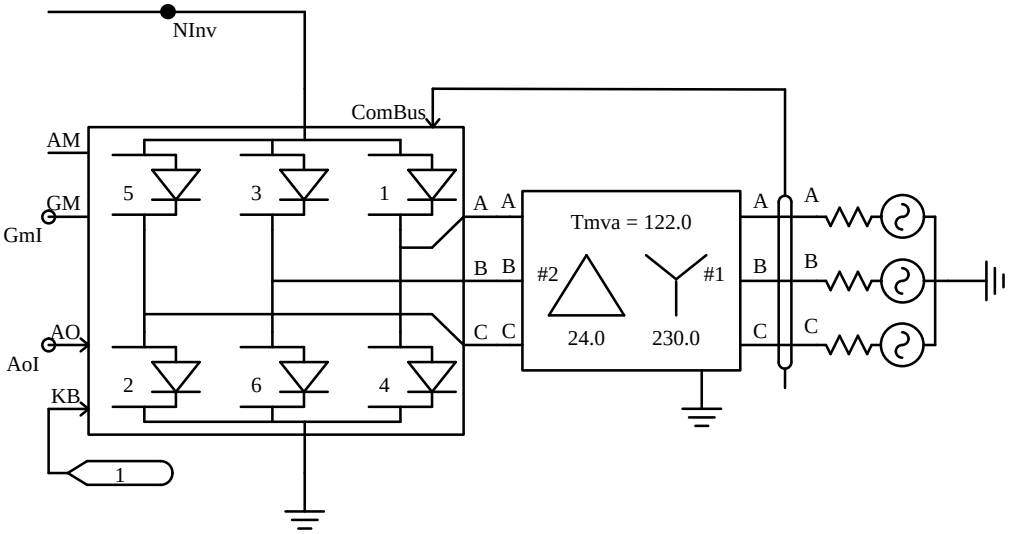
The parameter for the wire label is shown here:

Name	Wire Name	: AoR

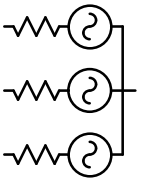
The remaining components of the rectifier portion for this circuit model do not have any parameters associated with them.

5.2.2 The Inverter Circuit Portion

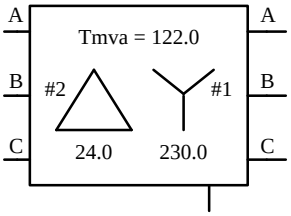
To create the inverter portion of the circuit, the rectifier components should be grouped, copied, mirrored, and placed back on the drawing canvas. Position it such that there is room for the components for the line model, which is three grid units long.



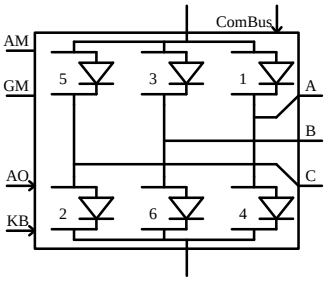
By copying the rectifier portion, the inverter portion creation is greatly simplified, since only the following parameters must be changed:



Section: CONFIGURATION
Name Source Name : Inverter
: : : :



Section: CONFIGURATION
Name Transformer Name : Inverter
: : : :



Section: CONFIGURATION
UP Thryristor direction (1=Up,0=Dwn) : 0
: : : : :

NInv

```
Section: MAIN DATA
    Nname   Node Name                          : NInv
      :       :       :       :       :       :
```

AoI

```
    Name    Wire Name                          : AoI
```

Finally, one new wire label for the measured gamma from the inverter value group is required.

GmI

```
    Name    Wire Name                          :: GmI
```

5.2.3 A Very Simple Line Model

The rectifier and inverter valve groups are interconnected on the DC side through a simple series RL (R=0.34 Ω L=0.04H) branch.

IDC

```
    R       Resistance                         : 0.34      Ohms
```

```
    L       Inductance                         : 0.04      H
```

The current which flows through this line is measured and assigned to the variable "IDC". This quantity will be used in the control system.

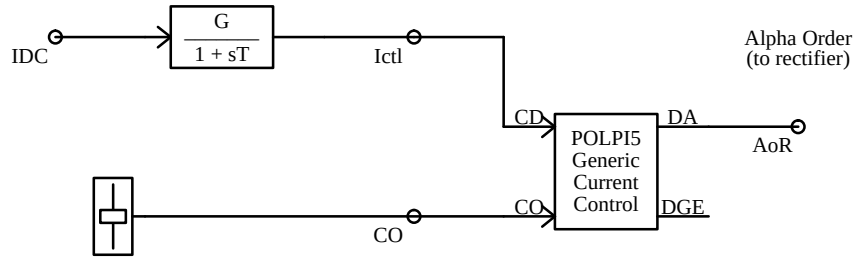
IDC

```
Section: CONFIGURATION
    Name    Signal Name                        : IDC
    RTmn    Plot current in RunTime            : Yes
Section: RUNTIME CURRENT PLOTTING
    DL      Description                        : $Name
    Max     Default Maximum Limit              : 4.0
    Min     Default Minimum Limit              : 0
    Units   Units                              : kA
```

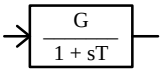
5.2.4 Rectifier and Inverter Controls

Generic current control and gamma control models are available for use with the valve group. The diagrams below show the rectifier and inverter controller icons, their parameters, and their labelling.

RECTIFIER CONTROLS



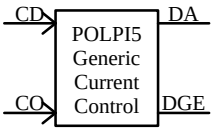
The measured DC current is passed through a 1st order lag function. The lag's gain of 0.27778 is chosen so that a DC current of 3.6kA produces a control signal of 1 pu. The 5mS time constant is used to provide some smoothing on the DC current before it is passed to the controls.



Section: CONFIGURATION		
Limit	Limit output?	: No
COM	Fortran Comment	: Real Pole
Section: MAIN DATA		
G	Gain	: 0.27778
T	Time Constant	: 0.005 sec

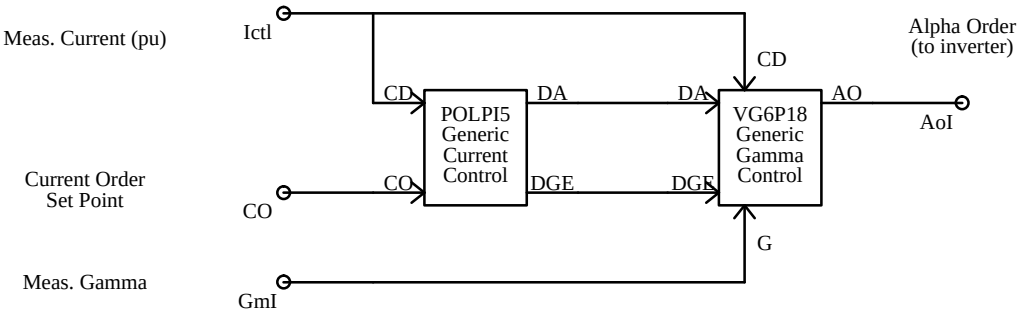
The slider component allows the creation of a slider on the OPERATOR'S CONSOLE through which the current order may be varied during the run.

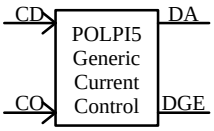
Desc	Description	: Iorder
Group	Group Name	:
Value	Initial Value	: 0.0
Max	Maximum Value	: 1.0
Min	Minimum Value	: 0.0
Units	Units (eg: kA, kV, P.U.)	: P.U.



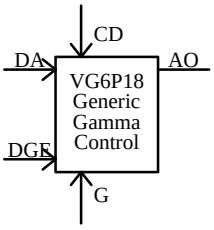
CM	Current Margin	: 0.0 p.u.
DV	Slope of Current Error	: 0.0 p.u.
AMAX	Alpha Maximum Limit	: 3.142 Radians
AMIN	Alpha Minimum Limit	: 0.0 Radians
GR1	Integral Gain	: 5.0 deg/amp–s
GR2	Proportional Gain	: 0.02 p.u.

INVERTER CONTROLS





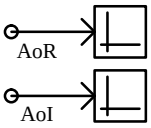
CM	Current Margin	: 0.1 p.u.
DV	Slope of Current Error	: 0.1 p.u.
AMAX	Alpha Maximum Limit	: 2.8 Radians
AMIN	Alpha Minimum Limit	: 1.5 Radians
GR1	Integral Gain	: 5.0 deg/amp–s
GR2	Proportional Gain	: 0.02 p.u.



F	Base Frequency	: 60.0 Hertz
AMIN	Alpha Minimum Limit	: 1.5 Radians
AMAX	Alpha Maximum Limit	: 2.8 Radians
GMIN	Minimum Gamma Order	: 0.2618 Radians
GP	Proportional Gain	: 0.2 p.u.
GI	Integral Gain	: 10.0 1/sec
CF	Incremental Current Level	: 0.4 p.u.
TF	Current Fade Out Constant	: 0.02 seconds

Notice that wire label icons have been used extensively in the interface between the controls and the valve groups. The circuit could also have been assembled by directly interconnecting the valve group inputs and outputs to the controller icons. By using wire labels, however, the circuit diagram can usually be made to appear less cluttered.

Any control variables assigned a name can be connected to a plot icon and thus made available for monitoring during the RUNTIME session.



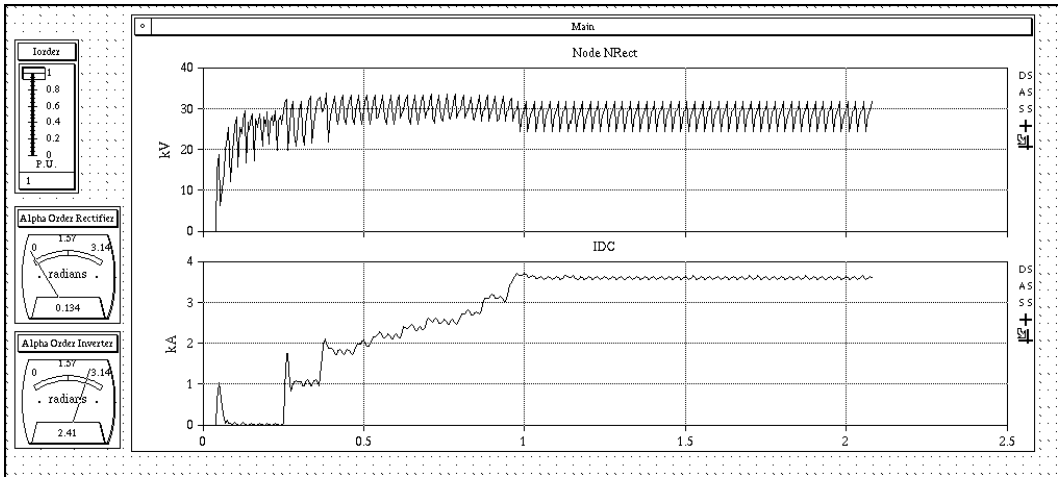
It is possible for the user to design their own current and / or gamma controller using individual control type function blocks available from the DRAFT palette. For more information regarding the models used to represent the controls, refer to the *EMTDC User's Manual*.

5.2.5 Compile and Save

As before, the circuit drawing must be compiled, and saved before the DRAFT module is exited or iconed. Use a time–step of 50µS, and a finish–time of 2500 mS for the circuit parameters. If any errors or warning messages are generated, ensure the proper components and parameter values have been used.

5.3 PERFORMING THE SIMULATION

A screen dump showing the OPERATOR'S CONSOLE setup for the simple HVDC system is given below. Meters have been used to display the firing angles produced by the controls. Since there are infinite buses at both ends, the DC valve groups are deblocked immediately upon startup of the case.



The current order is provided through a slider input. The current order should be set to zero at the beginning of the run and can slowly be raised to 1 p.u. over some portion of the run.

Under a more realistic AC system representation, the user starts the simulation with the valve groups blocked. A deblock sequence will then be started some cycles after the simulation begins so that there will be sufficient time for the AC commutating bus voltages to ramp up and stabilise. This is especially true if the user has placed synchronous machine models near the commutating bus.

The simple HVDC system presented here can be enhanced by the user to represent a physical power system more accurately.