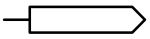
7 THE CIGRE BENCHMARK MODEL

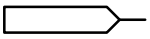
The example cases documented in previous sections of this manual have, for the most part, been chosen to illustrate general concepts and use of the PSCAD software. In this section, a practical system model is documented. The power system portion of the model is based on one developed as a CIGRE benchmark [1]. The model's sending end AC system is identical to that subjected to the frequency scan in the previous chapter.

General assembly of the power system model and its associated controls are documented. The technique of bringing a system model to a steady–state operating condition and saving its state into a *snapshot* file is also discussed.

Since the CIGRE benchmark model is fairly large, the circuit is spread over several DRAFT pages. Voltage and current signals are exported from the main circuit page, and imported into the controls page(s). The control system output signals are then exported from the control page and imported into the main circuit page.

Note that electrical networks may not be connected with import and export symbols: only "information" may be exported from one page to another. For example, current will not flow through an export symbol, but a current meter may measure the current in an electrical branch, and the current signal may be exported. To connect electrical networks on separate pages, transmission lines or cables must be used.


Export Symbol


Import Symbol

Open the "`CIGRE`" case in the "`Tutorial`" project, and select COPY on the "`Main50.dft`" circuit drawing icon. Inside the "`LearningPSCAD`" project, create a "`CIGRE`" case, and select PASTE from the main menu once inside that case.

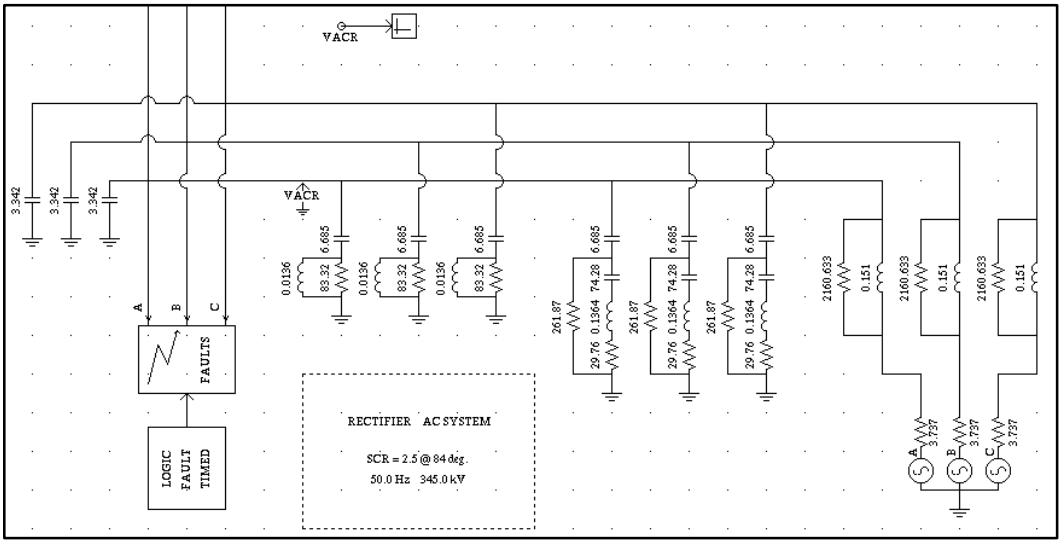
1. "First benchmark model for HVDC control studies", by M. Szechtman, T. Wess and C.V. Thio CIGRE WG 14.02 **Electra** No. 135 April 1991 (pp 54 – 73)

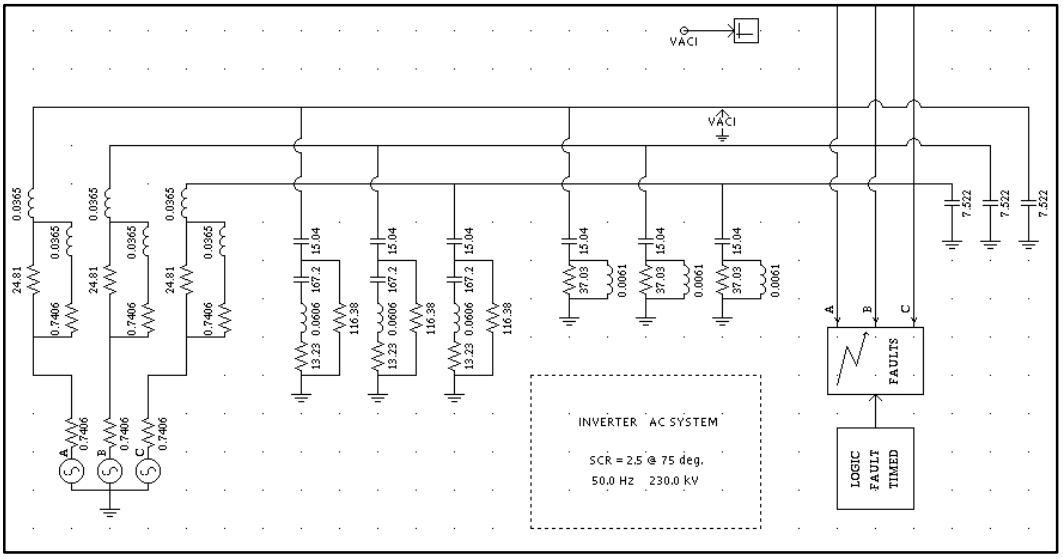
7.1 SENDING AND RECEIVING END AC SYSTEMS

The sending (rectifier) and receiving (inverter) end ac systems used for the model are illustrated below. The system has been setup to operate at 50 Hz. Component values have been chosen in accordance with the model documented in the CIGRE paper and result in the following short circuit ratios.

- Rectifier SCR = 2.5 @ 84° 345 kV
- Inverter SCR = 2.5 @ 75° 230 kV

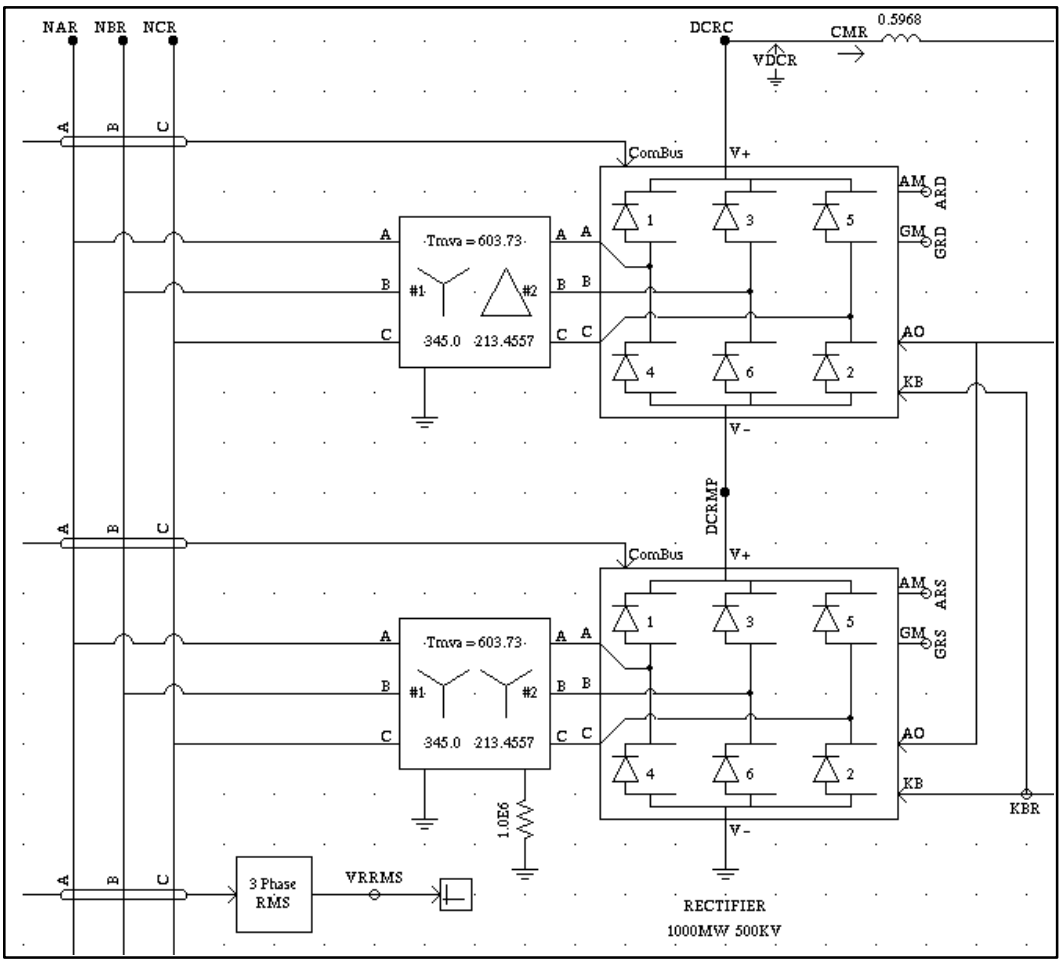
The impedance magnitude and phase versus frequency of the sending end ac system are shown in the previous section. It is interesting to note that both sending and receiving end ac systems have a impedance peak near 100 Hz (ie. 2nd harmonic at 50 Hz).





7.2 VALVE GROUPS AND DC SYSTEM

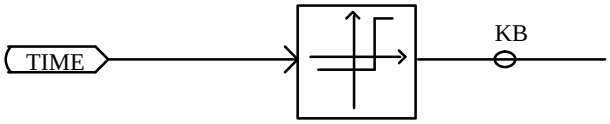
Two valve groups connected in series are used to represent 12 pulse groups as shown below. The 'KV' variable associated with the valve group model should be set to –1 for the wye–wye connected group and –2 for the wye–delta connected group. Each group operates from its own internal phase locked oscillator.

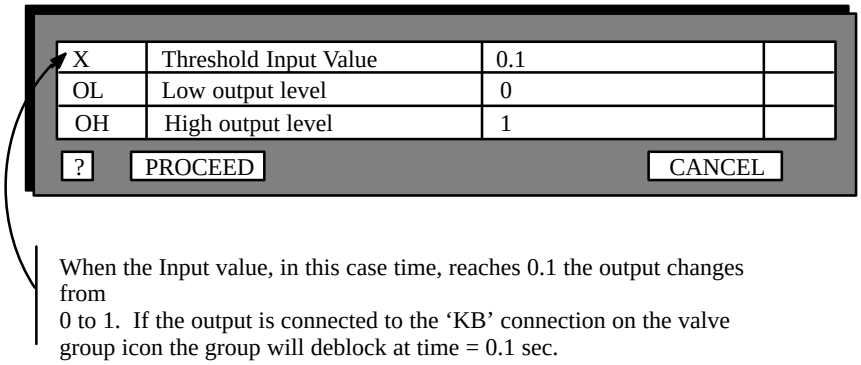


In order to ensure a proper startup of the valve groups when they are connected to a non infinite bus ac system, the 'KB' variable which is associated with the groups should be kept equal to zero until the ac system has had a chance to stabilize. With 'KB' equal to zero, firing pulses to the group's thyristors remain blocked.

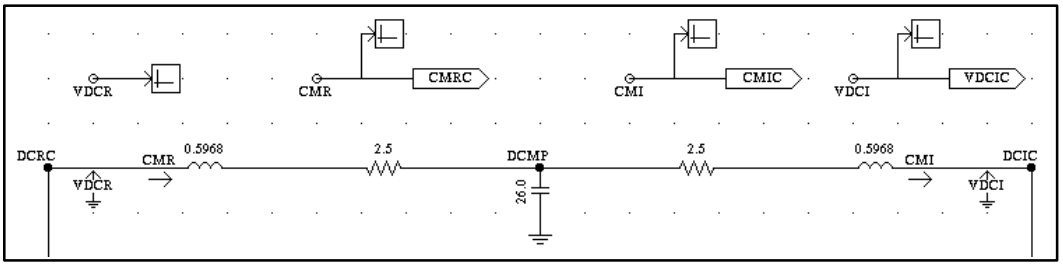
The duration required for the AC system to reach a steady–state operating condition depends upon the nature of the AC system itself. The presence of long transmission lines or machine models may require that the groups remain blocked for a significant amount of time.

By using the components illustrated below, the ‘KB’ signal can be automatically generated so that the valve groups deblock at a specific time. It is also possible to manually deblock the valve groups by using a switch icon from the OPERATOR’S CONSOLE.



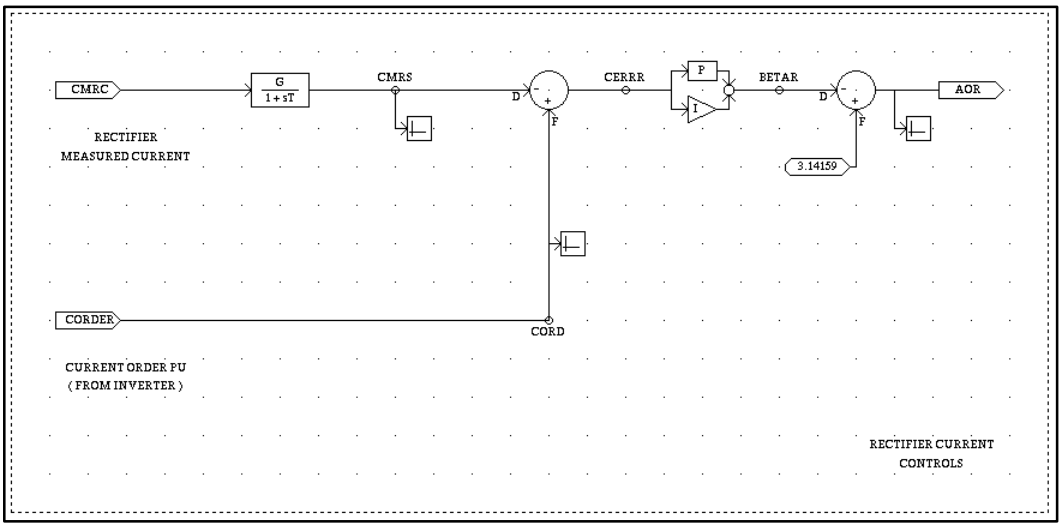


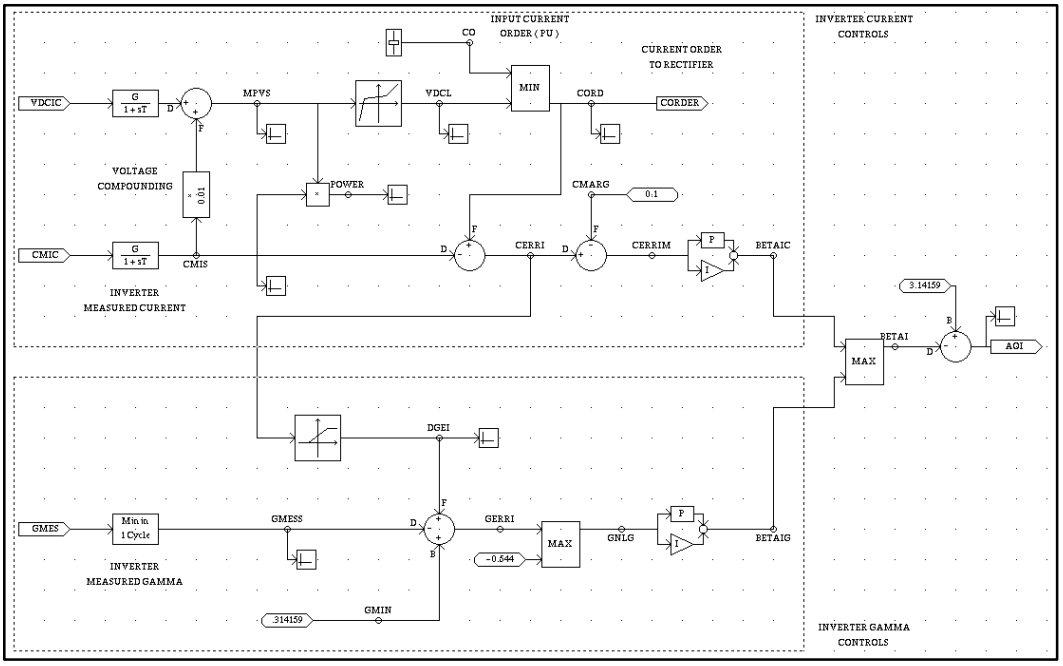
The DC system used for the model is shown below. A simple T–section is used to represent a cable, characterized by a high capacitance and a low inductance. The inductance and capacitance values selected result in an impedance maximum near fundamental frequency of 50 Hz.



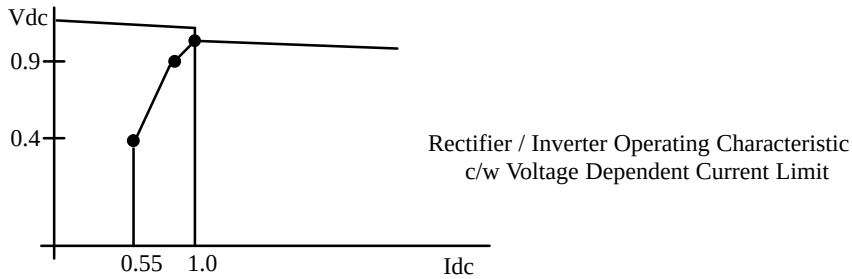
7.3 RECTIFIER AND INVERTER CONTROLS

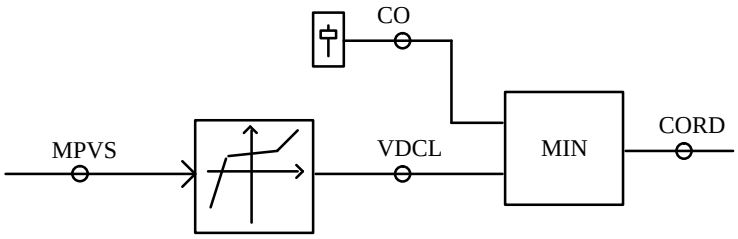
The controls models for both the rectifier and inverter are based essentially on proportional and integral function blocks. While the rectifier controls consist only of a current control loop, the inverter controls contain both a current control and gamma control loop. Voltage dependent current limits are included in the controls model. A master control loop is not modelled. A slider is used to set the current order from the OPERATOR'S CONSOLE.





The voltage dependent current limit is implemented by monitoring the inverter side DC voltage, and compounding it using the measured current to that at the mid–point of the cable. The computed mid–point voltage is then used as input to a non–linear gain in order to modify the basic control characteristic as illustrated below.





X1	Lower input threshold	0.4	
Y1	Lower threshold output	0.55	
X2	Upper input threshold	0.9	
Y2	Upper threshold output	1.0	
GL	Gain below lower threshold	0.0	
GU	Gain above upper threshold	1.0	

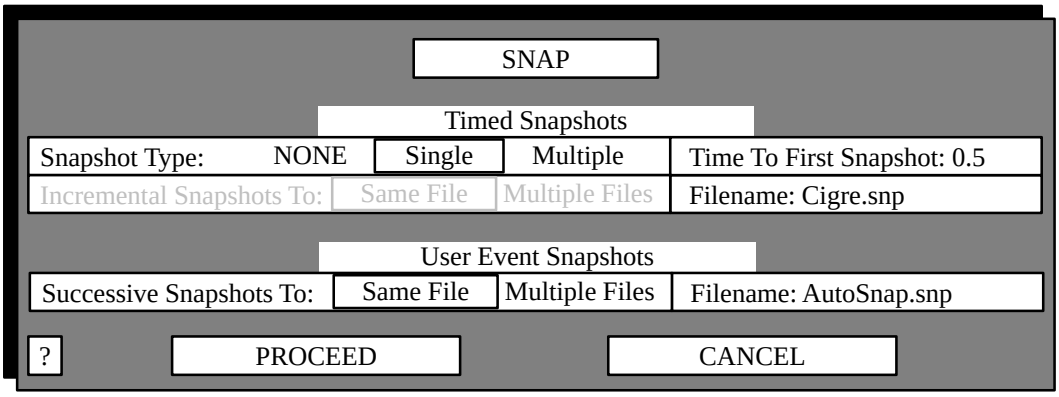
? PROCEED CANCEL

7.4 RUN–UP TO STEADY–STATE OPERATING CONDITIONS

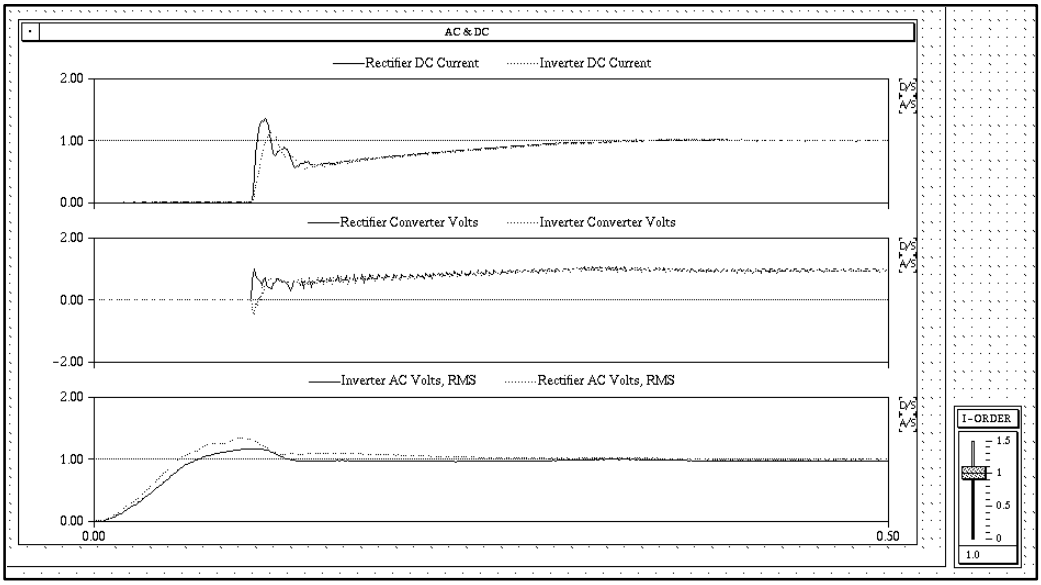
For many power system models, including the one documented here, it may take many cycles before the system reaches its steady–state operating condition. If many different disturbances are to be applied to the system under study, it is inefficient to re–establish steady–state operating conditions for each simulation prior to applying the disturbance.

The PSCAD/EMTDC software permits the taking of a *snapshot* at a pre–determined time. This snapshot feature saves the entire state of the system into a snapshot file. New cases may then be run using the data contained within the snapshot file as the initial conditions. In order to instruct PSCAD/EMTDC to take a snapshot select the SETUP option associated with the SNAP menu on the OPERATOR'S CONSOLE.

A snapshot may also be taken at any time by pressing the "camera button".

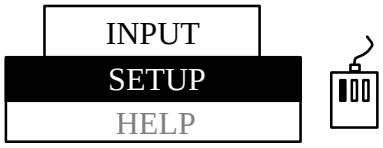


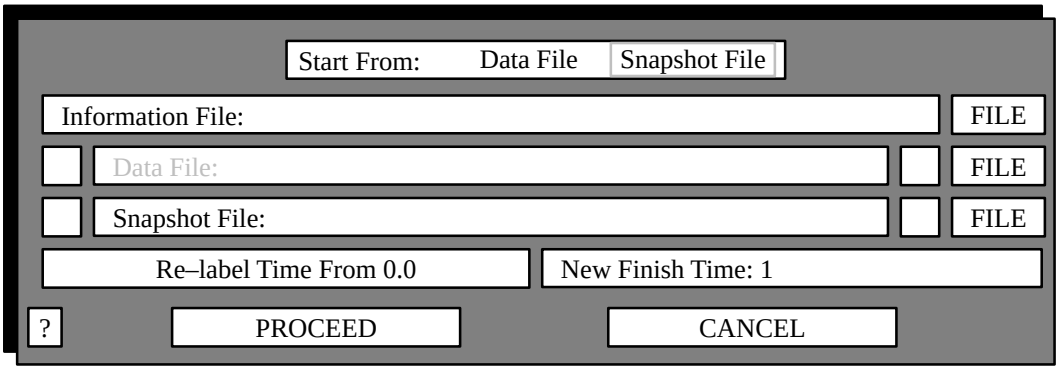
Once the snapshot setup has been defined the case may be started in the normal manner using the OPERATOR'S CONSOLE. The DC voltage and current, as well as ac bus voltages for the startup are shown below.



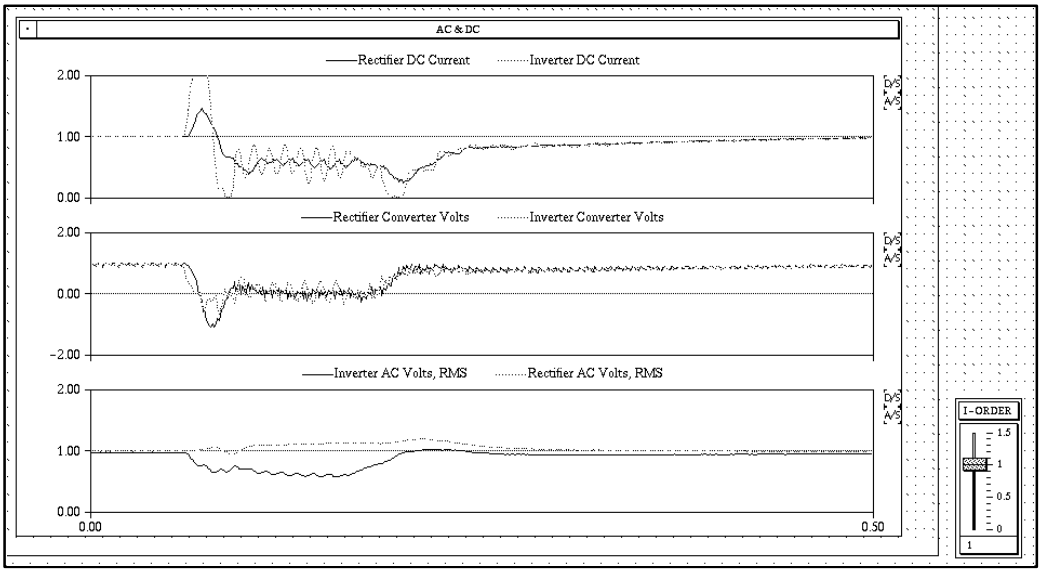
7.5 RUNNING FROM THE SNAPSHOT

To start the CIGRE benchmark model from the steady–state operating condition saved in the snapshot file, select SETUP from the INPUT menu on the OPERATOR'S CONSOLE.





The response of the system to a 5-cycle, single line to ground fault at the inverter bus is shown below.



To apply different faults to the system model, "small changes" may be made to the circuit drawing in DRAFT. A "small change" might be altering the value of a parameter. For instance, the fault duration may be changed; the time that the fault is applied may be altered (although not earlier than 0.5 seconds, the time of the snapshot); the fault type may be changed; and so on.

Large changes to the circuit drawing will invalidate the snapshot. For instance, the circuit topology may not be changed (as in adding/removing branches), and control blocks may not be added or removed.