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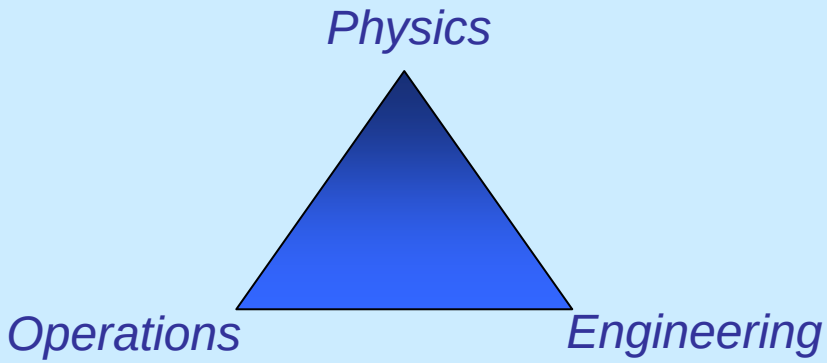
NSTX

PDR for the NSTX Plasma Control System Upgrade

December 15, 2006

Presented by: Paul Sichta

A Team Effort



Agenda

- Introduction
- Hardware & Software Design
- Integration & Test
- Review of CHITS from CDR
- Cost & Schedule

Introduction

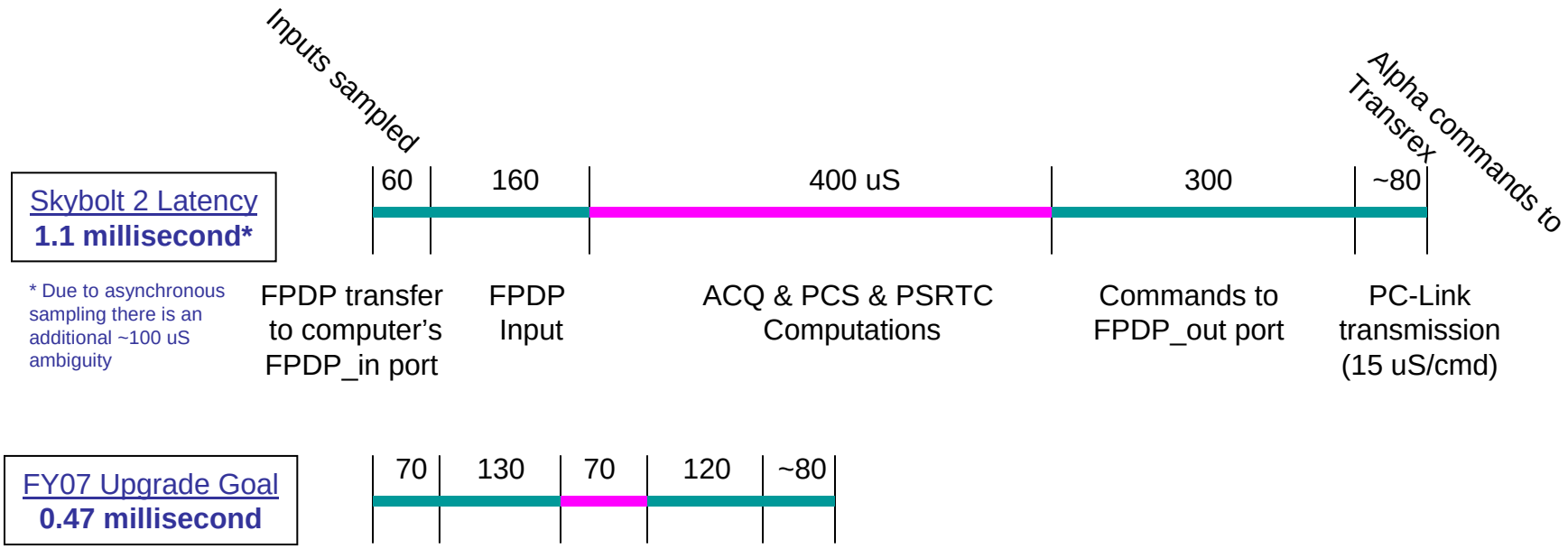
- Justification
- Previous Design Reviews
  - CDR (April ’06)
  - Peer Reviews for FPDP I/O Boards: DITS, FOMD, FOMA (July/August ’06)

Objectives

- Support NSTX research plan:
  - *Do what we do now, only better.*
- Improve RM&A: reliability, maintainability, and availability.
- Facilitate operations.
- Performance and other enhancements will be persued after (initial operations and) the FY07 NSTX campaign.

System Latency Improvement

- Expect an FPDP I/O performance improvement if Vmetro DMA issue is resolved.
- Computation capability expected to improve by a factor of six, e.g. rtEFIT from 12 milliseconds to 2.



RM&A-relevant Project Attributes

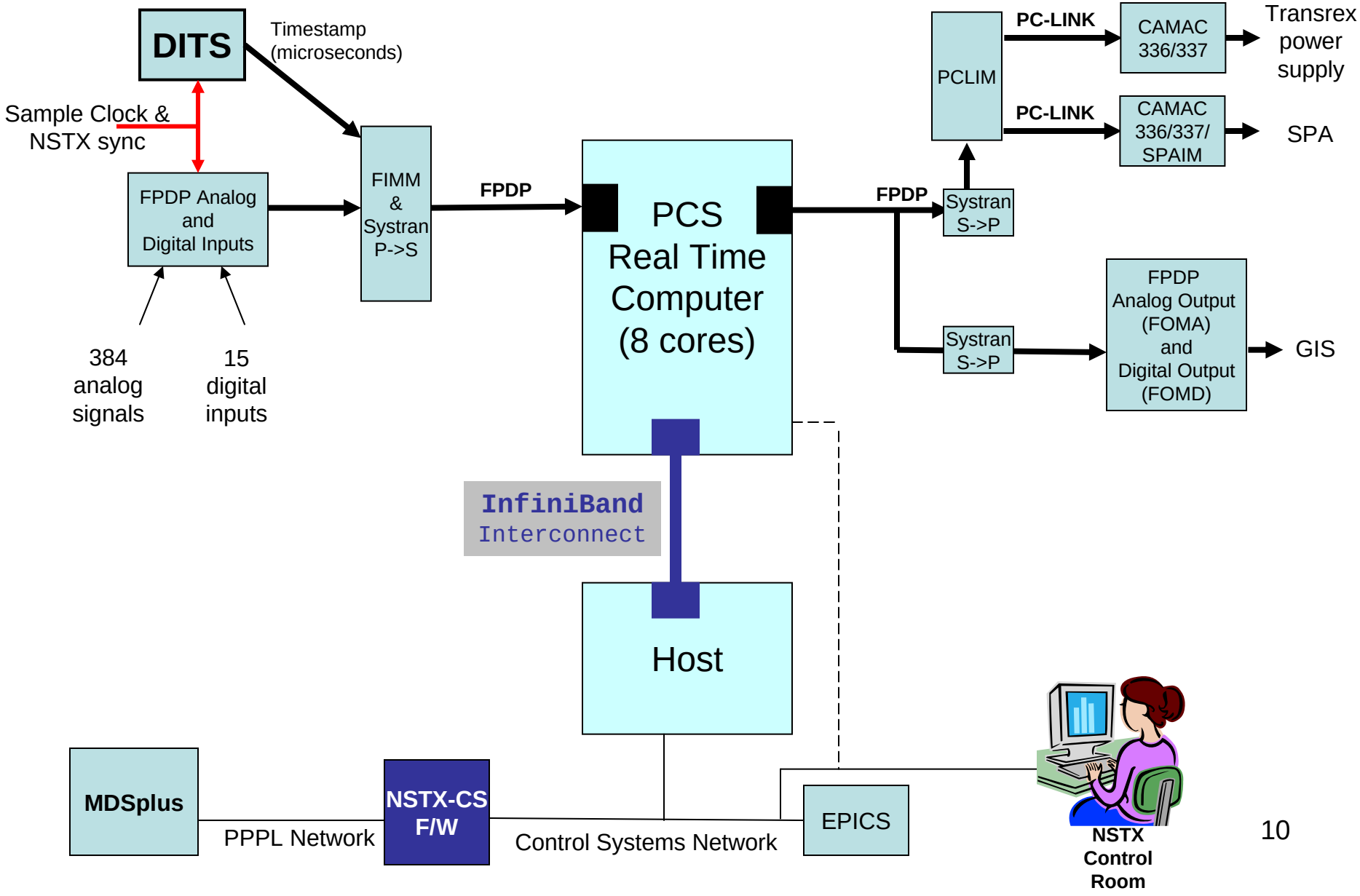
Project Attribute	R Reliability	M Maintainability	A Availability
Commodity Computing Hardware	X	X	X
Drawings & Design specifications	X	X	
Testing	X		
Spare Parts		X	X
HW & SW Support contracts		X	X
GA collaboration	X	X	
FPDP/FPGA/CPLD in-house expertise		X	
FPDP PCI board driver *source code* (Vmetro)		X	
Built-in Diagnostics	X	X	X
Development System	X	X	X

Mitigating operational problems

Problem	Solution
Unavailability of computing hardware and software support; Skybolt vendor ceased business operations.	New system uses commodity parts from leading suppliers. Core technologies are not sole-sourced, or are ‘open’.
ACQ would detect ‘a problem’ with the FPDP data (‘timeout’ problem) stream.	•More ‘visibility’ into the front-end device and data stream. •Independent, development system will also acquire raw FPDP data; available for analysis.
gis_supervisor often crashed overnight	•New program will be rewritten and will include error handling and reporting.
Computing capability lagging *way behind* industry standards, prohibiting world-class performance.	Upgraded computers and technology.

Hardware & Software

Hardware Diagram



Compute Elements

- Replace VME computers with commodity computers.
- Computers in the FCC. Racks borrowed from Unix cluster group.
- InifiniBand network for real-time to host communications.

HP DL385 Proliant Server
(host computer)

Vmetro FPDP I/O

InfiniBand Network

Sun V40Z
(4) dual-core
(realtime computer)

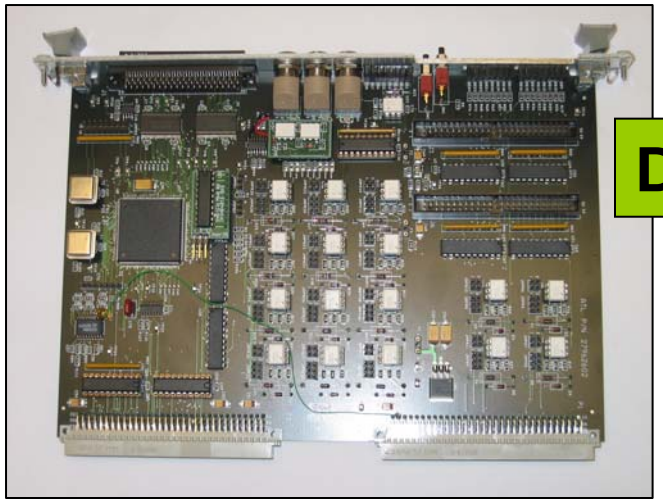
System Input/Output

- Preserve existing FPDP I/O infrastructure
  - 352 channel Data Acquisition.
  - 5 PC-Link interfaces (Transrex, SPA).
- Add time-stamp to the data.
- Replace VME I/O used for Gas Injection with an FPDP solution.
  (7) analog inputs
  (4) analog outputs
  (15) digital inputs
  (22) digital outputs

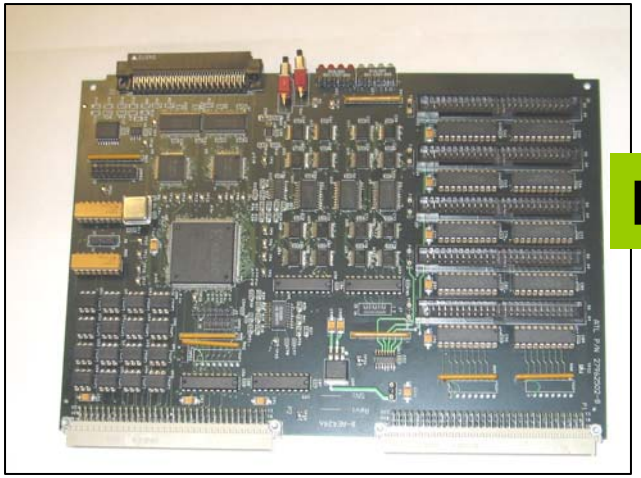
New PPPL-designed FPDP Modules

•FOMA – Analog output (8 chans).
•FOMD – Digital Output (64 bits). Also has 16 Digital Inputs to CPLD.
•DITS – **Digital Input** (48 bits) and **Time Stamp** (microsecond resolution of ADC/SAD sample clock, relative to NSTX Shot Clock).

For each board:
•Peer design reviews held in July, August.
•On-board Xilinx CPLD.
•Documentation:
  •User Guide
  •drawings (family tree, assembly, part list, schematics, printed circuit board, front-panel)
  •CPLD Software Design Document
  •Test Procedure
  •Test-Software Design Document

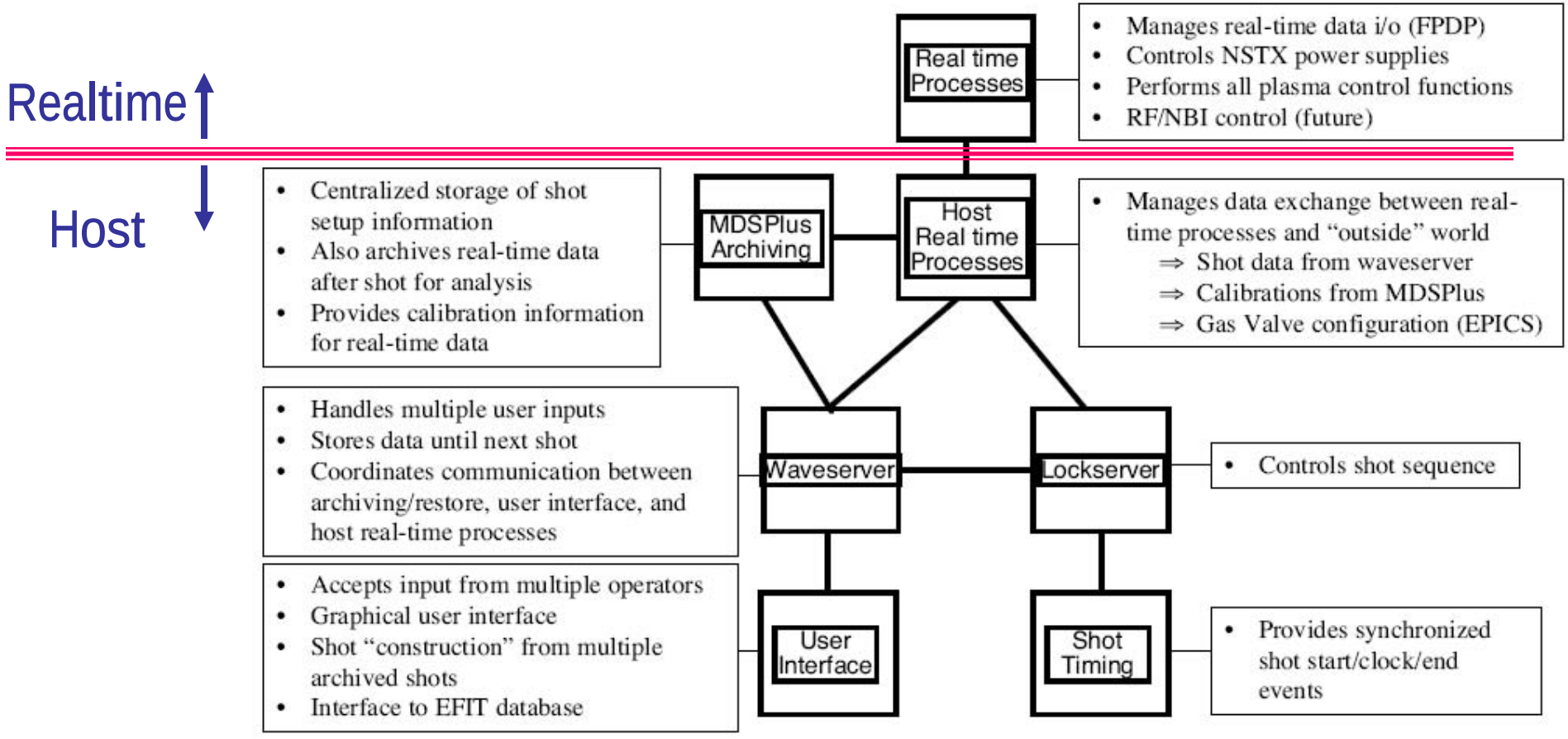


DITS



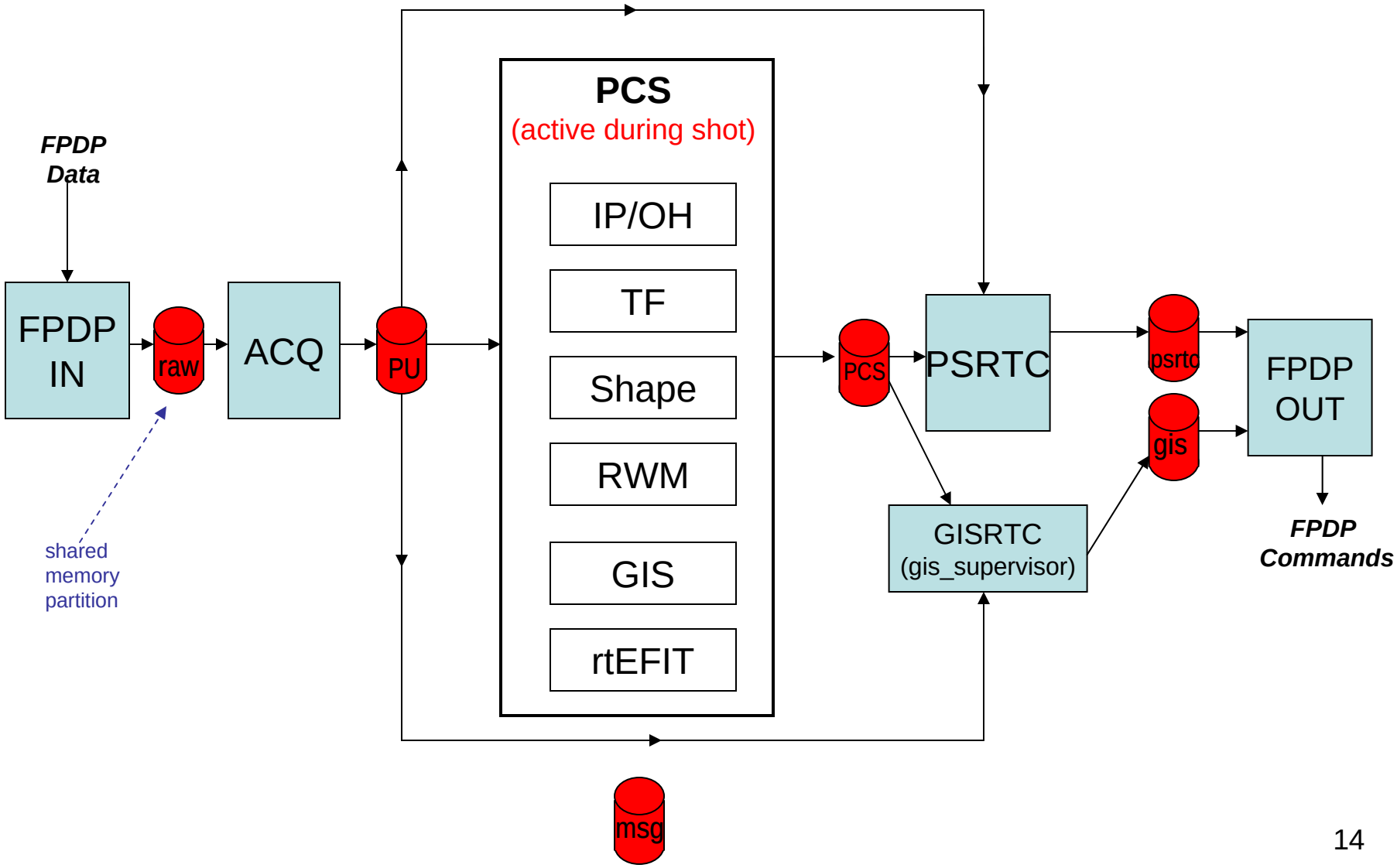
FOMD

Flexible PCS Software Infrastructure



Presented by D. A. Gates At the Fifth IAEA-TM on Control, Data Acquisition, and Remote Participation for Fusion Research Budapest, Hungary July 12-15, 2005

Real-Time Data Flow and Shared Memory Partitions



'global messaging' shared memory partition

Software Tasks

- Port host and real-time software to Linux
  - gis_supervisor (formerly a host program)
  - ACQ
  - PSRTC
  - PCS (GA) infrastructure & algorithm/categories

- Improve reliability & maintainability:
  - Separate data-output from PSRTC.
  - Separate data-input from ACQ.
  - Common program-interfaces using shared-memory.
  - eliminate FORTRAN (PSRTC source in ‘C’).
  - eliminate abandoned IPCS communication client.
  - Improved error detection, handling, and logging.

- Develop a replacement for the Sky’s host-realtime program interface.
- Modify Linux kernel for real-time applications.

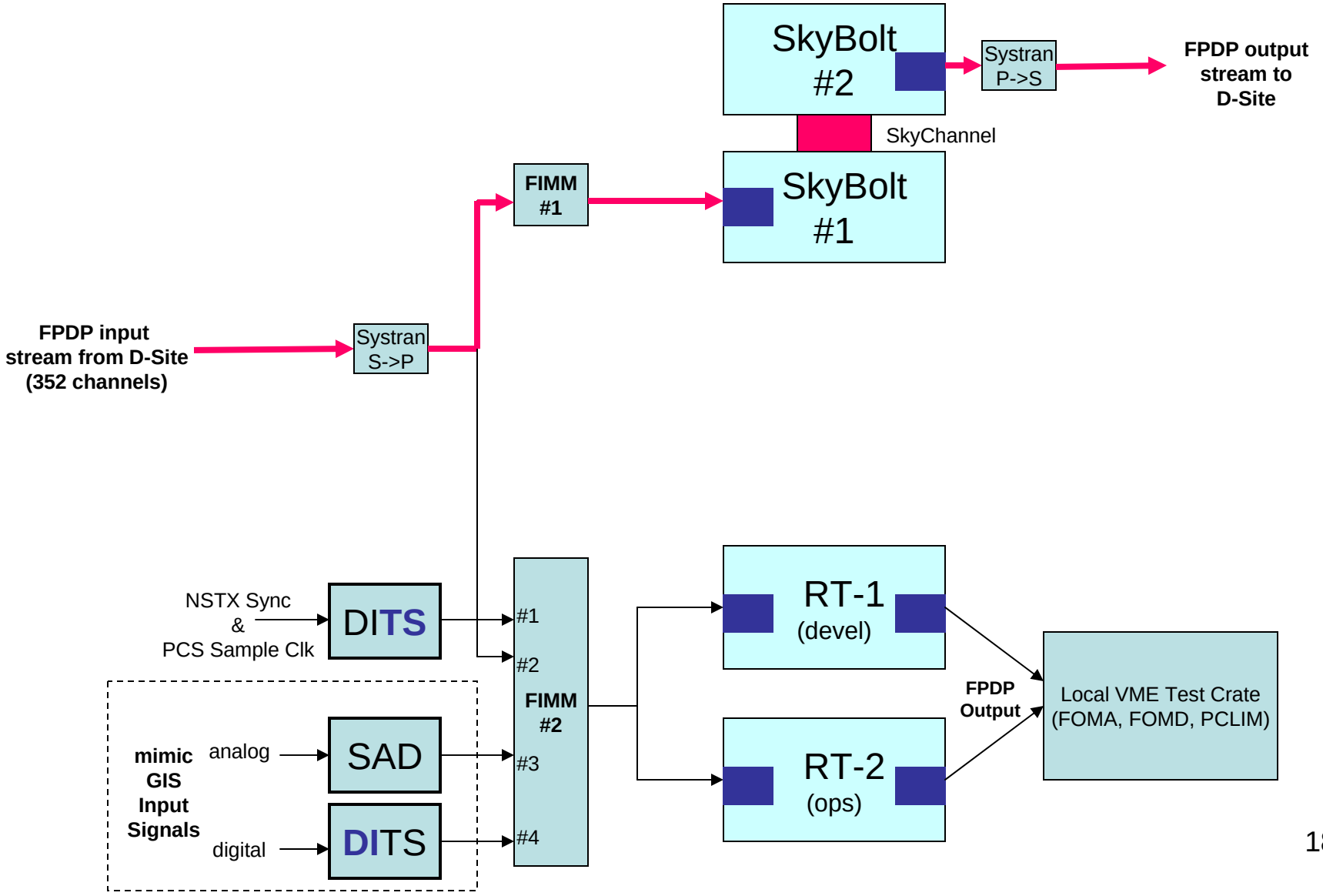
Testing

Testing & Operations

- 41% of labor is for testing.
- A PTP and an ISTP.
  - PTP :
    - communications monitoring & reliability
    - real-time performance measurements
    - ‘piggyback’ testing
    - individual gas valve and rectifier tests (while safed)
    - operator/HMI dry-run
    - challenge error detection/handling/recovery
  - ISTP
    - Follows FDR and PTP.
    - capture ‘output/commands’ for comparison to Sky.
    - Will call for an XMP, with a TBD plan.
    - Expect ~1 run days reserved for the ISTP/XMP.

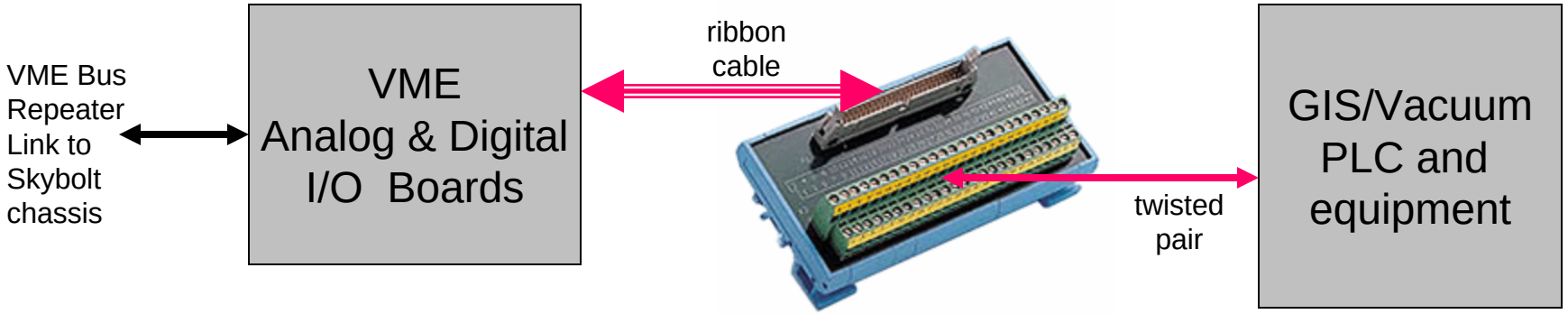
FPDP I/O in the FCC

Temporary arrangement in the FCC to permit simultaneous data acquisition

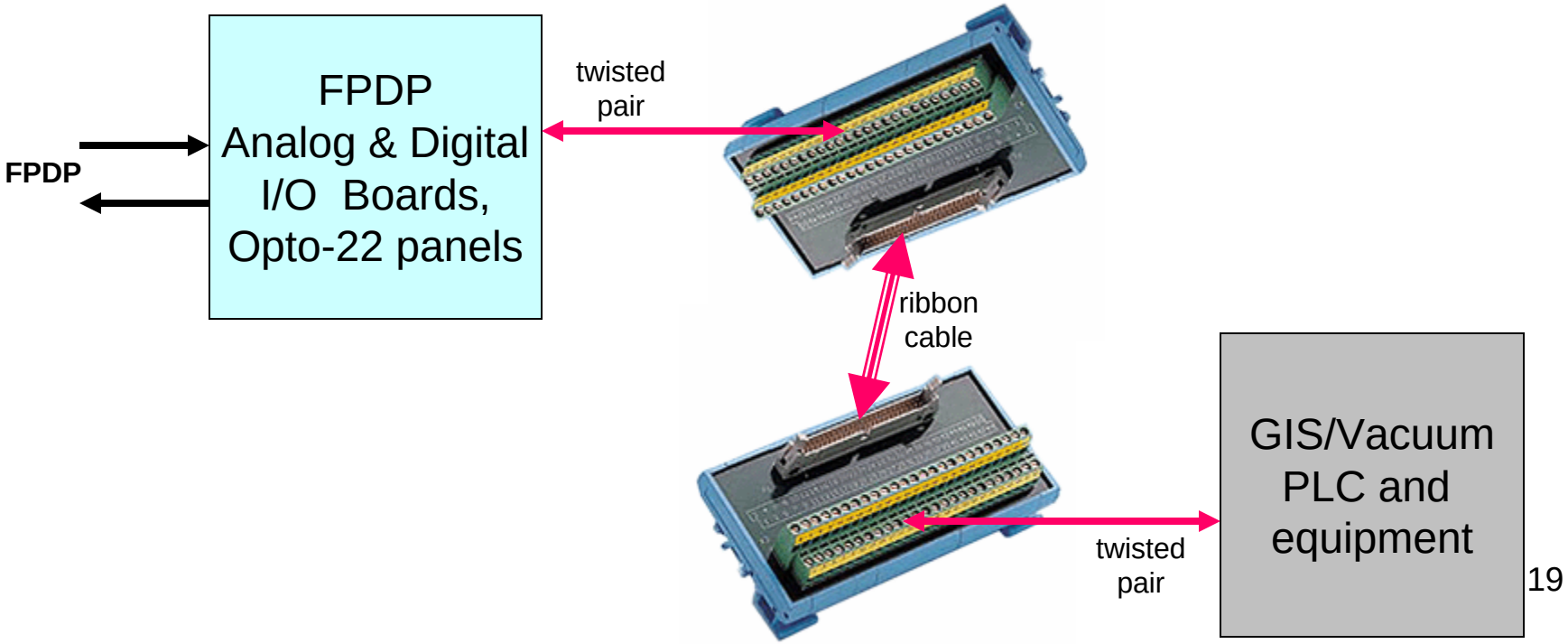


GIS/Vacuum I/O Wiring Conversion Plan

Existing wiring scheme:



New wiring scheme:



CHITS from previous reviews

CHITS from the PCS Upgrade CDR (1)

Chit	Response
Add planned A/C upgrade to the list of hardware requirements.	Air Cond. upgrade not needed.
Consider implications for FPDP i/o boards due to desired future upgrade to the PC Link.	FOMD board can support aspects of this. The in-house CPLD/FPDP technology and expertise are transferrable.
Consider Myrinet instead of InfiniBand for real-time to host communication.	InfiniBand has been prototyped and seems to be acceptable. Other networks/protocols could be looked at for future enhancements.
Consider multi-cpu computer rather than cluster of single-cpu.	Multi CPU (8 dual-cores) selected (Sun v40z) and procured.
Consider shared memory instead of MPI (over InfiniBand) for eal-time interprocess communication.	Shared memory will be used.

CHITS from the PCS Upgrade CDR (2)

Chit	Response
Will a Vmetro interface directly to a Systran (FPDP board).	Yes.
How do we support both the Skybolt and the new system for the Gas Injection?	An FPDP test configuration will allow the GIS FPDP modules to be located in the FCC. The test cell will have a cabling scheme to permit quick change-over between the old and new I/O.
Consider activity to include plasma modeling in testing requirements.	Action (still) pending, per development of the detailed test plan; still worthy of consideration.
Need to quantify resource requirements to have system ready for initial FY07 operations. Or, if that is not possible, then need a plan to introduce capbility during the run.	It is impractical to gather the resources need to support initial ops. The PTP will demonstrate capability during the run.

CHITS from the **DITS** Module Peer Review

Chit	Response
Consider using DITS to drive PIO1 line into computer.	PIO1 and PIO2 lines have configurable in/out direction (jumper selectable).
Move DITS to FCC so that the NSTX FPDP stream can remain unchanged for the Sky, but accessible for the new system.	Done.
Use only one header word.	Done.
Make time stamp 48 bits.	Done.
Consider not reseting block counter.	Block counter ‘reset’ is configurable (jumper selectable).
Consider increasing block counter to 32 bits.	Done.

CHITS from the **FOMA** & **FOMD** Modules Peer Review

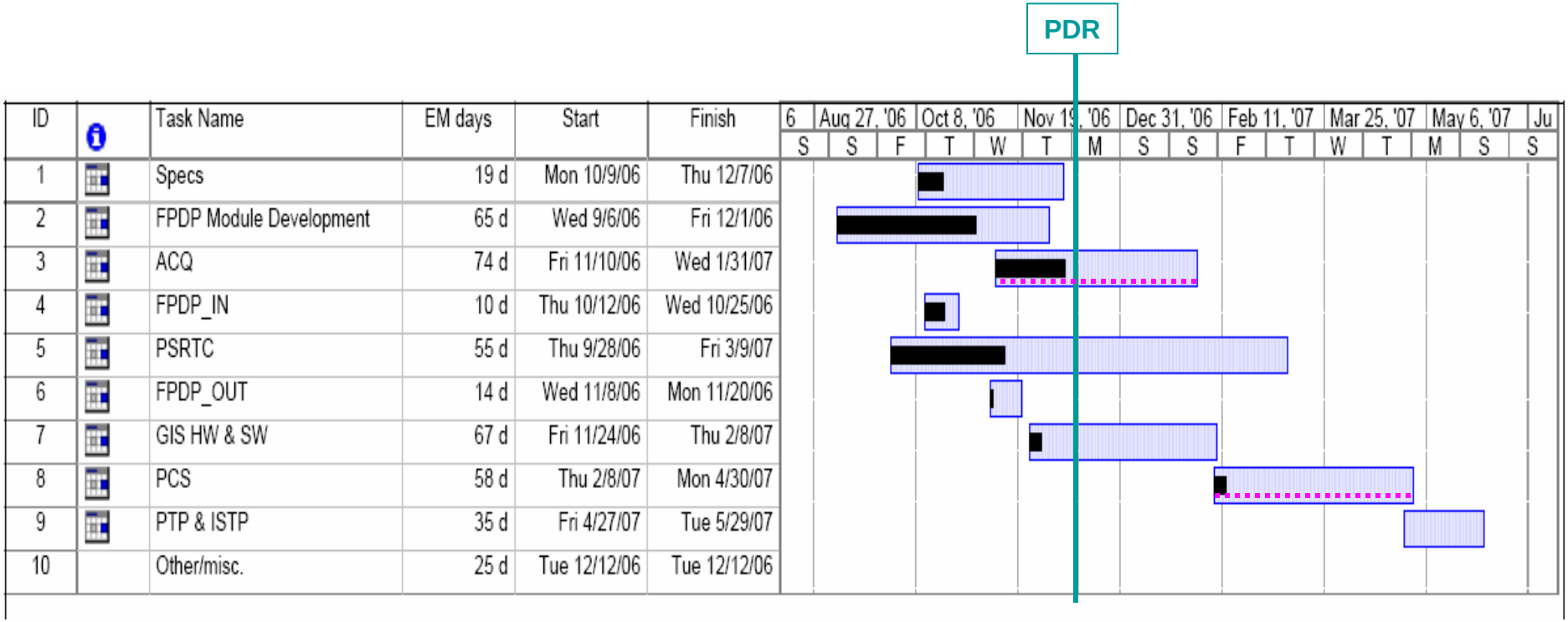
Chit	Response
FOMD: Provide front panel indicator that 5 V power is available on all five i/o banks.	Done.
FOMA & FOMD: Include keep-alive in CPLD (firmware) to reset outputs if not updated in 10 ms.	Keep-alive feature is configurable (jumper selectable). Time is hard-coded in firmware (default: 100 milliseconds, range microseconds thru seconds).
FOMA & FOMD: CPLD should (also) control the internal reset line (DACs and digital registers)	Done.
FOMD: Consider how to use this module to replace the PC Link. Explicitly consider addressing for individual rectifiers.	FOMD can support aspects of that; the CPLD and FPDP technology and in-house expertise is applicable.

Cost & Schedule

Resources

- Labor
  - ~2 year Engineering
  - (3) HW engineers
  - (5) SW engineers
- Jobs
  - X690 for computing
    - $420K total, FY07 loaded
    - $80K M&S unloaded (2 systems)
  - X692 for GIS VME Replacement
    - $260K total, FY07 loaded
    - $50K M&S unloaded

Schedule



- The project is several weeks behind schedule.
- Problems with the Vmetro-supplied driver software delayed Ed and Dana's efforts. Problem not solved, yet.
- Availability of Tina for PSRTC.
- Availability of Sichta for specifications.

Engineering Controls

- Work Planning Form #1296
- RLM: Al VonHalle
- Drawings:
  - ECN (revise) about 15 dwgs.
  - About 30 new dwgs.

Looking Ahead

- Write software specifications to encapsulate the work and define interfaces.
- Recoup lost schedule:
  - Seek ways to offload Dana's ACQ, PCS, and host programming & testing workload (critical-path).
  - Assistance from GA would improve schedule.
- Develop testing plan.
- FDR in March?