JOERGER ENTERPRISES, INC.

MODEL ADC-P

16 CHANNEL HIGH SPEED SCANNING ADC

"NEW"

FEATURES:

- *10USEC. CONVERSION TIME, 6USEC OPTIONAL*
- *12 BIT RESOLUTION*
- *SAMPLE AND HOLD INPUT AMPLIFIER*
- *16 DIFFERENTIAL INPUTS*
- *INTERNAL DATA MEMORY*
- *CONTINUOUS AND SINGLE CYCLE SCANNING MODE*

The Joerger Enterprises, Inc. Model ADC-P is a 16 channel scanning ADC packaged in a single width CAMAC module. It can accept up to 16 differential inputs and scan them continuously, or under program control be switched to a single scan mode. To improve accuracy, the input uses a sample and hold amplifier which holds the analog signal during conversion. A complete conversion cycle takes 10usec. per channel with a 6usec. version available. Three input ranges are available; ±10.24, ±5.12, or 0 to +10.24 volts. These ranges are switch selectable. Bipolar data is in 2's compliment and justified to 16 bits. Identity words are provided that read out the type of module, the input range selected and whether the module is in continuous or single scan mode. The module enters the single scan mode on command, resets itself to channel zero and scans all 16 channels. When in single scan the module can also accept an external, optically isolated trigger that will set the module to zero and cycle through all 16 channels. The converted data is stored in a 16 word data memory. The use of an internal data memory greatly simplifies system operation. The module operates as a complete analog input block, converting data and storing it in memory for readout. Internal logic insures that dataway read cycles and module write cycles never interfere. The analog section is powered by tracking 15 volt regulators to improve performance.

SPECIFICATIONS

ANALOG INPUTS

Channels	*16 differential inputs*
Ranges	*±10.24, ±5.12, 0 to +10.24v internally switch selectable (shipped 0 to +10.24v).*
Resolution	*12 Bits*
Input Protection	*±35 volts crate power on, ±20 volts crate power off.*
Input Impedance	*1M ohms*
Conversion Time	*10usec. per channel, 6usec. optional*
Common Mode Rejection	*50db minimum from D.C. to 1KHZ.*
Absolute Accuracy at 25°C	*±.03% of F.S., ±½ LSB maximum*
Nonlinearity	*±½ LSB maximum*
Temperature Coefficient of Gain	*±50ppm/°C maximum*

CAMAC COMMANDS

N·F0·A$_{0-15}$	*Reads out data from selected channel onto R lines 1-12, bipolar outputs have sign extension to bit 16.*
N·F1·A15	*Reads out ~~the module type~~, the input range and operating mode, continuous or single cycle, and if module is active.*
N·F6·A0	Reads out module type (R7, R9)
N·F24·A0	*Sets module into continuous scan mode.*
N·F26·A0	*Sets module into single scan mode, resets channel address and performs a complete scan of all 16 channels.*
(Z+C)S2 AND POWER UP	*Initializes module and places in continuous scan mode.*
X RESPONSE	*An X response is generated for all valid commands.*
Q RESPONSE	*A Q response is generated for ~~F0 and F1-A15~~* all valid commands.

SINGLE SCAN TRIGGER — *An optically isolated input that will reset the address counter and scan all 16 channels if in the single scan mode.*

VISUAL INDICATORS

"N"	*Module is addressed.*
Active	*Module is scanning.*
Single Scan	*Module is in single scan mode.*

POWER — *±24v, +6v, 8 watts maximum*

SIZE — *Single width CAMAC module.*

INPUT CONNECTOR — *Inputs are on rear printed circuit board. Compatible with Viking 3V18 connector. Front panel connector optional.*

TEMPERATURE RANGE — *0°C to 50°C*

JEI0582

JOERGER ENTERPRISES, INC.

MODEL ADC-P

16 CHANNEL HIGH SPEED SCANNING ADC

The Joerger Enterprises, Inc. Model ADC-P is a 16 channel scanning 12 bit ADC with an internal data memory. It has a cycle time of less than 160 usec corresponding to a per channel conversion of better than 10 usec. To improve accuracy a high speed sample and hold amplifier is incorporated. The module accepts up to 16 differential inputs, scans tham and switches them into a common amplifier. This amplifier is a high input impedance operational amplifier configured with a gain of approximately one. This takes the differential input and converts it to a single ended signal. The output of this amplifier then goes to another amplifier which is used in gain selection. It has two gain settings with a gain of one or two. These are switch selectable with the gain of one being used for ranges $\pm$10V and +10V, and the gain of two for ranges $\pm$5V and +5V. The output of this amplifier feeds a 1 usec sample and hold amplifier which stores the analog signal during conversion. The output of the amplifier goes to a high speed ADC through a range selection switch. Input ranges provided are $\pm$10.24, $\pm$5.12, +10.24 and +5.12 volts. Nine switches are used to select the range. These switches set the analog input into the ADC itself and in addition they select bipolar or unipolar mode, 2's compliment or straight binary output, and range information for readout by F1·A15 to identify the range selected. All nine switches must be set for the module to operate correctly.

The module has two modes of operation, continuous and single cycle. The operating mode can be set under program command or with an on board toggle switch. The unit is controlled by a four bit counter. The standard unit contains a 6 usec ADC and a 1 usec sample and hold and thus can operate easily at the 10 usec scan time used. However, to improve accuracy as much as possible, the multiplexer and memory address are handled separately. When the sample and hold amplifier switches to hold, the ADC is triggered and the multiplexer is switched to the next channel while the memory address remains at the present address for the converted data to be loaded. This then allows the multiplexer, input amplifier and the amplifier in the sample and hold to acquire the new channel while the ADC is converting the last channels information which is stored in the sample and hold. This addressing scheme is accomplished by using an adder in addition to the main address counter. The address counter controls the memories while the output of the adder which has added a one to the address counter controls the multiplexer keeping it one channel ahead.

The data memory is a 16x16 high speed Schottky memory. This internal memory greatly simplifies the use of the module. In continuous mode the module continuously scans the 16 channels and loads the data into memory. When data from one of the channels is required that channel can individually be addressed and the last converted data will be read out. The only disadvantage is that the data may be up to 15 channels (150 usec) old. Because the module must be able to read

out or write into the memory care is taken to insure these cycles do not interfere. This is accomplished by the use of high speed memories and the fact that when a module is commanded to read out, the actual data is recorded by the controller at S1. This is at least 400 nsec after the command is initiated. A portion of this time, 200 nsec, is used by the module to decide when to write into memory. Upon receipt of a read command the module internally delays this signal by 200 nsec before gating out the data. Now if at the end of a conversion there is no read signal present, the module updates the memories which takes 100 nsec. If a read signal is present, the memories are not updated until the read signal is removed. In this way the read and write cycles never appear to the outside world to interfere.

In addition to the continuous scan mode a single scan mode is provided. Command F26 or the on board switch places the unit in single scan. In response to command F26 the module resets the address counter and scans all 16 channels and stops. When the module is in a single scan it can also be triggered externally. An optically isolated input is provided that will also reset the address counter and scan the 16 channels. Function F24, a reset, or the on board switch will place the unit into continuous scan mode.

CIRCUIT DESCRIPTION

The commands used in the Model ADC-P are F0·A0-A15, F1·A15, F6·A0, F24·A0 and F26·A0. Commands F24 and F26 are fully decoded by IC's 5, 6, 7, 8, 12, and 19. These commands are used to trigger the continuous/single flip-flop, IC 31. To decode F0, F1 and F6, IC's 6, 13, 8, 14, and 20 are used. Command F0 with the appropriate subaddress is used to read out data. F1·A15 reads out the status of the module as follows:

R1	MODE	"1"= Single Scan, "0"= Continuous Scan			
R2	ACTIVE	"1"= Module Active, "0"= Module Inactive			
		±10.24v	±5.12v	+10.24v	+5.12v
R3	RANGE	0	1	0	1
R4	RANGE	0	0	1	1
R5	READS ON BOARD SWITCH	"1"= Single Scan, "0"= Continuous/Single Mode			

F6·A0 is used to read out the module identity, which is a "1" on R7 and R9. All commands return both an X and Q response.

The modules address is controlled by a four bit counter, IC25; an adder, IC 23; and a data selector, IC 24. The counter itself controls the memory address. The selector is used to switch the memory address during a data read to the dataway address lines. The adder is used to control the multiplexer address keeping it one channel ahead. When the module is reset either by (Z+C)S2 or when going into single scan the counter is reset to 15 thus placing the multiplexer on Channel 0.

The ADC Busy signal controls the module cycling. The busy signal is gated with the read signal in IC 36 to determine whether the modules memories can be updated at the end of busy. If there is no read signal, the trailing edge if busy will clock flip-flop 37, if there is a read signal present when it goes away it will clock IC 37. The output of this flip-flop is differentiated and loads the memory and triggers the sample mono. This places the sample and hold amplifier in sample for approximately 3 usec to acquire the next channels analog data. At the end of this time the module is placed in the hold mode, the counter is updated and a convert command is sent to the ADC.

In the single scan mode the timing is similar. However, upon receipt of F26 or the external single scan signal the module is first reset by mono IC 38. A short time later flip-flop 31 is set and a trigger is generated to take the first sample. This proceeds as in the continuous mode until channel 16 is complete. At this time IC 37 is clocked causing IC 31 to be reset stopping the scanner.

CALIBRATION

Whenever the input range is changed the modules calibration should be checked. There are two adjustments to be made, they are gain and offset. There are two offset adjustments, one used for bipolar inputs and one for unipolar inputs. For bipolar ranges either ±10.24v or ±5.12v the bipolar adjustment is made with the lowest input level ±½ LSB. For ±10.24v this would be an input voltage of -10.2375v. With this input the pot should be adjusted to read between all zeros on bits 1-11 and all zeros and a "1" in the LSB. Note, bit 12 reads "1" for negative inputs and because of sign extension a "1" will also be on bits 13-16. Next the gain should be adjusted. This is done by putting in the highest level input minus 1½ LSB. For ±10.24v range this would be +10.2325v. With this input the gain pot should be set to read between all "1"'s on bits 1-11 and all "1"'s and a zero on the LSB. For the unipolar input of +10.24v the unipolar offset should be set with an input of +.00125v and the gain set at +10.23625. For the +5.12v range the unipolar offset should be set with an input of +.000625v and the gain set with an input of +5.118125v.

JOERGER ENTERPRISES, INC.

MODEL ADC-P

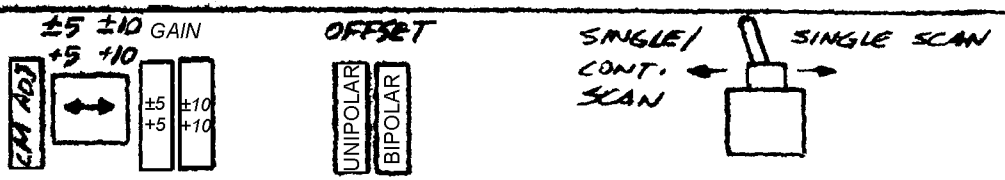
INPUT CONNECTOR

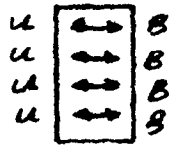
36 PIN P.C. EDGE CONNECTOR

MATING HALF - VIKING 3V18

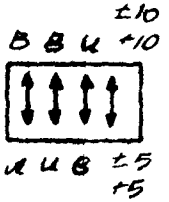
(VIEWED FROM REAR OF MODULE)

Solder Side	PIN #	PIN #	Component Side
CHANNEL 0 RETURN	1A	1B	CHANNEL 0 SIGNAL
" 1 "	2A	2B	" 1 "
" 2 "	3A	3B	" 2 "
" 3 "	4A	4B	" 3 "
" 4 "	5A	5B	" 4 "
" 5 "	6A	6B	" 5 "
" 6 "	7A	7B	" 6 "
" 7 "	8A	8B	" 7 "
" 8 "	9A	9B	" 8 "
" 9 "	10A	10B	" 9 "
" 10 "	11A	11B	" 10 "
" 11 "	12A	12B	" 11 "
" 12 "	13A	13B	" 12 "
" 13 "	14A	14B	" 13 "
" 14 "	15A	15B	" 14 "
" 15 "	16A	16B	" 15 "
GROUND	17A	17B	GROUND
GROUND	18A	18B	GROUND





U ≡ UNIPOLAR
B ≡ BIPOLAR



NOTE: TO CORRECTLY SET THE MODULES INPUT RANGE ALL 9 DIP SWITCHES MUST BE SET.

ADC- 104B

TOP TOGGLE SWITCH SET SCAN MODE, EITHER CONTINUOUS OR SINGLE 16 CHANNEL SCAN

Princeton University Memo

TO: W. Rauch

DATE: 4/16/87

FROM G. Kolinchak
P. Sichta
J. Wertenbaker

SUBJECT: ADC 320 Module dropout problem investigation.

The cause of the NB Stepper Motor problem is beleived to be due to a 320 ADC module problem. The 320 occasionally misread a monitor value which caused the Stepper Motor Control Program to behave erratically.

It was found that out of 100 samples of a channel we would get 5 samples of another channels data. Looking at the "N" line in the crate and the "R12" line we find that the data for another channel may still be valid at "S1", or 400ns into the read cycle. This problem was caused by two areas in the write to memory circuit. A capacitor (C9) which set the duration of the write to memory pulse was 100pf. The schematic shows 68pf for its value. The pulse was 120ns in duration and the problem was aggravated by a delay which was caused by C8. (The C8 delay was 40ns.)

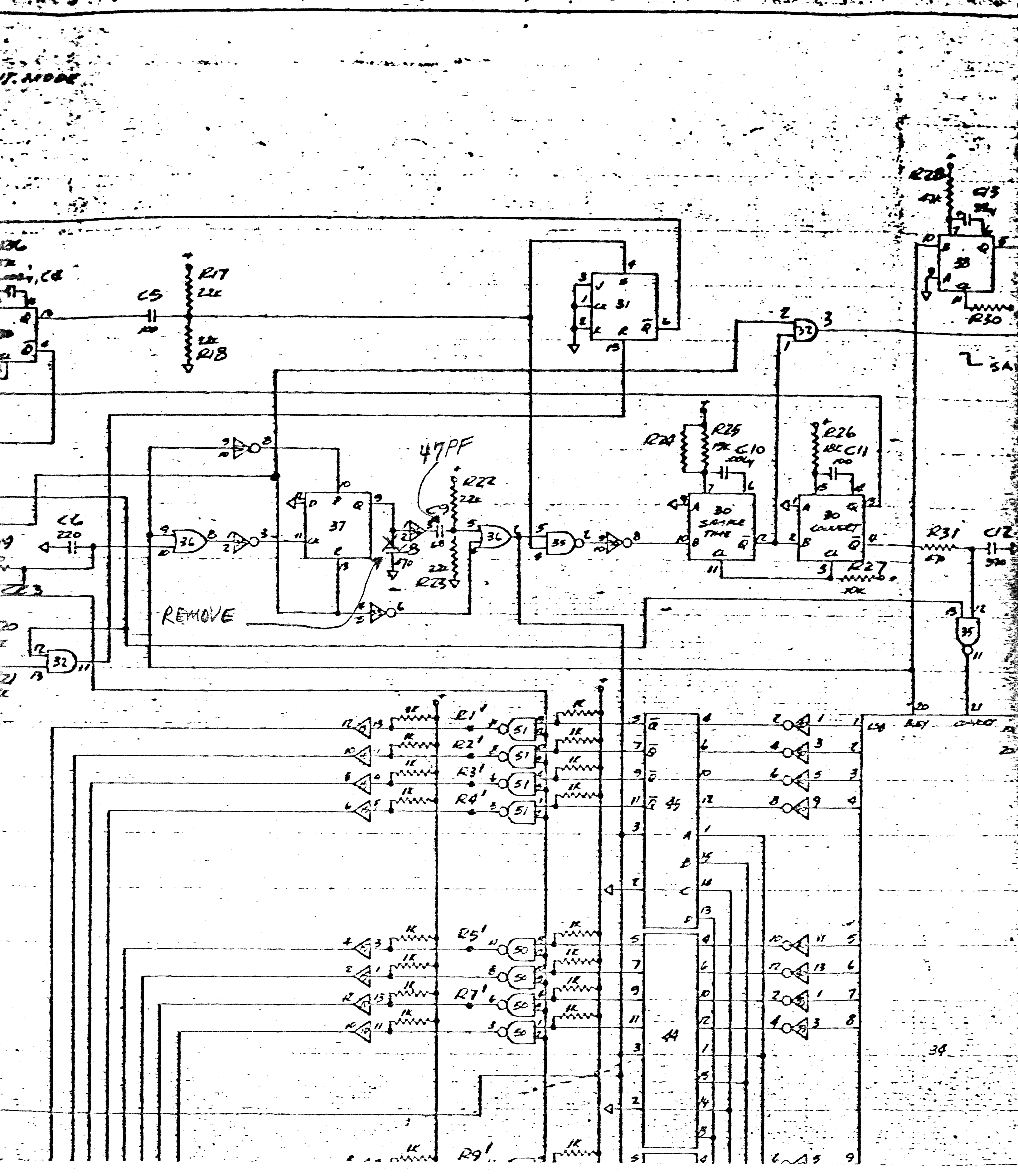
The proposed fix is to change C9 to 47pf which would then give a write memory pulse width of 55ns. The memory specification only requires a 25ns write pulse. Eliminating C8 would give us an additional 40ns safety margin. These changes would ensure a write memory to be completed at 330 ns into the CAMAC read. This leaves a good margin of$\approx$70 before "S1"at 400ns.

Two modules have been modified and tested overnight without detecting any errors.

A plan to modify and replace 320 modules in the field should be investigated and implemented in the near future.

cc: N. Arnold
W. Bergin
H. Feng
R. Gargiulo
S. Hosein
P. Hurst
J. Kampershroer
L. LAGIN
J. McEnerney
J. Montague
G. Oliaro
T. O'Conner
N. Sauthoff
G. Schobert

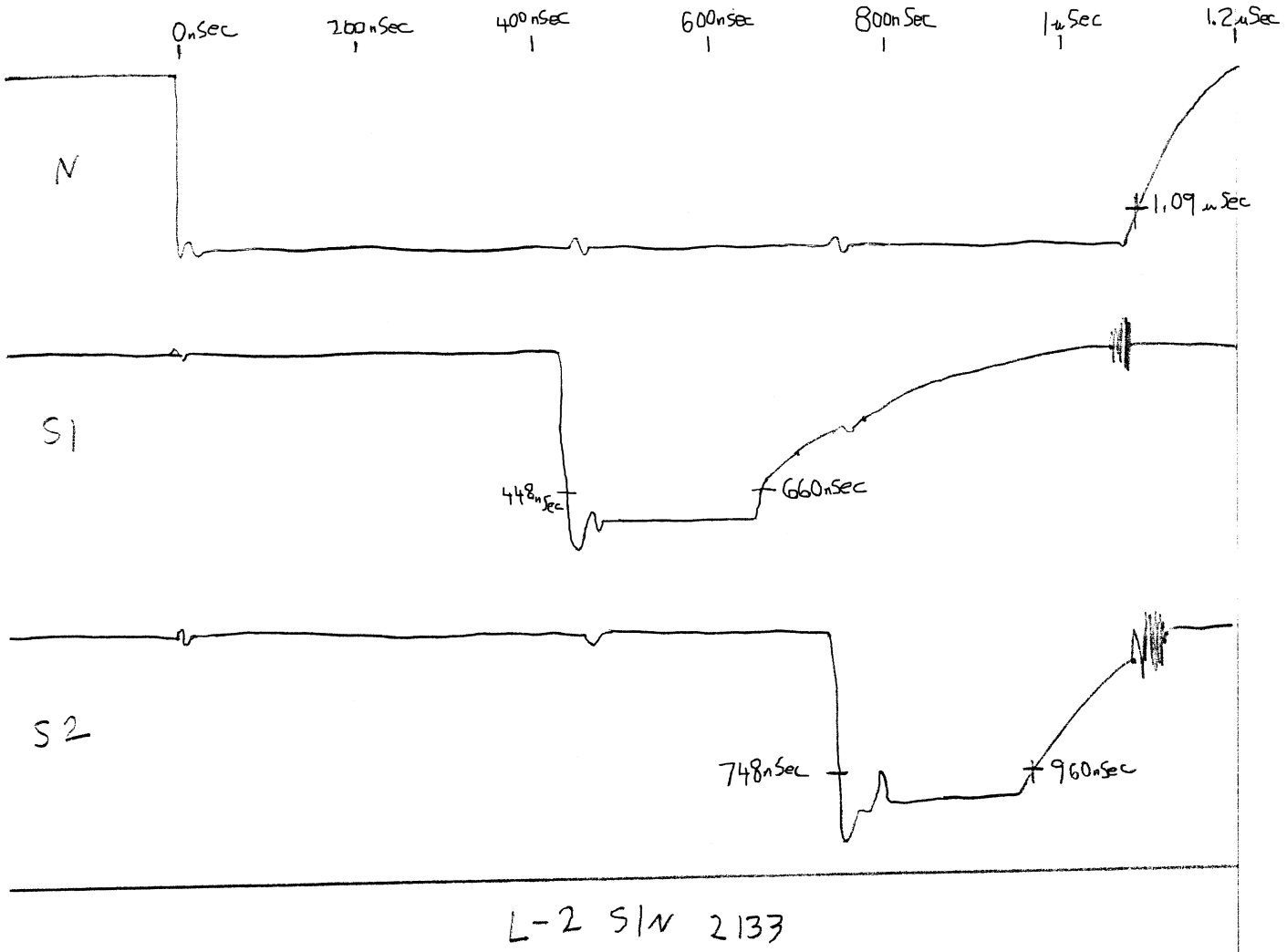
684	2A002880	00000FAE	60
685	2A002880	00000FAE	60
686	2A002880	00000FAE	60
687	2A002880	00000FAE	60
688	2A002880	00000FAE	60
689	2A002880	00000FAE	60
690	2A002880	00000FAE	60
691	2A002880	00000FAE	60
692	2A002880	00000FAE	60
693	2A002880	000008F8	60
694	2A002880	00000FAE	60
695	2A002880	00000FB0	60
696	2A002880	00000FB0	60
697	2A002880	00000FB0	60
698	2A002880	00000FB0	60
699	2A002880	00000FAF	60
700	2A002880	00000FAF	60
701	2A002880	00000001	60
702	2A002880	00000FAF	60
703	2A002880	00000FAE	60
704	2A002880	00000FAE	60
705	2A002880	00000FAE	60
706	2A002880	00000FAE	60
707	2A002880	00000FAE	60
708	2A002880	00000000	60
709	2A002880	00000FAE	60
710	2A002880	00000FAE	60
711	2A002880	00000FAE	60
712	2A002880	00000FAF	60
713	2A002880	00000FAF	60
714	2A002880	00000FAE	60
715	2A002880	00000FAE	60
716	2A002880	00000FAE	60
717	2A002880	00000FAE	60
718	2A002880	00000FAE	60
719	2A002880	00000FAE	60
720	2A002880	00000FAE	60
721	2A002880	00000FAF	60
722	2A002880	00000FAF	60
723	2A002880	00000FAE	60
724	2A002880	00000FAE	60
725	2A002880	00000FAF	60
726	2A002880	00000FAF	60
727	2A002880	00000FAF	60
728	2A002880	00000FAF	60
729	2A002880	00000FAF	60
730	2A002880	00000FAD	60
731	2A002880	00000FAD	60
732	2A002880	00000FAF	60
733	2A002880	00000FAF	60
734	2A002880	00000000	60
735	2A002880	00000FAE	60
736	2A002880	00000FAE	60
737	2A002880	00000FAE	60
738	2A002880	00000FAE	60
739	2A002880	00000FAF	60
740	2A002880	00000FAF	60



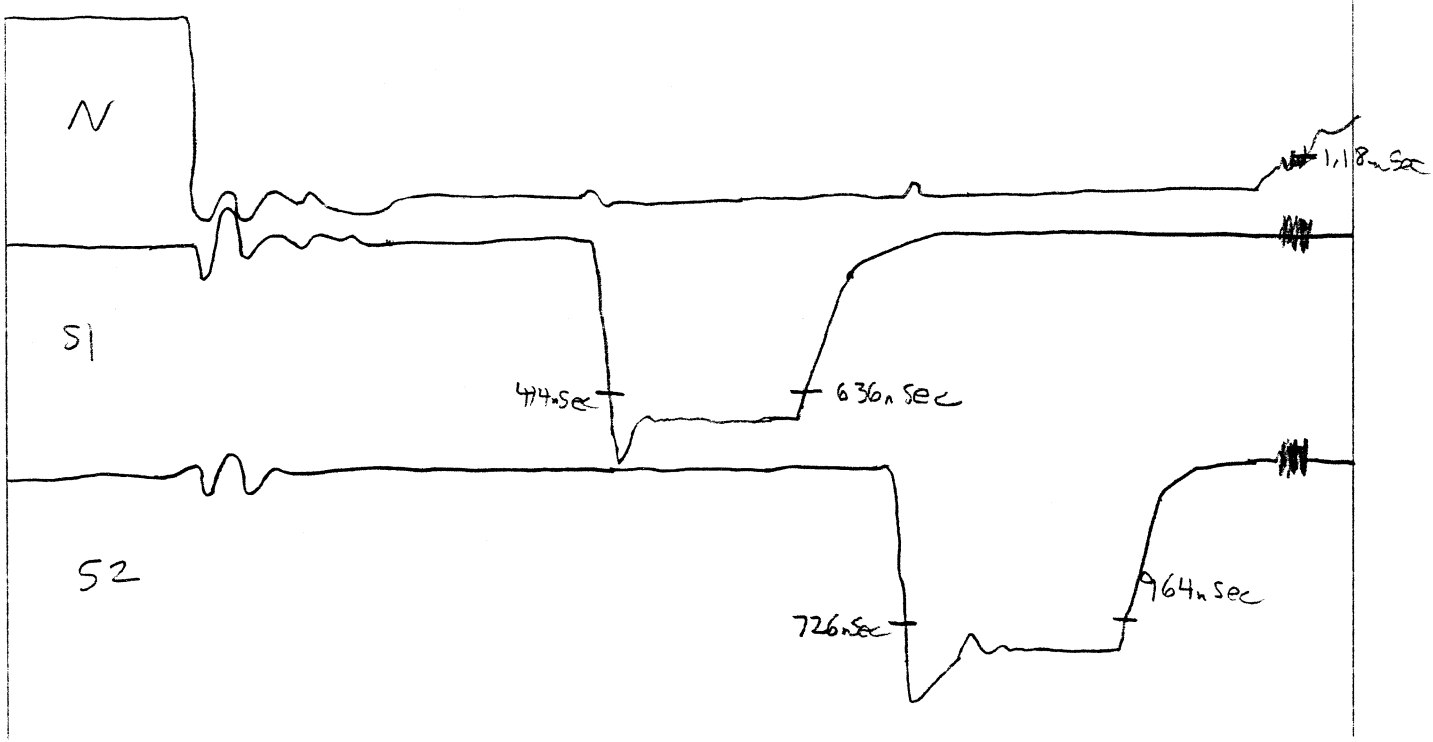
47PF
REMOVE
R17
R18
C5
R22
R23
R24
R25
C10
R26
C11
R27
R28
R30
R31
C12
C6
220
SAMPLE TIME
CONVERT
R1'
R2'
R3'
R4'
R5'
R7'
R9'
45
44
34

Attachment = 367-2

Transiac



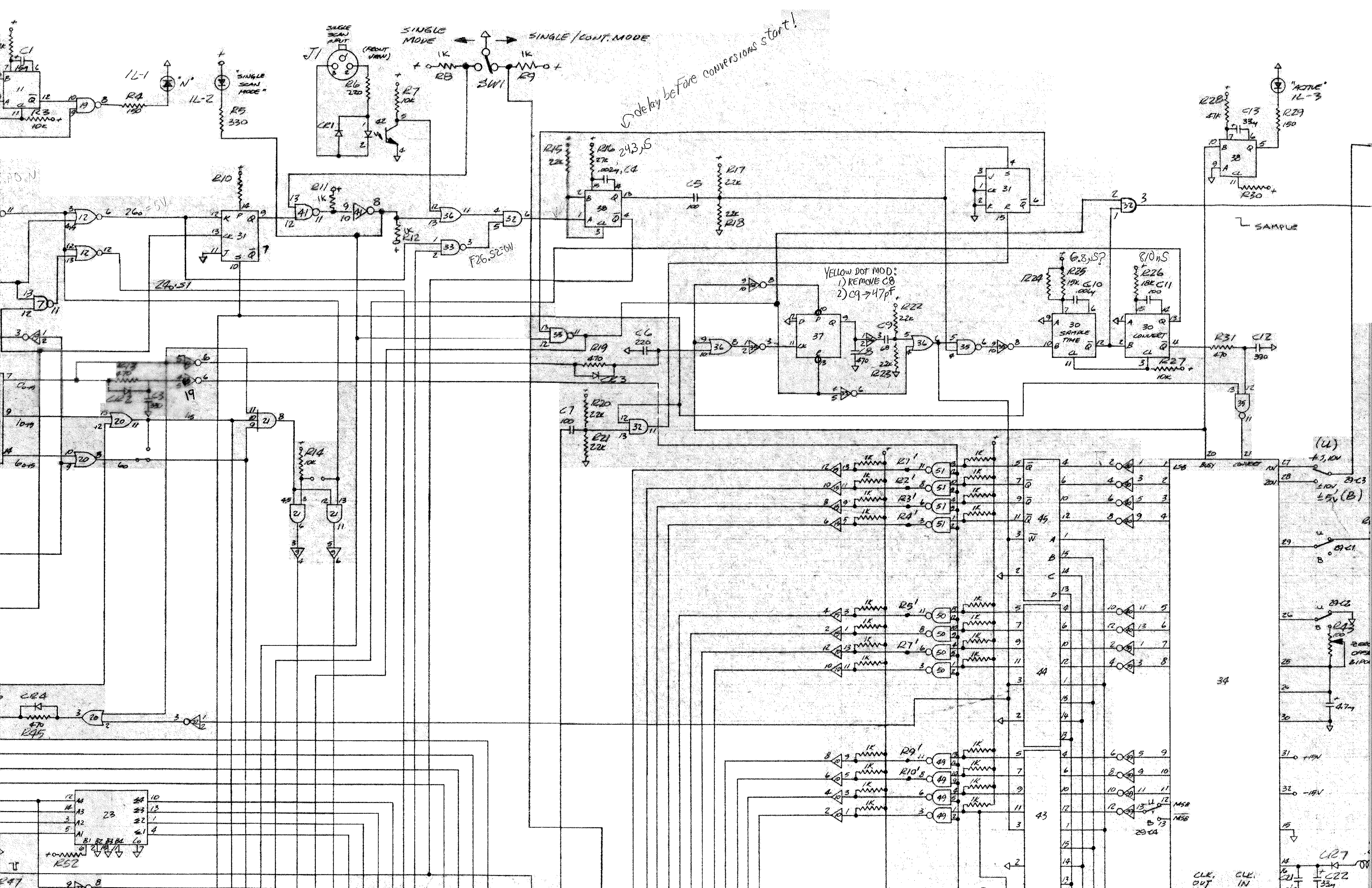
L-2 S/N 2133



3952 Crate controller Timing diagrams referencing S1, S2, and the time the L-2 takes data to the leading edge of the "N" line in slot 10.

Slot 10
Bit 12

S/N	Tdata(ns)	S1 (ns)	S2(ns)	Generation (1old, 4new)	model
1520	435	445		2	S003
2704	555	375		4	S003
3084	550	365	680	4	Z1D
2849	555	365		4	Z1D
2134	390	415		3	Z1B
0372	395	415		1	Z1A
2164	380	405		3	S003
None	560	345			Hsi's board
2133	380	405	730	3	Z1B
2530	545	365		4	S003
2210	380	395		3	S003
1809	410	435		2	S003
1690	420	440		2	S003
1677	420	435		2	S003
2121	400	435		3	not known



SINGLE MODE
SINGLE / CONT. MODE
SINGLE SCAN INPUT
J1
(FRONT VIEW)
R6 220
R7 10K
R8
SW1
R9
1K
CR1
IL-1
"N"
IL-2
"SINGLE SCAN MODE"
R4 150
R5 330
R3 10K
C1
R10
R11 1K
R12 1K
delay before conversions start!
R15 22K
R16 27K
243 nS
C4
C5 100
R17 22K
R18 22K
26₀=5V
24₀.S1
F26.S2=0V
YELLOW DOT MOD:
1) REMOVE C8
2) C9→47pF
R22 22K
C9
C8 470
R23
C6 220
R19 470
CR3
R13 470
CR2
C3
R20 22K
R21 22K
C7 100
R14 10K
R24
R25 15K
C10 .001
6.8 μS?
R26 18K
C11 100
810 nS
30 SAMPLE TIME
30 CONVERT
R27 10K
R31 470
C12 330
R28 47K
C13 33μ
R29 150
"ACTIVE" IL-3
R30
SAMPLE
45
44
43
34
LSB
BUSY
CONVERT
(U)
+5, 10V
±10V
±5V (B)
29-C3
29-C1
29-C2
R43
ZERO OFFSET BIPOLAR
4.7μ
+15V
-15V
MSB
29-C4
CLK. OUT
CLK. IN
CR7
C21
C22 33μ
CR4
R45 470
23
R52
R47

320 ADC MODULE YELLOW DOT MODIFICATION

John Wertenbaker
4/24/00

The following results were obtained with 0 volts on the channel 0 input and 8 volts (Hex C80) in all the other inputs. The module was given an F(0) A(0) command. Ideally, the module should read back 0 volts every time. But it was found that occasionally the module would read back data from another channel.

The data from the unmodified 320 module is subject to change until about 425 nSec after the N line goes active. This is acceptable for most L-2 crate controllers. But, it was found that some L-2 crate controllers clock the readback data later than other crate controllers.

The modification to the 320 module is as follows:

1) Remove C8.
2) Replace C9 with a 47pf capacitor.
3) Verify that C3 is 330pf.
4) Affix a yellow dot to the front panel of the module.

It is best to test the 320 module with L-2 crate controller S/N 2133. This L-2 clocks the data sooner than other L-2 crate controllers, making the problem show up more than others.