TABLE OF CONTENTS

KineticSystems Corporation

Standardized Data Acquisition and Control Systems **3388**

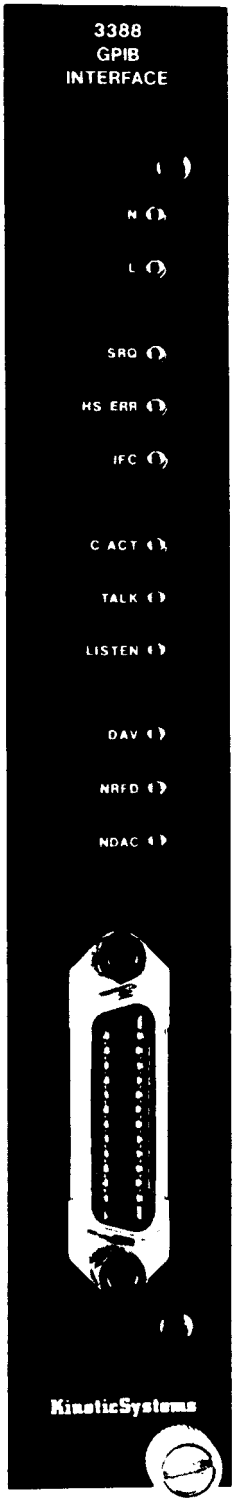
GPIB Interface

FEATURES

- **Provides for interface between a CAMAC system and GPIB-interfaced instruments**
- **Meets IEEE-488 and 583 requirements**
- **Provides GPIB T8, L4, C1 - C4, C25, SH1, AH1, SR0, RL0, PP0, DC0, DT0 interface functions**
- **GPIB T6, SR1, DC1, C5 - C24 interface functions can be implemented by additional user software**
- **Switch-selectable talk/listen address**

APPLICATIONS

- **Interface GPIB (IEEE-488) instruments to CAMAC (IEEE-583)**
- **Instruments such as DVMs and counters interfaced to a computer**
- **Data loggers**



GENERAL DESCRIPTION

The Model 3388 is a double-width CAMAC module providing the interface between a CAMAC system (IEEE Standard 583 - 1982) and the General Purpose Interface Bus (also called "GPIB" or "ASCII Bus," IEEE Standard 488). This module allows digital multimeters, counters, printers, calculators, display terminals, and other devices meeting the GPIB standard to be connected to a CAMAC system. In the past, interfacing such instruments to CAMAC often required special modules and engineering effort on a case-by-case basis. With the 3388, up to 14 other GPIB-interfaced instruments can be connected via standard GPIB cables.

The 3388 GPIB Interface module functions as a CONTROLLER, TALKER, and LISTENER as described in IEEE Standard 488. For example, while in the LISTEN mode itself, the 3388 can cause a digital multimeter to be in the TALK mode. The DMM then transmits data to the 3388 to be processed by the computer associated with the CAMAC system. The computer can then cause the 3388 to be in the TALK mode and a GPIB-interfaced printer to be in the LISTEN mode. Processed data from the computer can then be printed.

The 3388 can be set to the CONTROLLER IDLE state so that it can be a TALKER or LISTENER in a system containing another CONTROLLER (such as an intelligent terminal or a desk-top calculator).

GPIB SPECIFICATION SUMMARY

Item	Description
Interconnected Devices:	Up to 15 maximum on one contiguous bus
Interconnection Path:	Star or linear bus network up to 20 meters total transmission path length
Active Signal Lines:	Sixteen total: eight data lines, three data transfer control lines, and five bus management message lines
Message Transfer Scheme:	Byte-serial, bit-parallel, asynchronous data transfer using interlocked three-wire handshake technique
Data Rate	Depends upon host computer program and external devices
Address Capability:	Primary addresses, 31 TALK and 31 LISTEN

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FUNCTION CODES

Command		Q	Action
F(0)·A(0)	RD1	IRDY	Reads the Input register and clears the Input LAM status bit. (See Note 1.)
F(1)·A(0)	RD2	1	Reads the Status register.
F(1)·A(12)	RD2	1	Reads the LAM Status register.
F(1)·A(14)	RD2	1	Reads the LAM Request register.
F(8)·A(15)	TLM	LR	Tests whether a LAM request is present.
F(16)·A(0)	WT1	ORDY	Writes the Output register and clears the Output LAM status bit. (See Note 2.)
F(17)·A(13)	WT2	1	Writes the LAM Mask register.
F(23)·A(12)	SC2	1	Selectively clears the LAM Status register.
F(24)·A(0)	DIS	1	Disables the Attention control signal.
F(24)·A(1)	DIS	1	Disables the Remote Enable control signal and clears LAM 4.
F(24)·A(2)	DIS	1	Disable the End or Identify control signal.
F(24)·A(3)	DIS	1	Disables the Service Request control signal.
F(24)·A(4)	DIS	1	Disables the Universal and Addressed command inhibit.
F(25)·A(0)	XEQ	1	Executes the Interface Clear control signal. (See Note 5.)
F(26)·A(0)	ENB	1	Enables the Attention control signal.
F(26)·A(1)	ENB	1	Enables the Remote Enable control signal.
F(26)·A(2)	ENB	1	Enables the End or Identify control signal.
F(26)·A(3)	ENB	1	Enables the Service Request control signal.
F(26)·A(4)	ENB	1	Enables the Universal and Addressed command inhibit.
F(27)·A(0)	TST	IRDY	Tests whether the Input LAM status bit is set.
F(27)·A(1)	TST	ORDY	Tests whether the Output LAM status bit is set.
Z	CZ	0	Clears the Input register, the LAM Status and LAM Mask registers, and puts the interface in a known state.

Notes: 1. Q = 1 for Input data ready, Q = 0 otherwise.
2. Q = 1 for Output data ready, Q = 0 otherwise.
3. F(24)·A(5 - 15) and F(26)·A(5 - 15) reserved for future use (Q = 1, X = 1 response given).
4. X = 1 for all valid addressed commands.
5. READY (or LAM 4) is false during IFC and is set true on completion of IFC.

POWER REQUIREMENTS

+6 volts — 610 mA

ORDERING INFORMATION

Weight: .56 kg. (1 lb. 4 oz.)

Model 3388-D1A — GPIB Interface with IEC (Europe) proposed Standard Connector (25-contact "D" connector)

Model 3388-G1A — GPIB Interface with IEEE-488 - 1975 (USA) Standard Connector (24-contact ribbon connector with metric hardware)

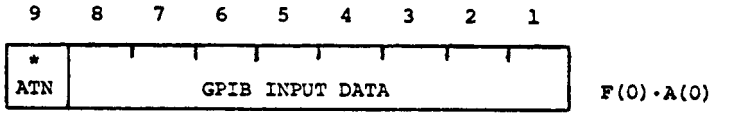
Accessories — Model 5852-Axyz, Cxyz, or Exyz-Series Cable Assemblies (Model 3388-D1A)
Model 5864-Series Cable Assemblies (Model 3388-G1A)

STATUS REGISTER (READ ONLY)

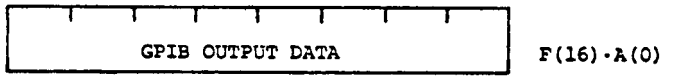
BIT	LABEL	DESCRIPTION
7	ATN	The Attention signal is being received true.
6	HS ERR	The Handshake Error condition true.*
5	SRQ	The Service Request control signal is true.
4	Ready	The module is ready to output data to the GPIB bus.
3	EOI	The End or Identify control signal is true.
2	MTA	The module is in the talker addressed state.
1	MLA	The module is in the listener addressed state.

*HS ERR = NRFD and NDAC control signals false when the DAV control signal is true.

REGISTERS

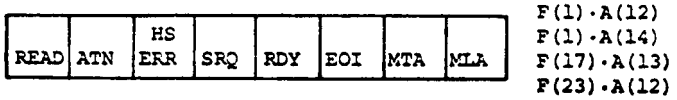


INPUT DATA REG



OUTPUT DATA REG

STATUS REG



LAM STATUS REG

* Strap selectable

BIT**	LABEL	DESCRIPTION
8	Read	The interface is waiting to complete the handshake until a CAMAC data read is done.
7	ATN	Attention control signal detected.
6	HS ERR	Handshake error condition detected.*
5	SRQ	Service Request control signal detected.
4	Ready	Action due to previous commands completed and the Bus is not busy.
3	EOI	End or identify control signal detected.
2	MTA	My Talk Address detected.
1	MLA	My Listen Address detected.

*HS ERR = NRFD and NDAC handshake control signals false when the DAV control signal is true.

**These bits represent edge triggered latches and thus indicate that the condition occurred at least once since the last time that bit was cleared.

LED INDICATORS

N	Flashes when the module is addressed.
L	On when the L signal is true.
SRQ	On when the Service Request control signal is true.
HS ERR	On when the Handshake Error condition is true.
IFC	Flashes when the Interface Clear signal is true.
C ACT	On when the Attention control signal is asserted by the module.
TALK	On when the module is in the Talker Addressed state.
Listen	On when the module is in the Listener Addressed state.
NRFD	On when the Not Ready for Data handshake signal is true.
NDAC	On when the No Data Accepted handshake signal is true.
DAV	On when the Data Available handshake signal is true.

OPERATION

In most applications the Model 3388 will be the system controller and instruments such as DVM's, counters, printers, etc. will be controlled via the GPIB. An extensive LAM status register and status register are included to simplify programming. Eleven front-panel LED's provide the programmer or user with valuable information about the current state of the interface. The read and write data are each packed in the lower eight bits of the CAMAC data words. This allows for easy ASCII representation in high level languages.

Since all GPIB data and command transfer operations use the three-wire handshake, the data transfer waits until the associated devices are ready for that byte transfer. Therefore the 3388 LAM status register can be used to minimize the software overhead.

When the 3388 is used in a system where it is the system controller, it can assert the "controller" GPIB control signals. In this application the F(26)·A(3) command (enabling the Service Request control signal) would not be used. This is used by the other devices on the bus to "signal" the controller. If the 3388 is not used as the system controller, it can request service, but it would not use the F(25)·A(0), F(26)·A(0) or F(26)·A(1) commands.

The GPIB control signals are available to the CAMAC system via enable/disable and Execute commands and bus status is monitored by LAM and Status registers.

For GPIB command or data byte transfers, the CAMAC write command Q response is determined by the completion of GPIB action previously initiated. When the module is acting as the system controller or is the current talker, it is available to send GPIB command or data bytes, respectively. When a command or data byte is accepted by the module (Q = 1 to the write command) the Ready LAM is cleared. Until all of the listeners on the bus have accepted the byte, there will be a Q = 0 response to any data write commands. Upon completion of the handshake cycle, the Ready LAM will be set and a Q = 1 response will result on the next write command. The Ready LAM and Q response are affected by certain control signals. An example is the Interface Clear (IFC) signal, which is asserted by an Execute command. When the module accepts the Execute command, the Ready LAM is cleared and Q to the write command is blocked. The IFC signal is asserted for 150 s. At the end of this time, the Ready LAM is set and Q = 1 response will result in the next write command.

The Read LAM is set when the module is an active listener and a valid data byte is available to it or when the Universal and Addressed Command Inhibit is disabled and a universal or addressed command is being sent to it. The Read LAM being true indicates that a valid byte is waiting to be accepted by the module. The handshake is held until the next CAMAC data read. The Read LAM is cleared by the CAMAC read and a Q = 0 response to future data read commands will result until a new byte is available.

GPIB ADDRESS

The 5-bit GPIB address for TALK and LISTEN on the 3388 is set by the switch on the 3388 PC card. See the STRAP AND SWITCH OPTIONS sheet for details.

THE GPIB THREE WIRE HANDSHAKE

The GPIB handshake operate automatically between the 3388 and other devices on the GPIB bus. A discussion is presented here to provide the user with a better understanding of its operation.

The three wire handshake consists of three low true signals, DAV (data available), NRFD (not ready for data) and NDAC (no data accepted). A typical handshake sequence is shown below. During Period 1, DAV is false and NRFD and NDAC are true. The device which is an active talker at this time must wait until all devices on the bus stop asserting NRFD true. Period 2 shows NRFD false, indicating that all devices on the bus are ready for data. The currently active talker can now set DAV true and send another data byte. This occurs during Period 2. All of the handshake signals are true during Period 3. At this point, the active talker is waiting for all of the listeners to stop asserting NDAC. At the beginning of Period 4, all active listeners have stopped asserting NDAC, indication that they have all accepted the data byte. The active talker senses this and releases DAV. When the active listeners sense DAV false, they again assert NDAC true. The handshake sequence is now completed and another cycle can begin as soon as all of the active listeners stop asserting NRFD.

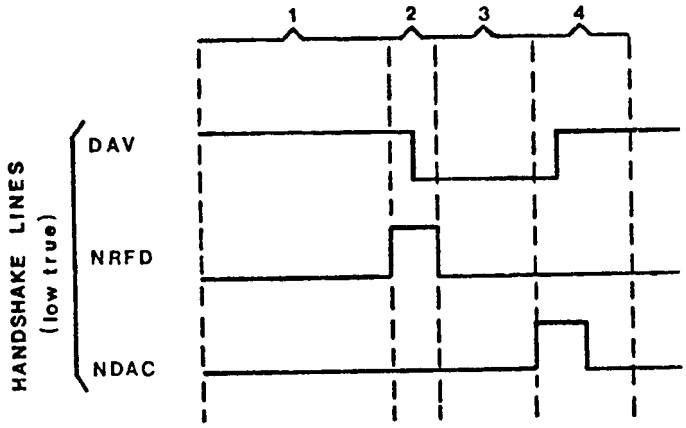


FIG. 1 Handshake Sequence

INTERACTION OF THE MODEL 3388 WITH THE THREE WIRE HANDSHAKE

When the 3388 is an active listener (MLA true), the Read LAM status bit will be set when DAV is sensed true. The handshake sequence is held in Period 3 until the next CAMAC read. The Read LAM is cleared by the CAMAC read and the module will stop asserting NDAC. When all other active listeners have stopped asserting NDAC, the handshake will move to completion.

TAKE CONTROL AND DATA ACQUISITION EXAMPLE (See Figure 2).

Command

#1 F(25)·A(0) Execute IFC. Q Response = 1.

Interface Clear (IFC) is pulsed low (true) for approximately 150 microseconds. This initializes all instruments on the bus.

#2 F(26)·A(0) Enable ATN. Q Response = 1.

Attention (ATN) is set to its low (true) state. This prepares all instruments to receive command instructions from the controller.

#3 F(26)·A(1) Enable REN. Q Response = 1.

Remote Enable (REN) is set to its low (true) state. This prepares all instruments with remote-local capability to enter the remote state upon receiving their listen addresses.

#4 F(26·A(4) Enables the Universal and Addressed command inhibit. Q Response = 1

This allows the 3388 to send or receive Universal or Addressed commands with no special treatment. Since the 3388 is the system controller, the Universal and Addressed commands are already handled by software. This command should be sent as part of the "start-up" sequence whenever the 3388 is the system controller.

#5 F(16)·A(0) Send command data. Q Response =1.

Send the instrument's listen address to put it in the remote mode and ready for data when ATN is false.

#6 F(16)·A(0) Send command data. Q Response = 0.

The data was not transmitted on the bus because the last transmission had not been accepted by all instruments yet. (Q Response = 0.) Note that the Ready Status bit was not true when the command was executed.

#7 F(16)·A(0) Send command data. Q Response = 1.

Send the 3388's talk address. It can now send data when ATN is false.

#8 F(27)·A(1) Check the state of output ready. Q Response = 1.

The last command data transmission has been completed.

#9 F(24)·A(0) Disable ATN. Q Response = 1

Attention (ATN) is set to its high (false) state. Now the bus is ready for data exchange between the presently active Talker and Listener.

Command

#10 F(16)·A(0) Send data. Q Response = 1.

Send data to instrument. For example, send range setting to voltmeter.

#11 F(16)·A(0) Send data. Q Response = 0.

Last transmission not completed. (Q Response = 0.)

#12 F(16)·A(0) Send data. Q Response =1.

Repeat command #11 until Q Response = 1 received. The data has now been transmitted.

#13 F(27)·A(1) Check the state of output ready. Q Response =1.

The last data transmission has been completed.

#14 F(26)·A(0) Enable ATN. Q Response = 1.

Attention (ATN) is set to its low (true) state. All instruments are now ready to receive command data.

#15 F(16)·A(0) Send command data. Q Response = 1

Send instrument Talk address. This enables the instrument to send data and causes the 3388 to leave the Talk Addressed state.

#16 F(16)·A(0) Send command data. Q Response = 1.

Send the 3388's Listen address. The 3388 will be ready to accept data sent out by the instrument.

#17 F(27)·A(1) Check the state of output ready. Q Response = 0.

The last command data transmission has not been completed. Note that the Ready status bit was not true when this command was executed.

#18 F(27)·A(1) Check the state of output ready. Q Response = 1.

The last command data transmission has been completed so ATN can be disabled.

#19 F(24)·A(0) Disable ATN. Q Response = 1.

Attention (ATN) is set to its high (false) state. Now the bus is ready for data exchange between the presently addressed Talker and Listener. As soon as DAV becomes true, the Read LAM Status bit is set.

Command

#20 F(0)·A(0) Read the input register. Q Response = 1.

This allows completion of the bus handshake sequence and clears the Read LAM Status bit. Data sent from the instrument is read.

#21 F(0)·A(0) Read the input register. Q Response = 0

A new data byte is not available. Note that the Read LAM Status bit was false when the command was executed.

In the preceeding example the sequence was controlled by Q test (Q = 0 until the handshake indicated a ready condition). If an interrupt driven system is used, the appropriate LAM status bits can be used to generate LAM's when an operation is completed.

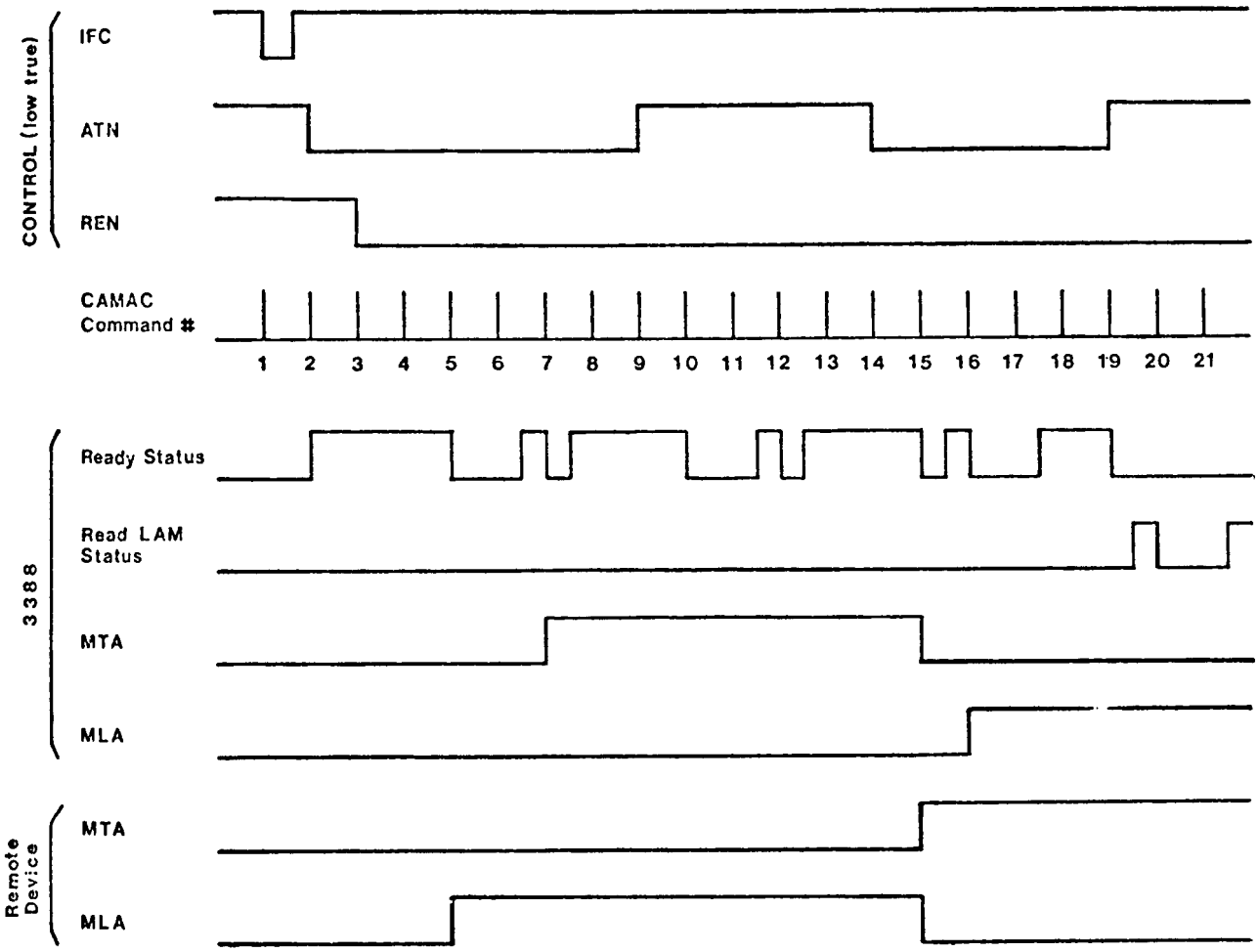


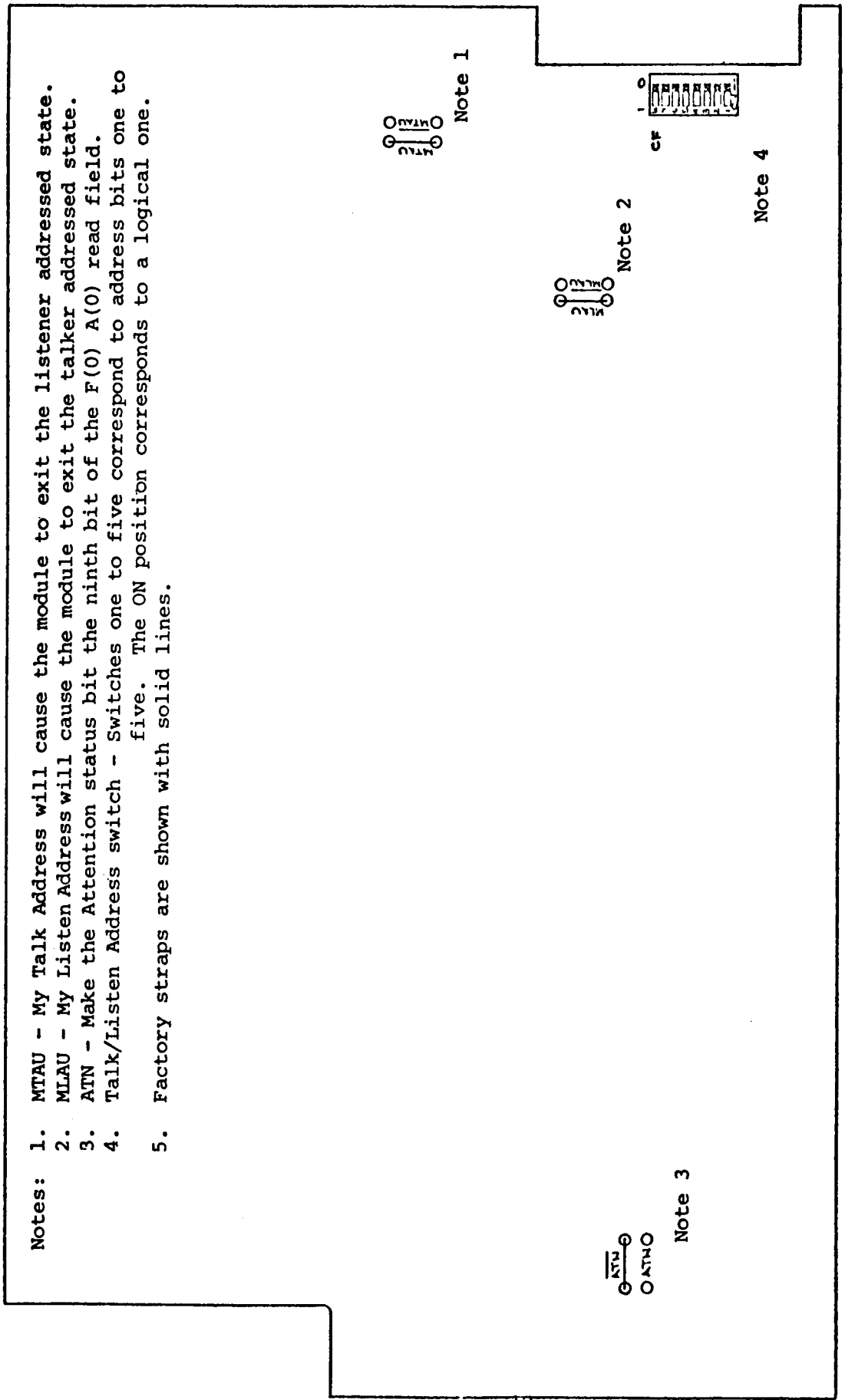
Fig. 2 Take Control and Data Acquisition Sequence

THE UNIVERSAL AND ADDRESSED COMMAND INHIBIT

The GPIB Addressed command group consists of all command bytes (bytes sent with ATN true) which have bits five, six and seven in the logical zero state. An example is the TCT (Take Control) command byte. The GPIB Universal command group consists of all command bytes which have bits six and seven in the logical zero state and bit five in the logical one state. The SPE (Serial Poll Enable) command is a Universal command.

The 3388's Universal and Addressed command inhibit is meant for use in systems where GPIB functions not implemented by the module hardware can be handled by software (generally set [F(26)·A(4)] whenever the 3388 is the system controller). When the Universal and Addressed command inhibit is disabled (state at power up), the handshake sequence will be held until the next CAMAC data read whenever a Universal or Addressed command is received or sent by the 3388. If the Universal and Addressed command inhibit is enabled [F(26)·A(4)] the handshake will be completed normally for all command bytes.

STRAP AND SWITCH OPTIONS



Notes:
1. MTAU - My Talk Address will cause the module to exit the listener addressed state.
2. MLAU - My Listen Address will cause the module to exit the talker addressed state.
3. ATN - Make the Attention status bit the ninth bit of the F(0) A(0) read field.
4. Talk/Listen Address switch - Switches one to five correspond to address bits one to five. The ON position corresponds to a logical one.
5. Factory straps are shown with solid lines.

INPUT/OUTPUT CONNECTORS

IEEE 488-1975 Connector
(socket: type AMP 57-20240

Contact	Signal Line	Contact	Signal Line
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	Gnd, (6)
7	NRFD	19	Gnd, (7)
8	NDAC	20	Gnd, (8)
9	IFC	21	Gnd, (9)
10	SRQ	22	Gnd, (10)
11	ATN	23	Gnd, (11)
12	SHIELD	24	Gnd, LOGIC

IEC Proposed Connector
(socket: Cannon DB25S)

Contact	Signal Line	Contact	Signal Line
1	DIO 1	14	DIO 5
2	DIO 2	15	DIO 6
3	DIO 3	16	DIO 7
4	DIO 4	17	DIO 8
5	REN	18	GND
6	EOI	19	GND
7	DAV	20	GND
8	NRFD	21	GND
9	NDAC	22	GND
10	IFC	23	GND
11	SRQ	24	GND
12	ATN	25	GND
13	SHIELD		

IEEE
Std 488-1978

Remote Message Coding

Mnemonic		Message Name	Type	Class	Bus Signal Line(s) and Coding That Asserts the True Value of the Message: DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	NDAC NRFD ATN DAV EOI SRQ IFC REN
ACG	addressed command group		M	AC	Y	0	0	0	X	X	X	X	XXX 1 X X X X
ATN	attention		U	UC	X	X	X	X	X	X	X	X	XXX 1 X X X X
DAB	data byte	(Notes 1, 9)	M	DD	D8	D7	D6	D5	D4	D3	D2	D1	XXX 0 X X X X
DAC	data accepted		U	HS	X	X	X	X	X	X	X	X	XX0 X X X X X
DAV	data valid		U	HS	X	X	X	X	X	X	X	X	1XX X X X X X
DCL	device clear		M	UC	Y	0	0	1	0	1	0	0	XXX 1 X X X X
END	end		U	ST	X	X	X	X	X	X	X	X	XXX 0 1 X X X
EOS	end of string	(Notes 2, 9)	M	DD	E8	E7	E6	E5	E4	E3	E2	E1	XXX 0 X X X X
GET	group execute trigger		M	AC	Y	0	0	0	1	0	0	0	XXX 1 X X X X
GTL	go to local		M	AC	Y	0	0	0	0	0	0	1	XXX 1 X X X X
IDY	identify		U	UC	X	X	X	X	X	X	X	X	XXX X 1 X X X
IFC	interface clear		U	UC	X	X	X	X	X	X	X	X	XXX X X X 1 X
LAG	listen address group		M	AD	Y	0	1	X	X	X	X	X	XXX 1 X X X X
LLO	local lock out		M	UC	Y	0	0	1	0	0	0	1	XXX 1 X X X X
MLA	my listen address	(Note 3)	M	AD	Y	0	1	L5	L4	L3	L2	L1	XXX 1 X X X X
MTA	my talk address	(Note 4)	M	AD	Y	1	0	T5	T4	T3	T2	T1	XXX 1 X X X X
MSA	my secondary address	(Note 5)	M	SE	Y	1	1	S5	S4	S3	S2	S1	XXX 1 X X X X
NUL	null byte		M	DD	0	0	0	0	0	0	0	0	XXX X X X X X
OSA	other secondary address		M	SE	(OSA = SCG ∧ $\overline{\text{MSA}}$)								
OTA	other talk address		M	AD	(OTA = TAG ∧ $\overline{\text{MTA}}$)								
PCG	primary command group		M	—	(PCG = ACG ∨ UCG ∨ LAG ∨ TAG)								
PPC	parallel poll configure		M	AC	Y	0	0	0	0	1	0	1	XXX 1 X X X X
PPE	parallel poll enable	(Note 6)	M	SE	Y	1	1	0	S	P3	P2	P1	XXX 1 X X X X
PPD	parallel poll disable	(Note 7)	M	SE	Y	1	1	1	D4	D3	D2	D1	XXX 1 X X X X
PPR1	parallel poll response 1	(Note 10)	U	ST	X	X	X	X	X	X	X	1	XXX 1 1 X X X
PPR2	parallel poll response 2		U	ST	X	X	X	X	X	X	1	X	XXX 1 1 X X X
PPR3	parallel poll response 3		U	ST	X	X	X	X	X	1	X	X	XXX 1 1 X X X
PPR4	parallel poll response 4		U	ST	X	X	X	X	1	X	X	X	XXX 1 1 X X X
PPR5	parallel poll response 5		U	ST	X	X	X	1	X	X	X	X	XXX 1 1 X X X

Mnemonic		Message Name	Type	Class	Bus Signal Line(s) and Coding That Asserts the True Value of the Message: DIO 8	7	6	5	4	3	2	1	NDAC NRFD ATN EOI SRQ IFC REN
PPR6	parallel poll response 6	(Note 10)	U	ST	X	X	1	X	X	X	X	X	XXX 1 1 X X X
PPR7	parallel poll response 7	(Note 10)	U	ST	X	1	X	X	X	X	X	X	XXX 1 1 X X X
PPR8	parallel poll response 8	(Note 10)	U	ST	1	X	X	X	X	X	X	X	XXX 1 1 X X X
PPU	parallel poll unconfigure		M	UC	Y	0	0	1	0	1	0	1	XXX 1 X X X X
REN	remote enable		U	UC	X	X	X	X	X	X	X	X	XXX X X X X 1
RFD	ready for data		U	HS	X	X	X	X	X	X	X	X	X0X X X X X X
RQS	request service	(Note 9)	U	ST	X	1	X	X	X	X	X	X	XXX 0 X X X X
SCG	secondary command group		M	SE	Y	1	1	X	X	X	X	X	XXX 1 X X X X
SDC	selected device clear		M	AC	Y	0	0	0	0	1	0	0	XXX 1 X X X X
SPD	serial poll disable		M	UC	Y	0	0	1	1	0	0	1	XXX 1 X X X X
SPE	serial poll enable		M	UC	Y	0	0	1	1	0	0	0	XXX 1 X X X X
SRQ	service request		U	ST	X	X	X	X	X	X	X	X	XXX X X 1 X X
STB	status byte	(Notes 8, 9)	M	ST	S8	X	S6	S5	S4	S3	S2	S1	XXX 0 X X X X
TCT	take control		M	AC	Y	0	0	0	1	0	0	1	XXX 1 X X X X
TAG	talk address group		M	AD	Y	1	0	X	X	X	X	X	XXX 1 X X X X
UCG	universal command group		M	UC	Y	0	0	1	X	X	X	X	XXX 1 X X X X
UNL	unlisten		M	AD	Y	0	1	1	1	1	1	1	XXX 1 X X X X
UNT	untalk	(Note 11)	M	AD	Y	1	0	1	1	1	1	1	XXX 1 X X X X

The 1/0 coding on ATN when sent concurrent with multiline messages has been added to this revision for interpretive convenience.

NOTES:

(1) D1-D8 specify the device dependent data bits.

(2) E1-E8 specify the device dependent code used to indicate the EOS message.

(3) L1-L5 specify the device dependent bits of the device's listen address.

(4) T1-T5 specify the device dependent bits of the device's talk address.

(5) S1-S5 specify the device dependent bits of the device's secondary address.

(6) S specifies the sense of the PPR.

S	Response
0	0
1	1

P1-P3 specify the PPR message to be sent when a parallel poll is executed.

P3	P2	P1	PPR Message
0	0	0	PPR1
.	.	.	.
.	.	.	.
.	.	.	.
1	1	1	PPR8

(7) D1-D4 specify don't-care bits that shall not be decoded by the receiving device. It is recommended that all zeroes be sent.

(8) S1-S6, S8 specify the device dependent status. (DIO7 is used for the RQS message.)

(9) The source of the message on the ATN line is always the C function, whereas the messages on the DIO and EOI lines are enabled by the T function.

(10) The source of the messages on the ATN and EOI lines is always the C function, whereas the source of the messages on the DIO lines is always the PP function.

(11) This code is provided for system use, see 6.3.