KINETICSYSTEMS CORPORATION

Model 3952-Z1E/Z1F

Enhanced Type L-2 Serial Crate Controller

INSTRUCTION MANUAL

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Model 3952-Z1E/Z1F Operating Manual

In systems driven by PRE-1986 Models 2050 through 2085 Highway Drivers, the following modification is required.

On the D117 Transmitter Card of the Driver:

1. On solder side, cut chip AR Pin 6 from AR Pin 12.
2. On component side (using pointed X-ACTO knife) cut printed circuit from chip AR Pin 6 underneath chip AR.
3. Wire AR Pin 12 to AR Pin 8.
4. Wire AR Pin 6 to AS Pin 16.

August, 1989

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Schematic Drawing #02267-D-4539	Insert

KineticSystems Corporation

Standardized Data Acquisition and Control Systems

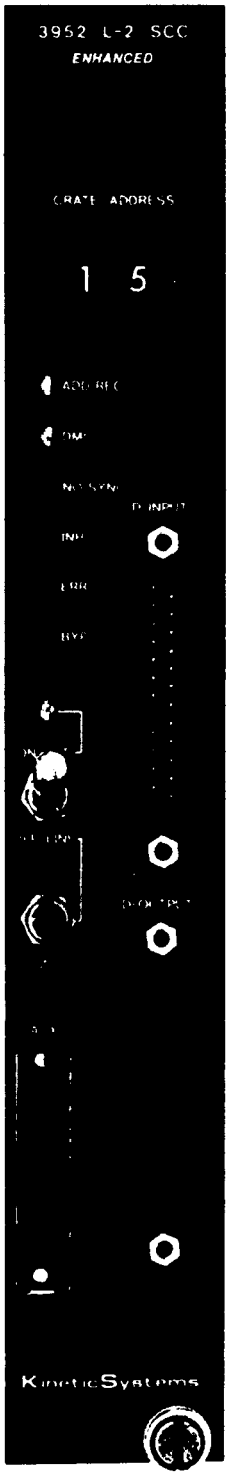
3952

Enhanced Type L-2 Serial Crate Controller

(Rev. Jun. 87)

FEATURES

- **Includes enhanced block-mode features**
- **Available with option for use in high magnetic fields**
- **Complies with IEEE Standards 583 and 595**
- **Supports auxiliary crate controllers**
- **Capable of "enhanced" data throughput to three megabytes per second**
- **Supports clock rates to five megahertz**
- **Strap-selectable for bit-serial and byte-serial operation**
- **Address selection allows up to 62 crates on a single highway**
- **Enhanced and standard L-2 SCCs can be mixed on the same highway**
- **Provides galvanic isolation of the Serial Highway with a companion U-Port adapter**
- **Supports enhanced list-mode operation when used with the 3830 LSM**
- **Transmits asynchronous Demand messages to the Serial Highway driver**



GENERAL DESCRIPTION

The Model 3952 is a double-width Type L-2 serial crate controller (SCC) providing the interface between the CAMAC Serial Highway and the Dataway in a CAMAC crate. It fully complies with IEEE Standards 583 and 595. The standard Serial Highway (SH) protocol provides for one Dataway operation associated with each message. KineticSystems Corporation has developed enhanced block modes to the SH protocol for applications where an extremely high data throughput is needed. The enhanced 3952 supports this block protocol. A CAMAC Serial Highway system consists of a Serial Highway driver (such as the 2160) interfaced to the host computer, the Serial Highway itself, and up to 62 Type L-2 serial crate controllers.

The 3952 enhanced L-2 SCC provides all features set forth in IEEE Standard 583 for crate controllers and IEEE-595 for Type L-2 SCCs. When a Serial Highway driver (such as the 2160) transmits a multi-CAMAC-word command message, an addressed enhanced SCC switches to block mode to interpret the message and perform the Dataway operations. Regular and enhanced SCCs operate in the same system as long as enhanced block-mode messages are not sent to the regular SCCs.

CRATE CONTROLLER OPTIONS

Relay contacts are provided for controlling external U-Port adapters such as KSC Models 3936 and 3939. Contacts have one side to the module common and the other side to the Serial Highway connectors. The bypass contact is closed for BYPASS = TRUE, and the loop collapse contact is open for LOOP COLLAPSE = TRUE. Reed relays are used in the 3952-Z1E. When high-intensity magnetic fields up to 150 gauss are anticipated, the 3952-Z1F should be used. These controllers contain specially shielded relays.

BASIC L-2 SCC OPERATION

The 3952 SCC receives a clock and data signal from the SHD or an "upstream" SCC. The clock rate can range from arbitrarily slow to five megahertz. This clock rate is set within the SHD and must take into consideration the transmission medium and other external devices such as U-Port adapters and modems. The SCC is strap-selectable for bit-serial (with clock and one data pair) or byte-serial operation (with clock and eight data pair). Choose byte-serial operation when a higher throughput is required. The clock and data signals follow the RS-422 balanced-line specification and are received at the D-IN connector on the SCC.

(continued on following page)

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BASIC L-2 SCC OPERATION *(continued)*

The SCC contains a two-digit, front-panel address switch. Use this switch to select the address of an SCC; valid addresses range from 1 to 62. *Note that only one SCC on the highway should be set to any given address.* The Serial Highway forms a continuous loop from the the SHD, through the SCC(s), and back to the SHD. When a particular SCC receives a command message not addressed to it, the SCC passes the message to the next SCC (or back to the SHD if this SCC is the last controller on the highway). When addressed, the SCC interprets the command message, performs the CAMAC operation, and transmits the reply message via the D-OUT connector. An enhanced SCC checks the command header to determine whether a regular or enhanced message is being received and performs the appropriate CAMAC operations.

DEMAND MESSAGE GENERATION

If enabled, the L-2 crate controller generates a three-byte Demand message in response to any L-signal in the crate and inserts the message into the data stream. Demand messages are inserted between other messages, and a three-byte memory is inserted in the incoming data stream as Demand messages are transmitted. When a three-byte gap is detected between incoming messages, the delay is switched out, allowing another Demand message to be generated.

If the L-signal in the crate is not cleared by a predetermined elapsed time, a Repeated-Demand message is generated. Repeated messages have each of the five Graded-L bits set to 1. The repeat-timer can be adjusted for delays between one millisecond and ten seconds. The delay is strap-selected. The timer can also be disabled. The rear-panel SGL connector has all the input and output signals necessary for encoding the SGL field of the Demand message.

SGL-ENCODER CONNECTOR

The rear-panel, 52-contact "D" SGL connector contains the 24 individual LAM lines, the signals for producing the SGLE (encoded LAM) bits, the Demand control signals, and the binary N lines. Demand generation can be provided by a 2010 SGL Adapter or a 3924 LAM Encoder module. Alternatively, demand generation can be provided using simple patching on a 5942-Z1B connector with the contact patched as follows:

contact 50 to 23 contact 19 to 21 contact 23 to 25

The 2010 SGL Adapter can provide this patching and allows up to five LAM lines to assert SGLE bits in the Demand message. The 2010 is also used to interface the 3952 to the Auxiliary Controller Bus. The 3924 LAM Encoder module provides for the orderly handling of overlapping LAMs.

U-PORT ADAPTERS

A Serial Highway can be configured to use twisted-pair or fiber optic cable. If the 12-volt common-mode limit for D-Port operation is likely to be exceeded or if the highway is long, U-Port adapters are recommended. A U-Port Adapter is used in conjunction with the Serial Highway driver and the remote Type L-2 serial crate controllers. For bit-serial operation, the 3936 provides galvanic isolation and transformer coupling, while the 3938 uses fiber optic cable. When high throughput or longer distances are required, the 3939 provides excellent performance in byte-serial mode using fiber optic cable.

LIST SEQUENCER MODULE

Enhanced versions of the 3952 support block-mode, single-NAF transfers for reading a transient recorder memory, etc. A 3830 List Sequencer module (LSM) can be used with the 3952 to support random-NAF transfers at full enhanced block-mode speed.

THROUGHPUT PERFORMANCE

When block-mode messages are being received in byte-serial mode, the 3952-Z1E and -Z1F support transfer rates up to three megabytes per second (one Dataway operation every microsecond); in bit-serial mode, the rates are up to 300 kilobytes per second (one Dataway operation every ten microseconds). *Caution: The actual maximum block rate depends upon the computer interface, Serial Highway Driver, and clock rate used. Consult KineticSystems Corporation for performance details on your particular system.*

CLOCK RATE

The 3952 will operate at a clock rate from arbitrarily slow to five megahertz. Generally a high clock rate produces a higher message throughput. The actual clock rate for any situation is determined by a number of factors. They are:

1. The signal loss through the transmission media determines the maximum clock rate.
2. The clock speed selection in the Serial Highway driver (SHD) controls the highway clock rate.
3. U-Port adapters (UPAs) generally provide a number of clock rate options. The UPA clock rate must be converted with that of the Serial Highway driver.

INTERNAL FUNCTION CODES (N = 30)

Command		SQ	Action
F(0)·A(1)	RD1	DSQ	Rereads the previous Read-field.
F(1)·A(0)	RD2	1	Reads the Status register.
F(1)·A(12)	RD2	1	Reads the LAM pattern.
F(12)·A(0)	F12	1	Selects the NAF list 0. (See Note 2.)
F(12)·A(1)	F12	1	Selects the NAF list 1. (See Note 2.)
F(12)·A(2)	F12	1	Selects the NAF list 2. (See Note 2.)
F(12)·A(3)	F12	1	Selects the NAF list 3. (See Note 2.)
F(17)·A(0)	WT2	1	Writes the Status register.
F(19)·A(0)	SS2	1	Selectively sets the Status register.
F(23)·A(0)	SC2	1	Selectively clears the Status register.

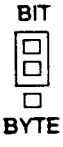
Notes: 1. SX = 1 is returned for all valid addressed commands unless the 3952 is bypassed.
2. This command is operable only when used with a 3830 List Sequencer Module.

STATUS REGISTER

Bit	True-State Definition	State On Power-up	Notes
1	Initiates Dataway Z	0	Write-only
2	Initiates Dataway C	0	Write-only
3	SCC control-bit for Dataway I	1	Read/Write
4	DERR	0	Read-only
5	DSX	0	Read-only
6	DSQ	0	Read-only
7	Dataway I	0	Read-only
8	(Reserved)	—	———
9	Demand enable	0	Read/Write
10	Internal demand (L24)	0	Read/Write
11	Loop collapse	0	Read/Write
12	SCC bypass	1	Write-only
13	Dataway off-line	1	Writes control-bit, reads actual state
14	Switch off-line	—	Read-only
15	Enhanced option	1	Read-only
16	Selected Ls present	—	Read-only

STRAP OPTIONS

BIT/BYTE SERIAL



Strap on left board, shown in BIT MODE.

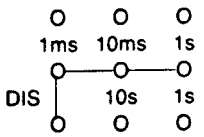
AUX CONTROLLER LOCKOUT

Strap on left board

A - ACL at start of Dataway Cycle

B - ACL after header

REPEAT TIMER



Strap on right board (shield removed), shown with timer disabled.

FRONT PANEL

LEDs	
ADD REC	Indicates that the crate is receiving a message addressed to it. A one-shot extends this signal.
ERR	Indicates that an error on the last incoming message caused a Dataway cycle not to occur OR a Dataway cycle did occur but X = 0 was returned.
ON-LINE	Indicates that the SCC is on-line.
BYPASS	Indicates that the SCC is in a bypassed state.
NO SYNC	Indicates that the SCC is out of synchronization. A one-shot extends this signal.
DMI	Indicates that the Demand Message Initiate signal is true. A on-shot extends this signal.
INHIBIT	Indicates that the Dataway Inhibit (I) signal is true.
SWITCHES	
ON-LINE ENABLE/ OFF-LINE	A locking toggle switch provides the manual On-line/Off-line control for the SCC. The On-line/Off-line state of the SCC is controlled by this switch and the Dataway Off-line (DOF) bit in the SCC status register.
Z/C	A three-position, center-off toggle switch is used to generate the Initialize (Z) signal and the Clear (C) signal. Pushing the switch up generates C; down generates Z. It is active only in the Off-line state.
CRATE ADDRESS	Two thumbwheel switches are provided to select the units digit and tens digit of the crate address. The switches provide numerical indication of the selected address.
CONNECTORS	
D-OUTPUT	D-Port output connector, 25-way Cannon Type DBC-25S (socket) or equivalent.
D-INPUT	D-Port input connector, 25-way Cannon Type DBC-25P (plug) or equivalent.
AUX	14-pin flat ribbon connector for observing internal logic signals and for the 3830 LSM.

POWER REQUIREMENTS

+6 volts — 3000 mA

ORDERING INFORMATION

Weight: 1.2 kg (2 lb. 9 oz.)

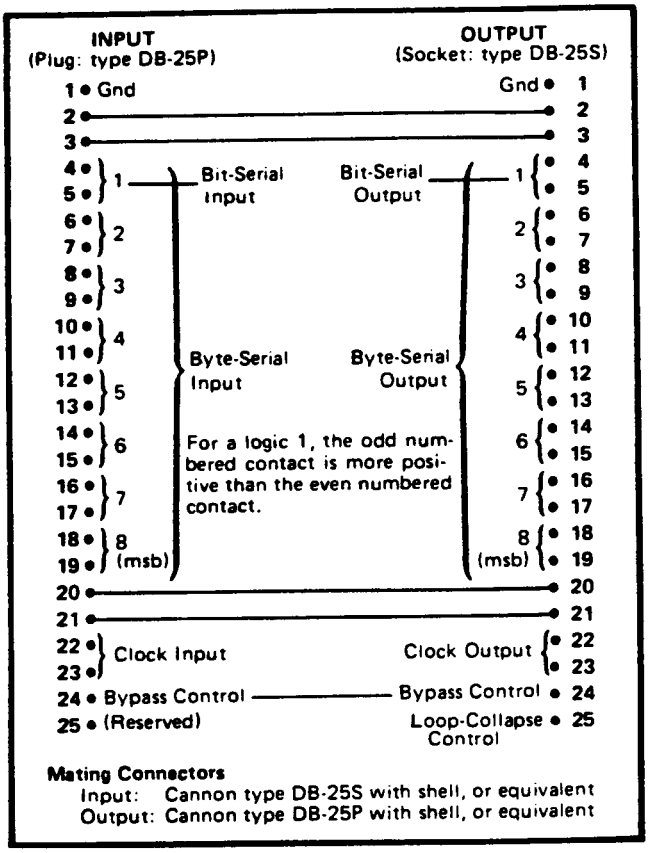
Model 3952-Z1E — Enhanced Type L-2 Serial Crate Controller with Standard Relays

Model 3952-Z1F — Enhanced Type L-2 Serial Crate Controller with High-gauss Relays

Accessories — Models 5932-Z1A, 5933-Z1A, 5940-Z1A, 5942-Z1A Mating Connectors
Model 5800-Axyz Bit-serial Highway Cable
Model 5800-Bxyz Bit-serial Highway Cable
Model 5843-Series ACB Cable Assemblies
Model 5860-R000 SGL Cable for 3924
Model 2010-Z1A SGL Adapter
Model 3933 Dual-loop U-Port Adapter
Model 3936 Single-loop U-Port Adapter
Model 3938 Bit-serial, Fiber Optic U-Port Adapter
Model 3939 Byte-serial, Fiber Optic U-Port Adapter

Note: The 3952-Z1E and -Z1F supercede the 3952-Z1C and -Z1D and are fully compatible with these versions of the SCC.

SERIAL HIGHWAY CONNECTORS

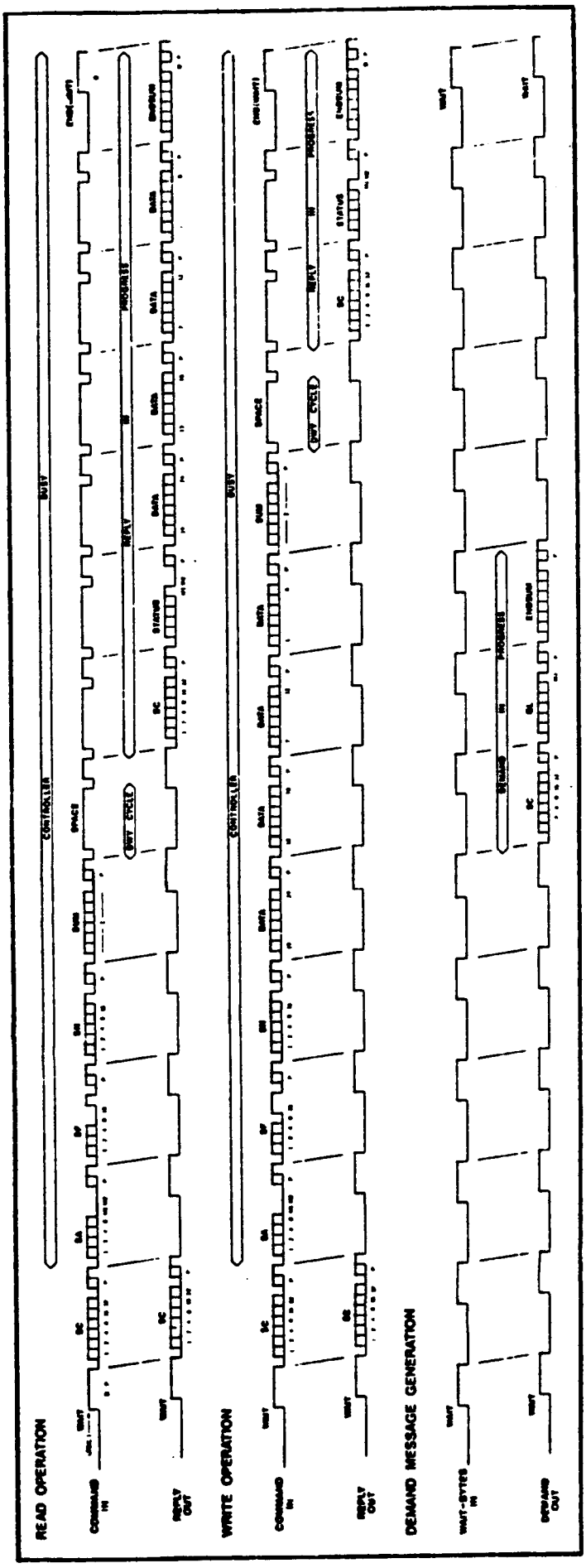


AUXILIARY CONNECTOR

PIN	SIGNAL
1	RAW CLOCK IN
2	CLOCK OUT
3	BIT DATA IN
4	BIT DATA OUT
5	GROUND
6	GROUND
7	
8	
9	IS3
10	F
11	LIST 3
12	LIST 2
13	LIST 1
14	LIST 0

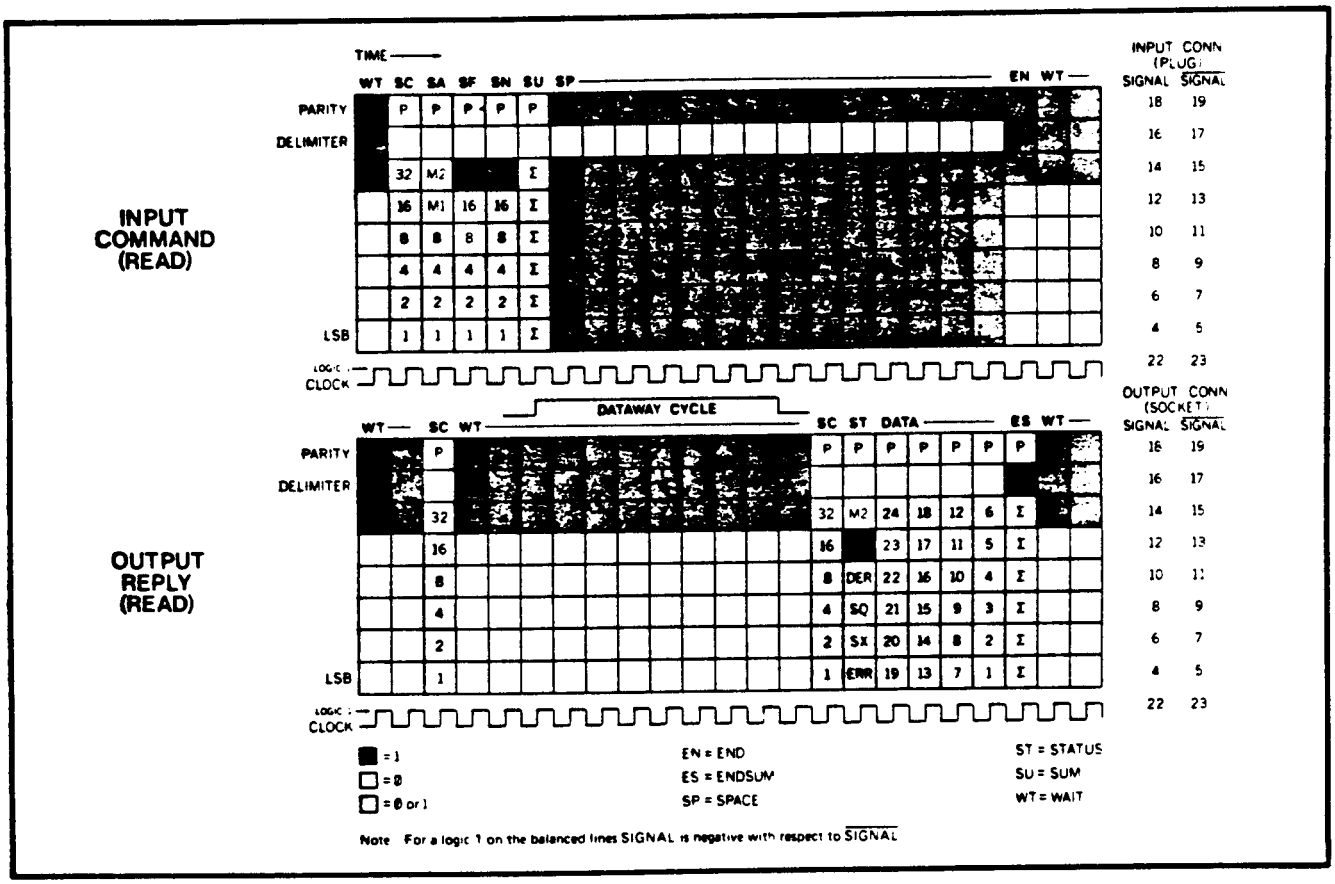
SGL–ENCODER CONNECTOR

Contact	Signal	Direction	Contact	Signal	Direction
1	Demand Busy	Out	2	L1	Out
3	SGLE1	In	4	L2	Out
5	SGLE2	In	6	L3	Out
7	SGLE3	In	8	L4	Out
9	SGLE4	In	10	L5	Out
11	SGLE5	In	12	L6	Out
13	External Repeat	In	14	L7	Out
15	——		16	L8	Out
17	Request Inhibit	In	18	L9	Out
19	Time-out	Out	20	L10	Out
21	Demand Message Initiate	In	22	L11	Out
23	Start timer	In	24	L12	Out
25	Selected L's present	In	26	L13	Out
27	——		28	L14	Out
29	Auxiliary Controller Lockout	Out	30	L15	Out
31	Byte Clock	Out	32	L16	Out
33	——		34	L17	Out
35	——		36	L18	Out
37	——		38	L19	Out
39	——		40	L20	Out
41	SCC Busy	Out	42	L21	Out
43	N1	In	44	L22	Out
45	N2	In	46	L23	Out
47	N4	In	48	L24	In/Out
49	N8	In	50	L-SUM	Out
51	N16	In	52	Gnd	——



BIT-SERIAL MESSAGE OPERATIONS

TYPICAL BYTE-SERIAL OPERATION



DESCRIPTION OF BLOCK TRANSFER FEATURE

The Model 3952 Z1E/Z1F Block Transfer Serial Crate Controller (BTSCC) contains all of the mandatory requirements of IEEE Standard 583-1975, Modular Instrumentation and Digital Interface System (CAMAC) and IEEE Standard 595-1976, Serial Highway Interface System (CAMAC). In addition to the mandatory features of a Type L-2 SCC, this unit contains a block transfer feature that increases the effective block data rate from approximately 6 million information bits per second to 24 million bps.

The BTSCC supports the following modes of operation:

1. Standard single-word transactions (per the L-2 SCC specification).

2. Blockmode to/or/from a single CAMAC NAF (used for memory dump, downloading to the LSI-11, etc.).

3. "Random-scan" block mode using the List Sequencer Module (LSM) to select the list of CAMAC NAF's.

Any one mode can be selected by the appropriate stimulus from the Serial Driver (SD). Of course, the SD must also contain features to support these block modes.

MESSAGE STRUCTURE FOR BLOCK DATA TRANSFER

Figures 1 and 2 show the bytes associated with the Command/Reply sequence for a block mode operation (single-NAF or list-mode). Note that it is a logical extension of the L-2 single-transaction sequence.

A key element is the CONTROL byte. The two LSB's of this byte are decoded as follows:

00: Initiate a Dataway Cycle, this is <u>not</u> the last word in the block.

01: Initiate a Dataway Cycle, this <u>is</u> the last word in the block.

10: Do <u>not</u> initiate a Dataway Cycle and this is <u>not</u> the last word.

11: Do <u>not</u> initiate a Dataway Cycle and this <u>is</u> the last word.

This method allows variable length blocks without the need for a word-count register in the BTSCC and provides a time buffer if the host computer memory does not respond to the data transfer rate.

The status byte in the Reply for each word provides the Q and X response from the module as well as error information. Bit 5 of the status byte, normally a 1 indicating reply, is set to 0 when the BTSCC detects command words which have a CONTROL byte of 2 or 3. The SD ignores all block reply words, after the first, that have bit 5 of its status byte set to 0.

COMMAND/REPLY SEQUENCE FOR BLOCK WRITE OPERATION

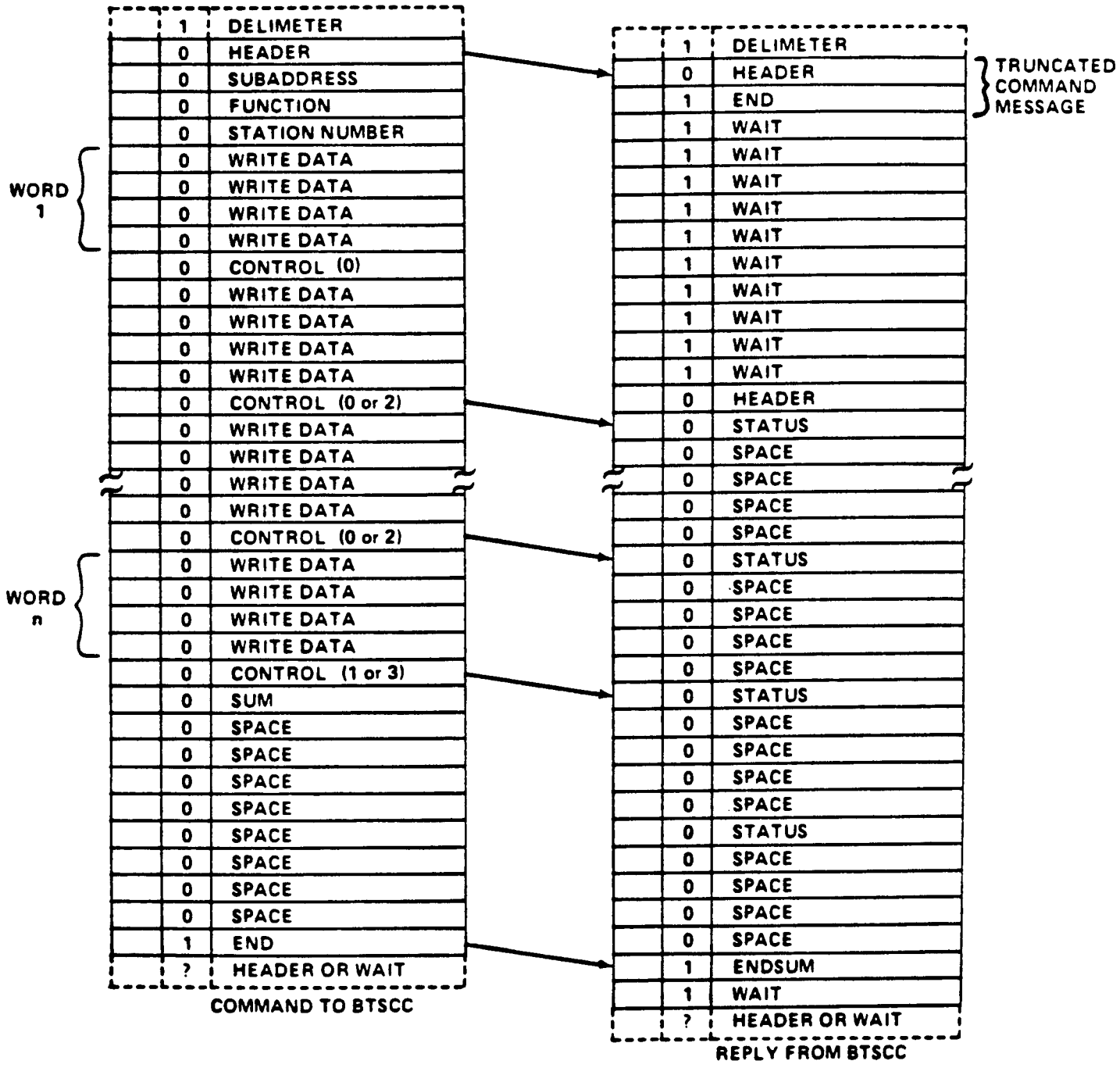


Figure 1: Command/Reply Sequence for Block Write Operation

COMMAND/REPLY SEQUENCE FOR BLOCK READ OPERATION

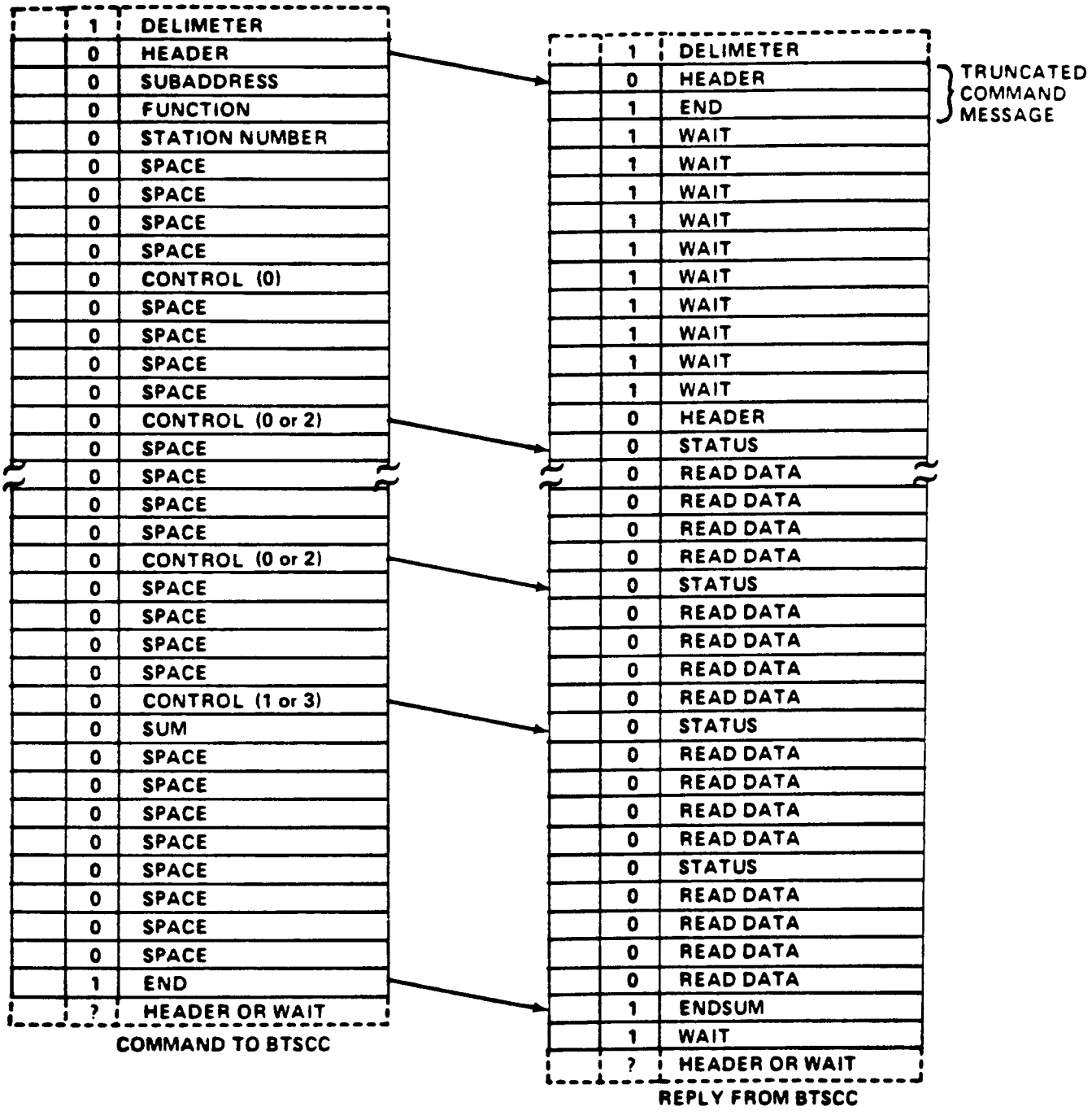


Figure 2: Command/Reply Sequence for Block Read Operation

Single NAF Block Mode

Single-NAF block mode is enabled in the BTSCC when a Function Code byte with bit 6 set to 0 is received. Bit 6, of the Function Code byte, for all other commands is sent by the SD as a 1.

With single-NAF block mode enabled the BTSCC expects a multi-word Read or Write sequence with the Subaddress, Function Code and Station Number bytes indicating the module slot to be addressed and Function Code to be performed, for example, a typical block-Write would be: N(6)·F(16)·A(0).

The data transfer sequence is complete when a Control byte of 1 or 3 is detected in the command message.

List-Mode Block Transfer

The BTSCC requires an additional module when operating in list-mode block transfer. This List Sequencer Module (LSM) has a 2k x 16 bit memory which is divided into four 512 x 16 segments, LIST 0, LIST 1, LIST 2 and LIST 3.

LIST 0 and LIST 1 contain sets of CAMAC Read NAF's to be processed for Input. LIST 2 and LIST 3 contain sets of CAMAC Write NAF's to be processed for Output.

List-mode block transfer is enabled when the BTSCC receives one of the following commands:

Command	NAF List	Data Type
N(30)·F(12)·A(0)	List 0	Read
N(30)·F(12)·A(1)	List 1	Read
N(30)·F(12)·A(2)	List 2	Write
N(30)·F(12)·A(3)	List 3	Write

Control of the LSM by the BTSCC is via a front-panel private bus with the following signals:

Signal	Time in Message	Description
List 0	After N byte	Selects Read List 0
List 1	After N byte	Selects Read List 1
List 2	After N byte	Selects Write List 2
List 3	After N byte	Selects Write List 3
INC NAF	After Dataway S2	Increments NAF pointer in LSM
SUM OK	After SUM byte is received correctly	Used in LSM to enable Rank 1/Rank 2 transfer on Write operations

If the LSM has been activated by the BTSCC during a "scan" transfer sequence (Write block type), the following occurs:

> The BTSCC drives only the Write lines and leaves the N, A, and F lines free. The LSM gains access to the N lines by way of the auxiliary controller bus at the rear of the BTSCC. It drives the F and A lines by access at its own slot Dataway connection.

Refer to Figure 1. For this sequence, the BTSCC receives an N(30)·F(12)·A(2) command, indicating a LIST2 selection. The remaining sequence is then:

A. After the Station Number (N) byte is received and a "LIST2" sequence identified, the BTSCC sets signal line LIST2. This line is part of the "private bus" cable between the units. The RAM address pointer in the LSM is set to word 1024, the start of the OUTPUT NAF LIST2.

B. When the first NAF appears at the output of the RAM it is latched into the LSM output buffer and enabled into the Dataway.

C. The Write data is received by the BTSCC and stored. A double buffer is used in the BTSCC so that a Dataway cycle can be occuring for word (j) while Write data is being received for word (j + 1). Dataway cycles will occur only if all byte parity is correct.

D. A CONTROL (0) byte is received, indicating valid write data in the write buffer and the start of a Dataway cycle.

E. The Dataway cycle for word 1 begins during the first WRITE DATA byte for word 2. At S1 time the RAM address pointer in the LSM is incremented. At the end of the Dataway cycle INC NAF is pulsed placing NAF 2 into the output buffer and onto the Dataway. At the same time, the BTSCC places the Write data for word 2 on the Dataway.

F. Also, Strobe S1 (generated by the BTSCC at t_0 + 400 ns in the Dataway cycle) causes the Write data (24 bits) to be latched in the addressed module.

G. The process is repeated (C through F) until the Dataway cycle for Word n occurs.

H. Because the possibility of an undetected error is far greater when only byte parity is checked, there is concern that incorrect data are written into output modules (causing a DAC to go to full scale, for example). The BTSCC pulses the SUM OK line to the LSM only if the SUM byte was received correctly. If the SUM OK pulse is received, the LSM passes this signal on to the Dataway P2 line. This "free use" patch line will cause the module to provide an output-update (Rank 1 to Rank 2) "tick" only if this "OK" signal is received. This limits the result to being a "missed point" in the Output sequence instead of a "sudden jerk". This produces a far "softer' result in the unlikely event of an undetected error (from a "double bit" in a byte, giving correct byte parity).

A "scan" Read transfer sequence operates in a similar manner to the Write sequence. Refer to Figure 2. For this sequence, the BTSCC receives an N(30)·F(12)·A(0) command, indicating a LIST0 selection. The remaining sequence is then:

A. After the N byte is received, the BTSCC sets the LIST0 signal line to the LSM. The RAM address is zero'd to word 0, the start of the INPUT NAF list.

B. The first NAF appears at the LSM memory output, is latched into the output buffer and enabled onto the Dataway.

C. A CONTROL (0) byte is received and the BTSCC starts the Dataway cycle. At S1 time, the address pointer increments so that the next NAF is readied within the LSM (also, see Q Repeat mode, discussed below). At the end of the Dataway cycle, INC NAF is pulsed and NAF 2 is enabled onto the Dataway.

D. The module Read data is stored in the BTSCC when this SCC generates Strobe S1. This data is readied for serial highway transmission in future bytes.

E. This process is repeated (C and D) until the last Dataway cycle is executed.

In some cases (with the ADC modules, for example) the Read data are not available when a Read command is executed. If a Q Repeat mode were previously enabled in the LSM and a Q = 0 response is detected at Strobe S1 within the LSM, the memory pointer is not incremented and the command is repeated.

For proper operation, Q Repeat mode must also be enabled in the SD. This causes the SD to "ignore" all Q = 0 responses and not increment its word count or perform a data transfer to the Host Computer.

If an over-run on Read or Write is attempted (incrementing the LSM memory pointer beyond the end-of-list flag in the LSM memory word), the LSM will stop asserting NAF's. This will result in N(0) commands(s) being executed with an X = 0 (command not accepted) response back to the SD and appropriate error indication.

INTERBOARD PIN CONNECTIONS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	DEMAND	34	W3	67	IR18
2	WRITE	35	W1	68	IR17
3	GND	36	MB5	69	IR16
4	GND	37	MB4	70	IR15
5	READ	38	MB3	71	IR14
6	ENA PLA2	39	MB2	72	IR13
7	EX COMP	40	MB1	73	IR12
8	ENA PLA1	41	MB6	74	IR11
9	DIP	42	DERR	75	IR10
10	CRB-L	43	IBYC1	76	IR9
11	PUP-L	44	OUT STAT	77	IR8
12	BCK	45	E N&W	78	IR7
13	IBTC1	46	SX	79	IR6
14		47	SGL5	80	IR5
15	ENA F	48	SGL4	81	IR4
16	ENA N	49	SGL3	82	IR3
17	ENA A	50	SGL2	83	IR2
18	DWG0	51	SGL1	84	IR1
19	W12	52	IRB6	85	INHIBIT LED
20	W11	53	IRB5	86	ON LINE SW
21	W10	54	IRB4	87	BYPASS LED
22	W9	55	IRB3	88	DEMAND LED
23	SACL	56	IRB2	89	COLLAPSE
24	W13	57	IRB1	90	BYPASS
25	OUT 6	58	IRB0	91	Z SW
26	OUT 12	59	INT READ	92	C SW
27	OUT 24	60	IS1L	93	GND
28	OUT 18	61	IR24	94	ON LINE
29	GND	62	IR23	95	GND
30	SQ	63	IR22	96	INC NAF
31	GND	64	IR21	97	LIST 3
32	IBYC2	65	IR20	98	LIST 2
33	W2	66	IR19	99	LIST 1
				100	LIST 0

MNEMONIC DEFINITIONS

MNEMONIC	DEFINITION
BCK	BYTE CLOCK TO SGL CONN.
BIT	BIT SERIAL MODE WHEN LOW
BYTE	BYTE SERIAL MODE WHEN LOW
IBYC1	INTERNAL BYTE GATE PULSE 1
IBYC2	INTERNAL BYTE GATE PULSE 2
IBTC1	INTERNAL BIT GATE PULSE 1
DERR	DELAYED ERROR BIT
SQ	SERIAL Q RESPONSE
SX	SERIAL X RESPONSE
SGL1-5	SERIAL GRADED LAM PATTERN (5 BITS)
DELIMITER	BIT 7 OF INPUT AND OUTPUT MESSAGE
TPE	TRANSVERSE PARITY ERROR
LPE	LONGITUDINAL PARITY ERROR
ERR	INPUT MESSAGE ERROR
READ	READ COMMAND BEING EXECUTED
WRITE	WRITE COMMAND BEING EXECUTED
EX COMP	DATAWAY CYCLE COMPLETE
DEMAND	LAM PENDING
DWGO	START DATAWAY CYCLE
E N&W	ENABLE N AND WRITE LINES ON DATAWAY
W1-13	WRITE DATA BIT USED INTERNALLY
W1-24	DATAWAY WRITE LINES
R1-24	DATAWAY READ LINES
IR1-24	INTERNAL READ LINES
IRB0-6	BYTE READ DATA TO OUTPUT BUS
INT READ	INTERNAL READ (USED WHEN READING LAM OR STATUS)
IS1L	INTERNAL S1 LOW TRUE
ENA PLA1	ENABLE FPLA1
ENA PLA2	ENABLE FPLA2
ENA A	ENABLE A REGISTER
ENA F	ENABLE F REGISTER
ENA N	ENABLE N REGISTER
EN IN LPCK	ENABLE INPUT PARITY CHECKER
EN OUT LPCK	ENABLE OUTPUT PARITY GENERATOR
CRBL	CONTROLLER BUSY LOW TRUE
DIP	DEMAND MESSAGE IN PROGRESS
NO SYNC	CONTROLLER HAS LOST BIT OR BYTE SYNC
OUT HEADER	PLACE HEADER ON OUTPUT BUS
OUT STATUS	PLACE STATUS ON OUTPUT BUS
OUT SPACE	PLACE SPACE BYTE ON OUTPUT BUS
OUT WAIT	PLACE WAIT BYTE ON OUTPUT BUS
OUT R24	PLACE UPPER 6-BITS OF READ DATA ON OUTPUT BUS
OUT R18	PLACE 2ND MS6-BITS OF READ DATA ON OUTPUT BUS
OUT R12	PLACE 3RD MS6-BITS OF READ DATA ON OUTPUT BUS
OUT R6	PLACE LOWER 6-BITS OF READ DATA ON OUTPUT BUS
OUT LP	PLACE LONGITUDINAL PARITY ON OUTPUT BUS

MNEMONIC DEFINITIONS

MNEMONIC	DEFINITION
3 BYTE DELAY	3 BYTE DELAY IS SWITCHED IN WHEN HIGH
HEAD COMP	INPUT MESSAGE CRATE ADDRESS AND THUMBWHEEL SWITCHES ARE EQUAL
OUT SGL	PLACE SERIAL-GRADED LAM PATTERN ON OUTPUT BUS
PASS MESS	PASS INPUT BYTE TO OUTPUT BUS
ILL ADD	THUMBWHEEL SWITCHES ARE EQUAL TO 0 OR GREATER THAN 62
EN PSC LOAD	ENABLE PARALLEL TO SERIAL CONVERTER LOADING
LIST0-3	SELECTS NAF LIST IN 3830
INC NAF	INCREMENTS NAF LIST IN 3830
SUM OK	USED WITH 3830 TO TRANSFER DATA IN I/O MODULES
W/W PINS	PLA ADDRESS USED FOR TESTING
MB1-5	INPUT BYTE DATA, USED TO LOAD F,N,A REGISTERS
SACL	SET AUXILIARY CONTROLLER LOCKOUT
PUP-L	POWER UP CLEAR (LOW TRUE)
E A&F	ENABLE A AND F LINES TO DATAWAY
N(30)	INTERNAL COMMAND TO SCC (WHEN LOW)
IBSY	SCC IS BUSY INTERNALLY
READ GATE	GATE READ DATA TO 2ND STAGE REGISTER
I	DATAWAY INHIBIT LINE (LOW TRUE)
DSQ	DELAYED SERIAL Q RESPONSE
DSQ-L	DELAYED SERIAL Q RESPONSE (LOW TRUE)
DSX	DELAYED SERIAL X RESPONSE
INH	INHIBIT BIT IN STATUS REG. (HIGH TRUE)
DEM	DEMAND ENABLE BIT IN STATUS REG. (HIGH TRUE)
LC	LOOP COLLAPSE BIT IN STATUS REG. (HIGH TRUE)
BYP	BYPASS BIT IN STATUS REG. (HIGH TRUE)
ST OFF LINE	OFF LINE BIT IN STATUS REG. (HIGH TRUE)
L1-24	DATAWAY LAM LINES
N1-23	DATAWAY N LINES
A1,2,4,8	DATAWAY A LINES
F1,2,4,8,16	DATAWAY F LINES

3952 Clean-up circuitry

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There are many generations of L-2 3952 crate controllers here at PPPL. This particular document is only going to discuss two versions, although each of these versions span several generations. These two versions are also described in TFTR-10A2-H67-REV. 1, CAMAC Link Operations Manual. The "old" type can be distinguished by the use of all red LED's and a 19 pin miniature "D" type auxiliary connector on its front panel. The "new" type uses a mix of red and yellow LED's and a 14 pin ribbon type auxiliary connector on its front panel. This "new" type also includes the "enhanced" versions.

The "new" type has improved circuitry on the clock, making it less susceptible to marginal clock signals. In bit-serial mode, this "clean-up" circuit has a different propagation delay than that of the "old" type. This results in the host U-Port's output becoming mistuned if an "old" 3952 is replaced by a "new" one, or vice versa. Therefore, a bad 3952 must be replaced with one of the same type, or the U-Port must be re-tuned. This pertains to bit-serial links only. The EPICS1 link is bit-serial.

In a byte-serial link, this delay does not matter. However, in a byte-serial link, there are conditions which require this improved "clean-up" circuitry, such as ribbon cables, long data cables, and 5211 fiber optic modules. It is therefore necessary to have one "new" 3952 for every few "old" ones, or else the link will develop occasional errors. The exact ratio of "old" to "new" has not been determined. The DAS links are byte-serial.