JORWAY CORPORATION

Instruction Manual
Model 411S
SCSI Bus CAMAC Highway Driver

Model 411S 2572
Serial No. 432

Second Edition 2.0

The Jorway Corporation
27 Bond Street
Westbury, NY 11590
(516)-997-8120

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1.0 Introduction

This manual describes the installation, operation, and programming of the Jorway Model 411S SCSI CAMAC highway driver. It is assumed that the user is familiar with the CAMAC system, as described in IEEE Standards 583 and 675. Knowledge of the SCSI-2 specification, ANSI Standard X3.131, while not required, will be helpful, especially in writing software using the SCSI message system and interpreting the controller's replies to various SCSI commands.

NOTE:

> To avoid confusion with the software entity of the same name, the Model 411S will be referred to in this document as a "controller" at the risk of confusion with the crate controllers to which it is connected.

2.0 General Description

The Jorway Model 411S is a 3 1/2 inch rack mounted instrument that interfaces a multi-crate CAMAC data acquisition system to any computer supporting the ANSI standard Small Computer System Interface (SCSI) Bus. The CAMAC system can consist of up to seven CAMAC crates on the parallel Branch Highway and up to 63 Crates on the Serial Highway. Models with the Enhanced Serial Driver provide data transfers in special block modes capable of operating at 3 megabytes per second.

The Model 411S is also available as a conversion kit for existing Unibus or Q-bus models in a 5 1/4 inch chassis. Connection to the SCSI bus, and the Serial and Parallel Highway ports is at the rear of the chassis. New Model 411S models are housed in a 3 1/2 inch rack mounted chassis with the SCSI and Highway ports at the front panel. Various configurations are available supporting the CAMAC parallel Branch Highway or the Serial Highway or both.

Model 411-2429	Parallel Branch Highway
Model 411-2472	Serial Highway
Model 411-2572	Enhanced Serial Highway
Model 411-2472	Parallel Branch Highway and Serial Highway
Model 411-2572	Parallel Branch Highway and Enhanced Serial Highway

Option 1 is available on the Model 411S(which provides a single powered CAMAC module slot). This slot is commonly used to house a Serial U port or Bypass CAMAC module. This allows the Model 411S with Serial Driver to use the identical module that is used in the CAMAC crate. The Option 1 chassis is 5 1/4 inch high(of greater depth than the 3 1/2 chassis) to accommodate the module slot. Other options are also available such as operation on 115 or 230 VAC, 50 or 60 Hz.

A Model 411S can be intermixed with other SCSI devices on a single SCSI port, which can support up to 7 devices. The standard model uses the single-ended protocol, which allows a SCSI bus length of six meters; as an option the differential SCSI bus can be employed to allow a length of 25 meters. The Model 411S has two SCSI-2 low density connectors at the front, allowing SCSI devices to be daisy-chained. If not daisy-chained, one connector is used for a SCSI terminator.

The Model 411S obeys all mandatory requirements in the SCSI-2 specification. All types of CAMAC operations are permitted, including high-speed Block Transfers under hardware control. Any of seven block transfer modes can be selected, including THE ESONE standard modes Address Scan, Q-Stop, Q-Repeat, Stop-on Word as well as Fermilab extended subaddress scan. During block transfers, only data is transferred on the SCSI Bus. For any transfer, the user can elect to transfer either two or three data bytes for each CAMAC cycle. In the latter case, an additional null byte is inserted in the data stream so that 24 bit data is aligned on 32 bit memory boundaries. The order of byte transmission is user selectable as high-order first or low-order first.

4K bytes of data is FIFO buffered within the Model 411S. In addition, the 411S can utilize the SCSI disconnection/reselection protocol and can transfer data at a rate of 10 Mbytes/sec on the SCSI bus in synchronous SCSI mode. It can, therefore, acquire a block of data at CAMAC speed up to 3 Mbytes/sec while disconnected from the SCSI bus, and then connect to the SCSI bus and transfer the data at the higher rate. This allows efficient use of the SCSI bus bandwidth, which may be shared with other devices such as disks. CAMAC transfers are not interrupted by the disconnection/reselection process, but proceed continuously until the transfer length is satisfied. The burst size, i.e., the number of bytes transferred on the SCSI bus after a reselection, is user selectable at 1/8, 1/4, or 1/2 of the FIFO buffer size, which itself can be increased to 32 Kbytes.

Modules asserting LAM's can interrupt the computer using the SCSI Asynchronous Event Notification (AEN) protocol. In the course of this protocol, the Model 411S becomes a (temporary) SCSI Initiator, selects the host adapter as a Target, and sends the pattern of asserted LAM's to the host. If this protocol is enabled, and a LAM occurs on the parallel Branch Highway, a GL operation is automatically performed, and the result transferred in 4 bytes. If the LAM is from the Serial Highway, the contents of the serial demand stack is transmitted. For this protocol to be successful, the host adapter must be capable of acting as a SCSI target. Alternatively, the user can perform a GL operation or read the serial demand stack by performing a CAMAC read addressed to parallel or serial crate 0.

The top PC board in the S411 has a single 8-position DIP switch and 3 straps that must be positioned (on posts) before operation. Switches 1(LSB) - 3(MSB) establish the binary encoded SCSI ID of the 411S. An "ON" switch represents a binary 0. Switches 4 - 6 are presently used. Switches 7 & 8 and two straps (pushed on posts) determine the burst size (see above) as a fraction of the FIFO buffer capacity. The following are valid combinations:

Sw#8	Sw#7	Fraction	Straps
on	on	1/8	X8-X9, X14-X15
on	off	1/4	X6-X7, X12-X13
off	on	invalid	
off	off	1/2	X4-X5, X10-X11

A strap between post X17 and either X16 (little endian) or X18 (big endian) determines the order of byte significance during data transfers. Systems from Digital Equipment Corp. transmit and expect the least significant byte of a data word first (little endian). Systems based on Motorola processors, Sun, and most VME hosts are the opposite.

The SCSI bus must be terminated at both ends by resistor networks or their equivalents, which requires power. A wire in the SCSI cable is dedicated to this purpose. The SCSI Standard states that this line must be powered by all SCSI "Initiators". The Host interface normally serves this function as well as providing back termination of the Bus. Therefore, a SCSI terminator plug must be inserted in the unused bus connector of the last device on the Bus. The model 411S is capable of powering the SCSI terminator, but this feature is normally disabled.

3.0 Programming

In order to issue a command to the Model 411S, the host interface must perform the following tasks in the appropriate SCSI Bus phase. Many of these tasks are automatically performed, in a fashion transparent to the user, by the port driver provided by many processor vendors.

1. Bus Arbitration
2. Select the Controller
3. Send the Identify message
4. Send the Command Descriptor Block

5. Send or Receive Data
6. Receive the Status Byte
7. Receive the Command Complete Message

Bus Arbitration is only required if there are devices on the bus, other than the host interface, that might become SCSI Initiators. Note that the Model 411S Controller can become a (temporary) Initiator for the purpose of transmitting a LAM message. Therefore, arbitration by the host is required if LAM's are enabled. The hardware of the host SCSI interface normally performs the Arbitration procedure, but this can be skipped if there are no other potential Initiators.

The Controller is selected by asserting the SCSI Data line corresponding to the Controller ID together with the SCSI SEL signal. The line associated with the host ID may optionally be included. The selected Controller will respond by asserting the SCSI BSY signal and enter target mode. The SCSI target determines the type and direction of data transfer on the bus by controlling the signals C/D, I/O, and MSG. These signals determine the bus "Phase" in accordance with the following table:

Phase	C/D	I/O	MSG
Command	1	0	0
Data Out	0	0	0
Data In	0	1	0
Status	1	1	0
Message Out	1	0	1
Message In	1	1	1

The "In" direction indicates a transfer from the target to the Initiator (controller to host). The host interface, acting as Initiator, should monitor the bus phase and send or receive the type of data requested by the target. Since the sequence of bus phases is normally known to the host, an anomalous phase is indicative of an error condition. The Message Phases are used for physical path management and to recover from error conditions.

In accordance with the SCSI-2 specification, the host should select the model 411S with the ATN signal asserted, causing the controller to enter the Message Out phase initially. The Controller then expects the host to send a one byte IDENTIFY message that selects the logical unit within the target. This message is described in section 7.

NOTE:

The Model 411s does not at present support SCSI "queue tagging", so 3-byte IDENTIFY messages will invoke an error indication.

If the host continues to assert ATN, the Controller will remain in Message Out phase, and the host may send another message such as a SYNCHRONOUS DATA TRANSFER REQUEST. When ATN is no longer asserted, the Controller enters Command Phase and expects the host to send a Command Descriptor Block. The following commands are accepted by the Model 411S:

1. INQUIRY
2. TEST UNIT READY
3. REQUEST SENSE
4. CAMAC Commands

The Command Descriptor Blocks accepted by the Model 411S are either 6 or 10 bytes long and will be described in the next section. Following the Command Phase, the Controller will enter Data Phase if the command involves a data transfer, is valid, and contains no errors. Following this, the Controller will

enter Status Phase and send one byte of status. If the command is invalid, does not involve a data transfer, or for some reason cannot be performed, the Controller will proceed directly from Command Phase to Status Phase. Only three possible status bytes are generated by the Model 411S:

Value	Status
0	GOOD
2	CHECK CONDITION
4	CONDITION MET

CHECK CONDITION status indicates an error. The REQUEST SENSE command may be used to determine the cause. CONDITION MET status is used to return the value of the CAMAC Q signal during a CAMAC command. A status of 4 indicates Q = 1, 0 indicates Q = 0. Following the Status Phase, the Controller will enter Message In phase and send a single null byte(as required by the standard); it will then cause the bus to go free. Linked commands are not presently supported by the Model 411S.

3.1 INQUIRY Command

The INQUIRY command may be issued at any time to determine the characteristics of any logical unit on any target. Thirty-six bytes of information are returned indicating the type of device attached, the manufacturer, model number, and revision level. This command is generally issued by an operating system at start-up but may be issued by a user. The Command Descriptor Block is as follows:

INQUIRY Command

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code (12h)							
1	Logical Unit Number			Reserved				EVPD
2	Page Code							
3	Reserved							
4	Allocation Length							
5	Vendor Specific			Reserved			Flag	Link

All reserved fields in all SCSI commands must be zero. In accordance with the Standard, the Model 411S will reject any command violating this rule. The only valid Logical Unit Number for the Model 411S is 0. The EVPD, Page Code, Vendor Specific, Flag, and Link fields must also be 0. The Allocation Length is the number of data bytes that the host expects the Controller to return and is typically 36 (decimal) but may be less (in which case the returned data will be truncated).

The data returned by the Model 411S conforms to Table 7-15 of the SCSI Standard. The Peripheral Device Type will be 1 Fh. The Peripheral Qualifier will be 000b. If a non-zero logical unit is specified in the preceding IDENTIFY message, the Peripheral Qualifier will be 011b. The INQUIRY command will return GOOD Status-unless an improper bit is detected in the Command Descriptor Block.

3.2 TEST UNIT READY Command

The TEST UNIT READY command is a rapid way to determine, if the Controller is ready to accept data transfer commands, since there is no associated data phase. The TEST UNIT READY command returns GOOD status if the Controller is ready. There is one situation in which it may not be ready and will return CHECK CONDITION status in response to this command: the UNIT ATTENTION condition. The UNIT ATTENTION condition is established at power-up by SCSI Bus Reset or by receipt of a BUS DEVICE RESET message. While the UNIT ATTENTION condition exists, CAMAC commands and the TEST UNIT READY command return CHECK CONDITION status, and CAMAC commands cannot execute. After this status is transmitted, a "Contingent Allegiance" is said to exist, and the UNIT ATTENTION is cleared. A REQUEST SENSE command, if issued at this time, would return a Sense Key indicating UNIT ATTENTION. Note that the sense data is cleared after a REQUEST SENSE command, or if another TEST UNIT READY or CAMAC command is issued.

NOTE:

The Model 411S will be ready to process SCSI commands within 50 microseconds of power-up or reset. It will, however, be in the Unit Attention condition, which must be removed before CAMAC transfers can take place (including CAMAC non-data commands). This can be done by issuing a single TEST UNIT READY command (which will return Check Condition status). It is not necessary to issue a REQUEST SENSE command, but if this is not done an error in the command itself will go undetected. Conservative practice is to issue TEST UNIT READY commands until GOOD status is returned.

The format of the TEST UNIT READY command follows:

TEST UNIT READY Command

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code (00h)							
1	Logical Unit Number			Reserved				
2	Reserved							
3	Reserved							
4	Reserved							
5	Vendor Specific		Reserved				Flag	Link

The Logical Unit field, Reserved fields, and all fields of byte 5 should be 0. If any are non-zero, CHECK CONDITION status will be returned and a Sense Key of "illegal request" established for a future REQUEST SENSE command. A similar result will be obtained if the preceding IDENTIFY message specified a non-zero logical unit. The two conditions differ in the "Additional Sense Code", as noted later.

3.3 REQUEST SENSE Command

The REQUEST SENSE command is normally issued, after a CHECK CONDITION status is returned by any command, to determine the reason. The format of the Command Descriptor Block follows:

REQUEST SENSE Command

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code (03h)							
1	Logical Unit Number			Reserved				
2	Reserved							
3	Reserved							
4	Allocation Length							
5	Vendor Specific		Reserved				Flag	Link

Bytes 1,2,3, and 5 should be 0, or the command itself will return CHECK CONDITION status ("illegal request"). The Allocation Length is the number of bytes the host expects in reply. The Model 411S normally returns 16 (decimal) bytes of sense data(using the format and codes specified in the Standard). The reply format follows.

Sense Data Format

Bit / Byte	7	6	5	4	3	2	1	0
0	Valid	Error Code (70h)						
1	Segment Number (0)							
2	0	0	0	0	Sense Key			
3	0							
4	(MSB)							
	Word Count Defect							
6								(LSB)
7	Additional Sense Length (8)							
8	Main Status Register							
9	(MSB)							
	Serial Status Register							
10								(LSB)
11	0							
12	Additional Sense Code							
13	0							
14	C7	C6	C5	C4	C3	C2	C1	N16
15	N8	N4	N2	N1	A8	A4	A2	A1

The following Sense Keys may be returned by the Model 411S:

Sense Key	Description
0h	NO SENSE- No specific sense key is available. This would be the case, if a REQUEST SENSE were issued after a successful command.
4h	HARDWARE ERROR- Parity error during data transfer or CAMAC module did not return X signal.
5h	ILLEGAL REQUEST- A non-zero logical unit was selected, or a command was issued that is not implemented or contained an improper bit (possibly in IDENTIFY msg.)
6h	UNIT ATTENTION- The Controller has been reset.

9h SHORT TRANSFER- A stop-mode block transfer did not transfer the expected number of bytes, because a CAMAC cycle failed to return the Q signal.

0Bh ABORTED COMMAND- Target aborted the command, usually because the host detected an error and informed the driver by the SCSI message.

In those cases where the sense key leaves some doubt as to the exact cause of an error, the Additional Sense Code provides more specifics. The following ASC's from the SCSI-2 Standard may be encountered:

00h	No additional sense information.
20h	Invalid Command Operation Code.
24h	Invalid field in CDB.
25h	Logical unit not supported.
29h	Power on reset or Bus Device Reset occurred.
3Dh	Invalid bit in IDENTIFY message.
44h	CAMAC Cycle did not return X_=1.
47h	SCSI Parity error.
80h	CAMAC cycle did not return Q_=1.

The word count deficit is the number of CAMAC words not transferred. It will be non-zero in the case of an error, or if a stop-mode transfer is terminated by Q failure. More detailed information concerning specific CAMAC errors, particularly those detected on the serial highway, can be obtained from other fields in the sense data. These fields will be discussed later under the heading of "errors".

3.4 CAMAC Commands

The SCSI Standard does not provide for a device like a CAMAC highway controller. Therefore, non-standard Command Descriptor Blocks are used following the IDENTIFY message of the SCSI-2 specification. Both 6 and 10 byte commands are used; the former for non-data transfers, and the latter for data transfers.

3.4.1 CAMAC Non-Data Commands

A CAMAC non-data command has a function code between 8 and 15, or between 24 and 31 (the F8 bit set). The Command Descriptor Block for a non-data CAMAC command consists of 6 bytes, as follows:

CAMAC NON-DATA Command

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code (0C1h)							
1	Logical Unit Number			F16	1	F4	F2	F1
2	0	0	0	N16	N8	N4	N2	N1
3	0	0	0	0	A8	A4	A2	A1
4	S/P	C7	C6	C5	C4	C3	C2	C1
5	Control Byte (0)							

The logical unit must be 0, or an error will result. The S/P bit is set to 1 for operations on the CAMAC serial highway if this option is installed in the controller. If this bit is 0, an operation on the parallel branch highway will result.

NOTE:

> Unlike Unibus and Q-Bus versions of the Model 411, 7 crates can exist on the parallel highway even if a serial highway is simultaneously active. The PAR ONLY switch found on these units is inactive or omitted in the SCSI units.

After the command is executed, the Controller proceeds to the Status Phase and returns one of the following status bytes, then the Command Complete message (which is null):

Status Byte	Description
0	GOOD Status, Q_=0
2	CHECK CONDITION (Error)
4	GOOD Status, Q_=1

If CHECK CONDITION status is returned, the REQUEST SENSE command may be issued to determine the reason.

3.4.2 CAMAC Data Transfers

CAMAC data transfers use the same Operation Code (Byte 0) for reads and writes-unlike other SCSI commands. The distinction is conveyed in the CAMAC Function Code within the Command Descriptor Block. Data transfers may made in either 16 or 24 bit mode. The former only transfers data on the low order 16 data lines of the CAMAC Dataway; therefore, it requires only two bytes to transfer a CAMAC word on the SCSI Bus. In 24 bit mode, all Dataway data lines are used, and three bytes are required for each Dataway cycle. In order to align memory data on full word boundaries in 24 bit mode, a null byte is inserted in the SCSI data stream as the most significant byte of each CAMAC word transferred. Transfer lengths are always stated in bytes; therefore, it will be two or four times the number of CAMAC words involved.

NOTE:

When using 16-bit mode Inexperienced CAMAC users are often disturbed to find non-zero bits appearing on the high order eight Dataway write lines (W17-W24). This is unavoidable, as the Dataway is "hard-wired" to use 24 bits. If it is desired to use 16-bit mode with modules sensitive to all 24 bits, a single 24 bit write command may be issued with a null high order byte. Following this, 16 bit mode may be used, and the high order bits will be 0.

CAMAC data transfers use a 10 byte Command Descriptor Block as follows:

CAMAC Data Transfer Command

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code (E1h)							
1	Logical Unit Number			Reserved				
2	0	0	BS	F16	0	F4	F2	F1
3	M3	M2	M1	N16	N8	N4	N2	N1
4	0	DD	SCS	SNXC	A8	A4	A2	A1
5	S/P	C 7	C 6	C 5	C 4	C 3	C 2	C 1
6	(MSB)							
...	------			Transfer Length				--------
8								(LSB)
9	Control Byte (0)							

The BS bit is set to 1- for 24-bit CAMAC transfers, in which case 4 bytes will be transferred on the SCSI bus for each CAMAC word. If a scan mode transfer attempts to advance out of the starting crate, the SCS bit sets single crate scan mode, causing an error halt. The SNXC bit ("skip non-existent crates") permits a scan to pass over non-existent crates on the parallel highway. If it is not set, a time-out error will result when a non-existent crate is addressed. It does not apply to the serial highway. (The SCS and SNXC bits replace the switches found on Unibus and Q-Bus versions of the Model 411.)

The S/P bit selects between the serial or parallel CAMAC highway, as noted above. Bytes 6 through 8 specify the transfer length IN BYTES, which may be as long as 16 Mbytes. The DD bit disables SCSI disconnection and reselection on a command by command basis, although this function is normally performed by operating system level software.

3.4.3 Block Transfer Modes

The M3 M2 and M1 bits specify the mode of transfer. Models with Enhanced Serial Drivers (411S-2572 and 411S-2573) have two additional modes for enhanced serial transfers as well as an additional Q-Ignore transfer mode. Enhanced serial transfers require a type L-2 crate controller supporting Enhanced operations such as the Jorway Model 174 (L-2 controller with Block Modes).

The M3 M2 and M1 bits specify the mode of transfer as follows:

M3	M2	M1	Models -24XX Transfer Mode	Models 25XX (Enhanced Serial) Transfer Mode
0	0	0	Q-Stop	Q-Stop
0	0	1	ECA	ECA
0	1	0	Q-Repeat	Q-Repeat
0	1	1	Address Scan	Address Scan
1	0	0	Zen Mode	Enhanced Serial Block Mode , Q-Stop
1	0	1	not assigned	Enhanced Serial Block Mode, Q-Ignore
1	1	0	not assigned	Q- Ignore (non Enhanced)
1	1	1	Stop-on-Word	Stop-on-Word

In Address Scan mode, consecutive Subaddresses are addressed until either Subaddress 16 is finished or a CAMAC cycle returns Q_=0. The Station number is then incremented, and the process continues. ECA mode is similar to Address Scan with the following difference: although subaddresses increment (module 16), station increment occurs only when Q=0. Zen mode is similar, except that the subaddress is fixed at 0. ECA mode is included for compatibility with existing models of the Model 411S.

In Q-Stop, Q-Repeat, or Stop-on-Word mode, the Station, and Subaddress remain fixed at the initial value. In Q-Stop and Stop-on-Word, the transfer terminates if Q = 0. In the former mode, data from the cycle giving Q = 0 is not transferred; in the latter, it is. Stop-on-Word is useful for single word (2 or 4 byte) reads of module status registers(which often do not return Q), or block reads of memories that drop Q on the last valid word.

In repeat mode, data is not transferred if Q = 0, but CAMAC cycles continue. All transfer modes terminate if the transfer length is satisfied or an error occurs, and the Controller proceeds to the Status Phase. Note, it is not possible to transfer an odd number of bytes of CAMAC data, although an odd transfer length is permissible for the INQUIRY or REQUEST SENSE commands.

In Enhanced serial block operation two modes are available, Q-Stop and Q-Ignore. Enhanced Q-Stop serial block mode operates with read or write commands and will terminate the block transfer on either (1) a Q = 0 response from the module during the serial block operation , (2) transfer length satisfied or (3) error. Because there will be serial operations in the serial highway pipeline when any of these conditions occur additional operations may be performed at the module which cannot be accounted for (Overrun). Enhanced Q-Ignore serial block mode operations count the transfers being requested on the serial highway instead of transfers completed as is done in Q-Stop. When the requested wordcount is satisfied, the transmitted commands for dataway operations at the crate controller terminate. As a result there is no Overrun at the module. The receiver portion of the serial driver waits for the operations in the serial pipeline to complete and if no errors are detected (i.e. parity checksum OK), the block transfer is completed successfully. If errors occur during the block transfer , operations at the module may be indeterminate. Operations in Enhanced serial block mode Q-Ignore return status of Q = 0 for all operations.

4.4.4 CAMAC Errors

CAMAC data transfer commands return only three possible status bytes, as noted above. If the transfer terminates with X or Q equal to 0, or an error is detected on the serial or parallel highway, CHECK CONDITION status (2) will be returned any time the transfer length is not satisfied. In this case, the REQUEST SENSE command can be issued to determine the cause of termination, and the number of bytes successfully transferred. Please refer to the 3.3 for the format of the data returned, and a brief discussion of errors. For more complex errors, particularly those detected on the serial highway, the main status register

and serial status register should be examined. It was noted that bytes 4 through 6 indicate the number of CAMAC words that failed to be transmitted between the controller and the CAMAC system. It is stressed that this value is in terms of CAMAC WORDS(16 or 24 bit) instead of bytes. (In the case of CAMAC writes, the word incurring the error will be counted as transferred.)

Byte 8 of the sense data contains the following flags:

Bit	Name	Significance
7	NO_Q	Module returned Q_=0
6	NO_X	Module returned X_=0
5	TO	Time-out on parallel or serial highway
4	CRTO	Crate overflowed (SCS set)
3	SNEX	Command not executed on serial highway
2	BDSQ	Branch Demand Sequence set
1	DSNE	Serial Demand Stack not empty
0	BDMD	Branch Demand present

Only the high-order 5 bits are associated with errors and are self-explanatory. The low order 3 bits pertain to LAM's on the serial or parallel highway and will be discussed in the next section. If SNEX is set, it is known that the serial operation definitely did NOT take place at the addressed crate, and a retry can be attempted. For either SNEX or TO from a serial operation, the Serial Status Register, sense bytes 9 & 10, can be used to establish further details on the type of error. Considered as a 16 bit register, the bits have the following significance:

BIT	MNEMONIC	SIGNIFICANCE
15	SNEX	Serial No Execution (see above)
14	RNRG1	Reply not recognized (length > 1)
13	RNRE1	Reply not recognized (length = 1)
12	CMDFOR	Corrupt Command Format
11	HDRREC/	Truncated Command Header Received
10	RPE	Parity Error in Reply
9	TIMOS	Serial Time-out
8	CRET	Command type message detected at receiver
7	DERR	Delayed Error bit set in reply
6	RERR	Error bit set in reply
5	LOSYN	Sync lost while awaiting reply(Bit Mode only)
4	SYNC	Receiver has lost Byte Sync(Bit Mode only)
3	SPARE or LASTX	Unused bit on Serial Drivers Board type A5111 LASTX on type A5178 (Enhanced Serial Driver)
2	HNGD	Hung Demand message received
1	DALISQ	Demand Alarm interrupt
0		Not used

As the setting of SNEX indicates that a serial operation was not performed at the addressed location, in most cases references to this bit alone will indicate what action should be performed, i.e., repeat CAMAC operation N number of times before declaring a failure. Reference to other bits may also be made to indicate the reason for SNEX. Possible combinations are:

1. CRET and SNEX	Command message returned not claimed by any crate controller. Good transverse and longitudinal parity occurred up to and including Sum byte.

2. RERR and SNEX	Indicate Error Reply message detected with Error bit set to "1" and good parity in Error Reply.
3. TIMOS and SNEX	Indicate that Serial Time-Out occurred before serial transmitter began its operation. Normally, it indicates that a receiver did not have sync in Bit Mode and the transmitter was therefore prevented from starting.

Other status register bits may also be set along with SNEX because of garbage bytes occurring on the highway. SNEX, however, indicates a positive indication that no CAMAC command was executed.

Byte 14 of the sense data returns the final Crate number in the 7 most significant bits, and the value of N16 in the least significant bit. Byte 15 returns N8-N1 in the hi-order nibble, and A8 - A1 in the low-order nibble. In the case of an Address Scan terminated by an error, the CAMAC address will have been bumped.

4.4.5 Commands to Crate 0

Commands to CAMAC crate 0 are used for system wide purposes such as enabling/disabling asynchronous LAM's, and polling for LAM's. An F(26) command to serial or parallel crate 0 will enable LAM's from the respective highway to signal the host asynchronously, as described in the following section . An F(24) command disables them. Recall that the host adapter must have target capability for the AEN procedure to work. An F(0) command to parallel crate 0 will result in a branch GL operation, and either 2 or 4 bytes will be sent to the host, using the byte order selected for data transfers. When a demand is received on the parallel highway, the Branch Demand Sequencer is set. It is reset by a read of parallel crate 0 or by the AEN procedure to be described. In addition, the BDMD bit in the main status register is a live indicator of the state of the parallel highway D line.

An F(0) command to serial crate 0 will transmit the entire contents of the serial demand stack to the host. In this case, the number of bytes to be sent is not known to the host in advance, but can be determined by the host software. In the case of a serial F(0) LAM poll, the high-order byte of each word in the demand stack is sent first, regardless of the strap-selected byte order. The 16 bits of the Serial Demand Stack word have the following significance:

BIT	MNEMONIC	SIGNIFICANCE
15	DSE	Demand Stack Empty ,complement of DSNE (see above)-it will read as 0 for a valid demand
14	SCR32	Demand Crate Address MSB
13	SCR16	Demand Crate Address
12	SCR8	Demand Crate Address
11	SCR4	Demand Crate Address
10	SCR2	Demand Crate Address
9	SCR1	Demand Crate Address LSB
8	SGL5	Demand SGL Pattern
7	SGL4	Demand SGL Pattern
6	SGL3	Demand SGL Pattern
5	SGL2	Demand SGL Pattern
4	SGL1	Demand SGL Pattern
3	SDN8	Demand Number MSB
2	SDN4	Demand Number
1	SDN2	Demand Number
0	SDN1	Demand Number LSB

Demand number N indicates that there are N demands in the stack. Since a read of serial crate 0 reads the entire stack, the demand numbers will be a decreasing sequence-unless a demand arrives while the stack is being read.

5.0 Asynchronous Event Notification

If LAMs are enabled as described above, and a LAM arises in an enabled CAMAC module, the Model 411S will become a temporary Initiator and will inform the host at the next opportunity-using the SCSI-2 AEN procedure. It will arbitrate for the bus, select the host SCSI adapter, and send the IDENTIFY message followed by the SCSI SEND command. The host adapter must have been programmed to execute the proper Target mode phases. The SEND command instructs the Target (the host adapter) to transfer data from the Initiator (the Model 411S). The data transmitted is the same, as described above, for LAM polls.

6.0 SCSI Messages

The Model 411S responds to the following SCSI messages:

IDENTIFY
ABORT
BUS DEVICE RESET
INITIATOR DETECTED ERROR
MESSAGE PARITY ERROR
MESSAGE REJECT
NO OPERATION
SYNCHRONOUS DATA TRANSFER REQUEST

The IDENTIFY message is the SCSI-2 method of selecting the Logical Unit within a target. If a non-zero Logical Unit is specified in the IDENTIFY MESSAGE, the ensuing command will fail. The IDENTIFY message is one byte long, as follows:

IDENTIFY MESSAGE

Bit	7	6	5	4	3	2	1	0
	1	DP	0	0	0	Logical Unit Number		

It will be noted that there is also a Logical Unit Number field in the Command Descriptor Blocks (described earlier). This field has been maintained in the SCSI-2 Specification for compatibility with SCSI-1. If the Logical Unit is conveyed by the IDENTIFY message, this field in the CDB is not used and should be set to zero. The DP bit is termed disc priv in the SCSI standard and is set to 1 to notify the Target that it is allowed to disconnect from the SCSI bus and later reselect. If this bit is not set, the S411 will perform all transfers possibly in one tremendous SCSI transfer. The DD bit, described earlier, can also negate Disc Priv.

The ABORT message interrupts the currently executing command, and the Controller enters the BUS FREE phase. The BUS DEVICE RESET message causes a hardware reset of the Controller. A Dataway Z is generated, and the UNIT ATTENTION condition is set. LAMs are disabled, and Dataway Inhibit asserted. If synchronous transfers were in effect, the Controller reverts to asynchronous mode.

The INITIATOR DETECTED ERROR message causes the Controller to issue the RESTORE POINTERS message, and then to retry the Data Phase of the current command. The MESSAGE PARITY ERROR message causes the Controller to resend the previous message. The MESSAGE REJECT message

causes the Controller to perform an "unexpected disconnect". This should not occur due to the limited and well defined message repertoire of the Model 411S.

The SYNCHRONOUS TRANSFER REQUEST message causes the Model 411S to prepare to use synchronous transfers in future data phases and to return a similar message confirming the parameters it will use. Synchronous transfers provide a speed improvement during SCSI Data Phases by eliminating the round-trip propagation delay associated with the REQ/ACK handshake. This message is 5 bytes long, as follows:

Byte	Contents
0	1
1	3
2	1
3	Transfer Period
4	REQ/ACK Offset

The Transfer Period is specified in units of 4 nanoseconds. If proposed by the host, the Model 411S can transfer at a 5 Mbytes/sec. rate, and accordingly, returns the value 50 (decimal) in byte 3 or a lower value. A value of 8 is returned in byte 4, unless the host proposed a smaller offset.

The Model 411S generates the following SCSI messages under the appropriate circumstances. The host must be prepared to process them. The second two messages are responses to host messages, and their generation can therefore be prevented.

COMMAND COMPLETE
RESTORE POINTERS
SYNCHRONOUS DATA TRANSFER REQUEST

The COMMAND COMPLETE message is one byte transmitted in MESSAGE IN phase at the completion of every command-after the STATUS Phase. Since the Model 411S does not support linked commands, this message is always NULL. The RESTORE POINTERS message tells the host to reset its data buffer pointer to its initial value, since the Target intends to retry the data transfer phase of the current command from the beginning. The SYNCHRONOUS DATA TRANSFER REQUEST message is only generated in response to a similar message from the host. The Model 411S will not initiate synchronous transfers. All AEN transfers use asynchronous mode.

Since some operating systems are not prepared to accept the MESSAGE REJECT or MESSAGE PARITY ERROR messages, the Model 411S does not generate either. In the event that it receives corrupted or invalid message, it merely disconnects from the bus. This "unexpected disconnect" informs the host that an error has occurred; however, the response to an invalid IDENTIFY message is sent in Status Phase, as noted earlier.

During Asynchronous Event Notification, the Model 411S generates the IDENTIFY message to convey the host's Logical Unit Number(which is expected to be zero). It further expects the host to send the COMMAND COMPLETE message after sending the status byte.

7.0 Serial Highway Operation

7.1 Installation and Hardware Settings

If the Serial Highway Option is installed, either a Bit-Serial or Byte-Serial Highway can be connected to the connectors labeled "D-input" and "D-output". A number of switches will be found on the Serial Highway Driver board, which occupies the lower most slot in the backplane. These switches can be

set through an access door in the front panel of the Serial Highway Driver. They control the following operation parameters. The selections made at shipment should be as listed in the second column.

1. Mode (Bit/Byte)	Byte Mode
2. Number of Stop-Bits(Bit Mode)	1
3. Clock Rate	5 MHz.
4. Excess Space Bytes	9
5. Time-out Interval	64 Bytes
6. Stack Alarm Level	16 Demands

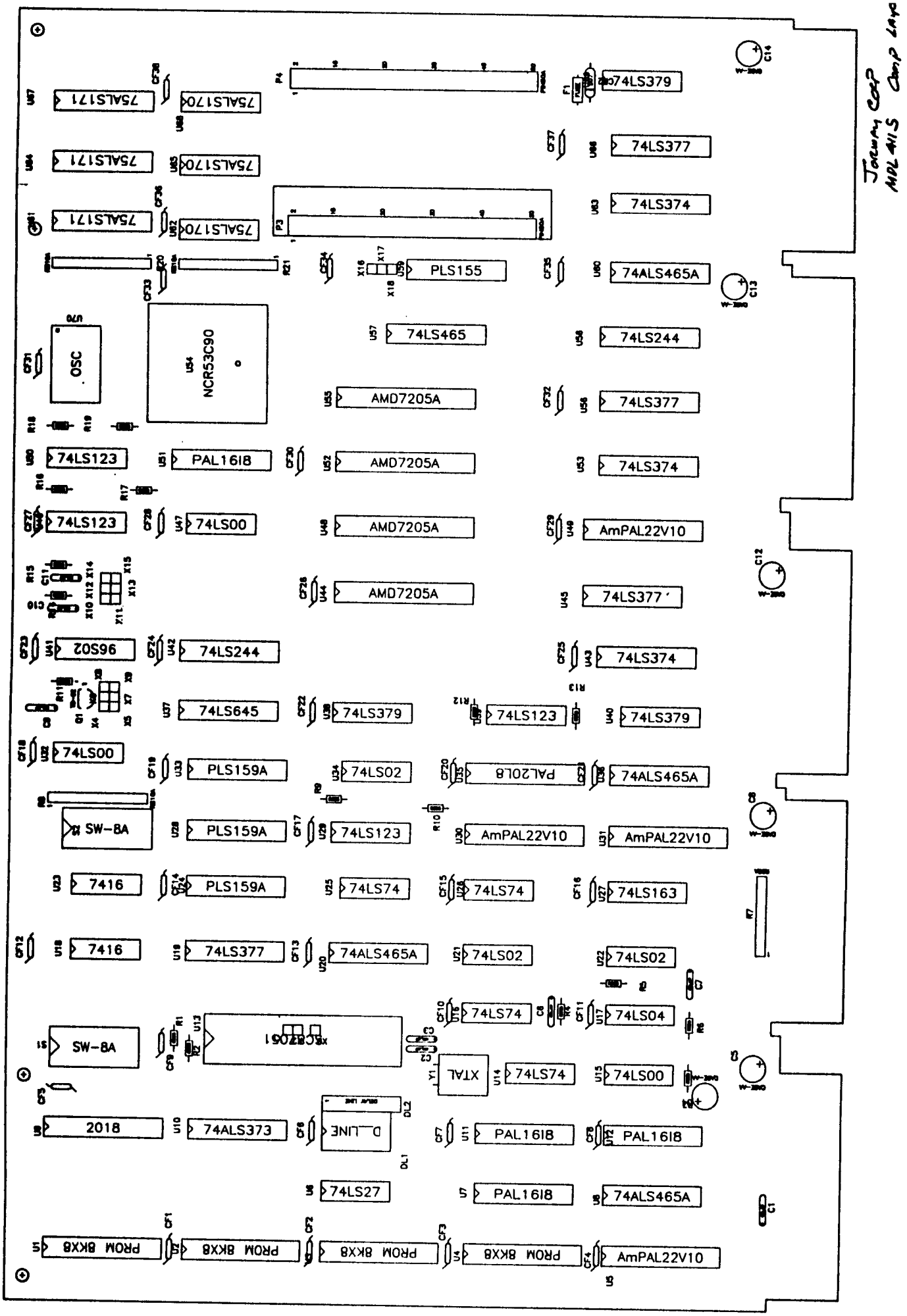
Appendix 1 shows the locations of the switches.

7.1.1 Serial Time-Out

The serial time-out circuits operate in the terms of message bytes instead of real time. This allows the timer to be set for the particular serial highway configuration independent of the system clock rate. To avoid spurious time-out indications, the settings must exceed the maximum number of bytes that can be received under normal circumstances(between the time that a Serial CAMAC operation is commanded and the final byte of the reply received). Factors contributing to this number are the following:

12 Bytes	Longest message transmitted, Command Header to received Endsum.
15 Bytes(max)	Allowance for excess space bytes selected
1 Byte	For each Crate Controller in system
3 Bytes	For each Controller sending demands

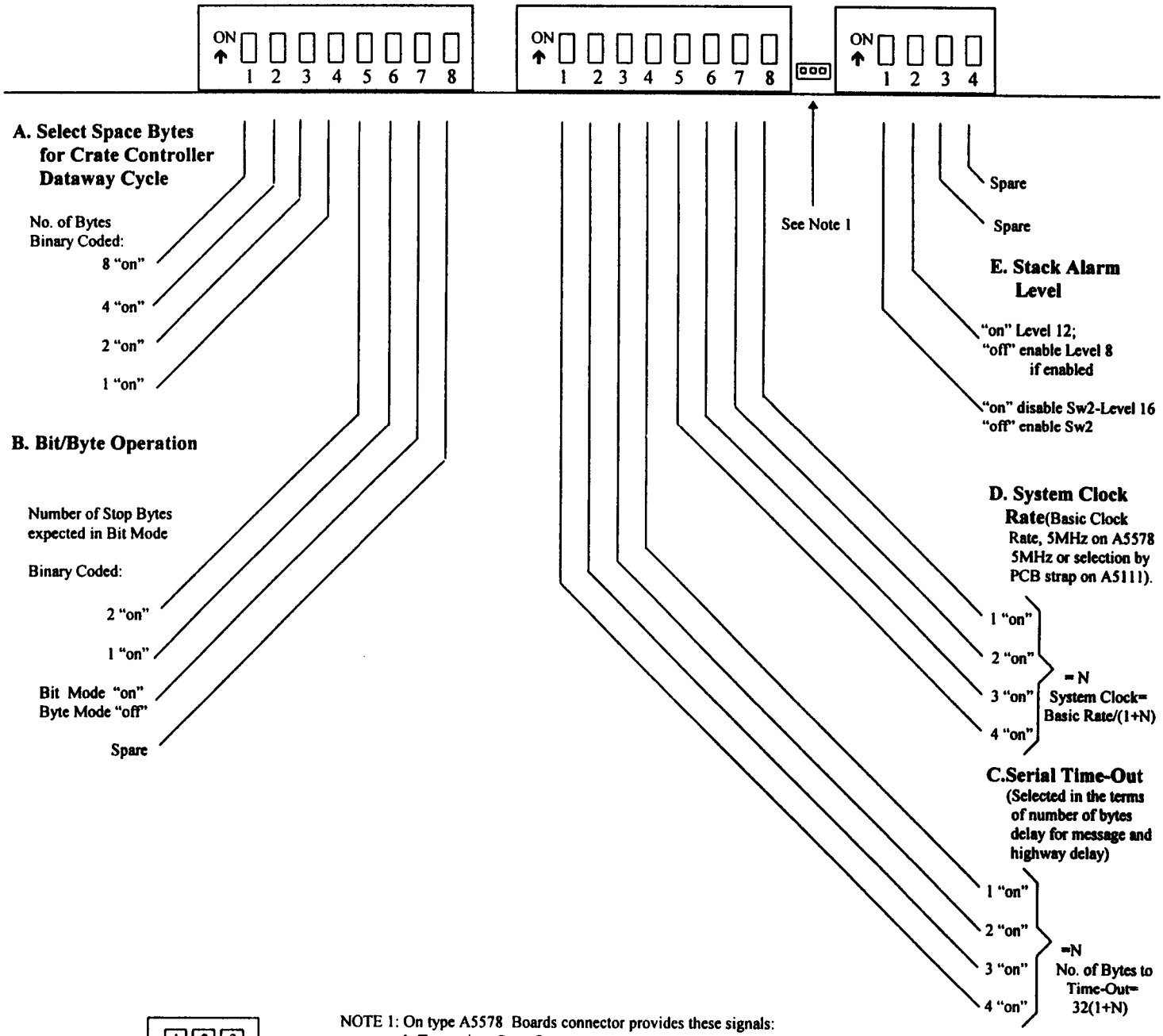
The number of bytes to serial time-out may be selected at 32(1+N) where N is a binary number 0 to 15 selected by a switch on the driver board. During Unbypass and Loop Collapse, the timer is automatically inhibited in order to provide for the required 100ms of space bytes.


Jaguar Corp
MDL 4115 Comp Layout
74LS379
74LS377
74LS374
74ALS465A
PLS155
74LS465
74LS244
AMD7205A
74LS123
PAL1618
74LS00
AmPAL22V10
74LS645
PLS159A
74LS02
74LS163
74LS74
74LS04
74ALS373
74LS27
PROM 8KX8
NCR53C90
OSC
XTAL
SW-8A
2018

Appendix 1

Serial Driver Board
Selector Switches

Edge View



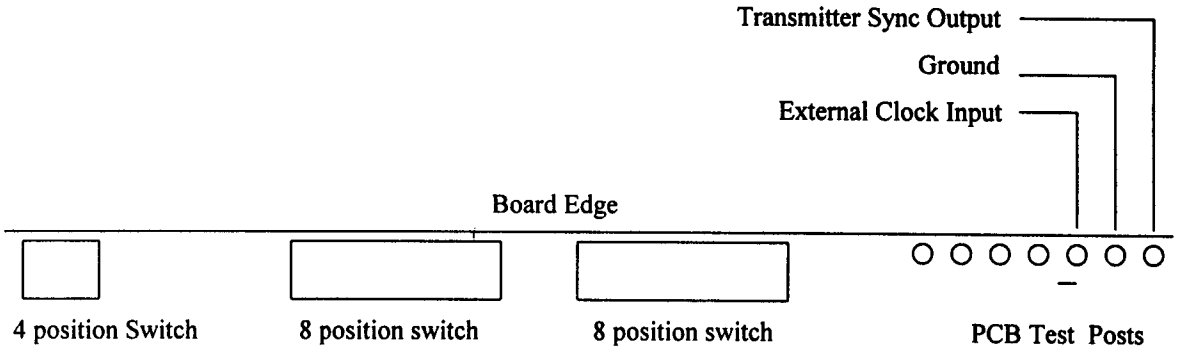
NOTE 1: On type A5578 Boards connector provides these signals:

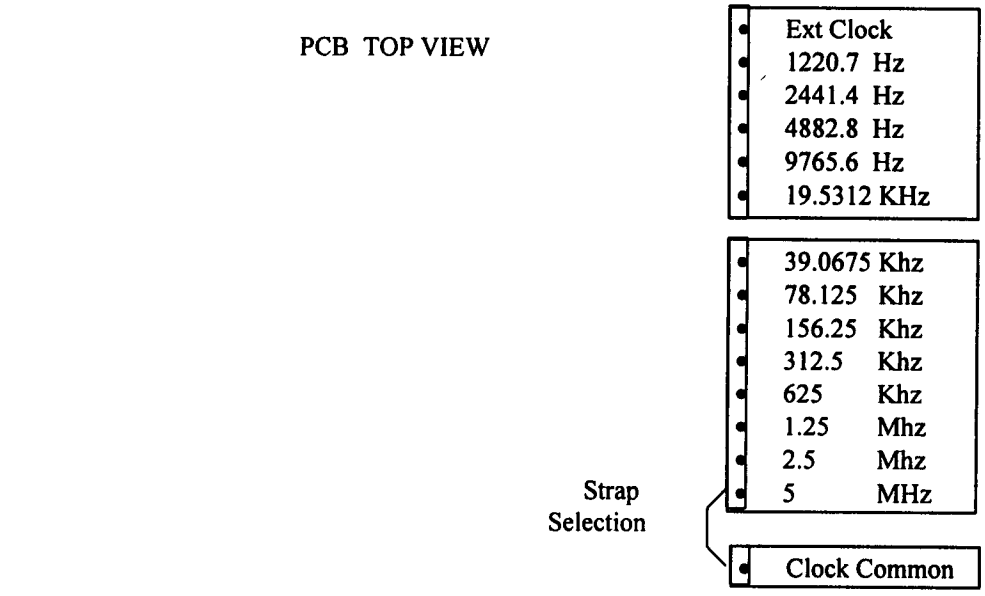
1. Transmitter Sync Output
2. Ground
3. External Clock Input (Function enabled by on - board strap)

Appendex 2

Serial Driver Board (Basic Clock Rate) for Assembly No. A5111 only

The basic clock rate for the Serial Driver board is normally set at 5 Mhz. The board edge selector switches described in Appendex 1 allow for changing the system clock rate to a range of 5 Mhz to 312.5Khz. If a system clock rate lower than 312.5 Khz or an external clock rate is desired straps on the Serial Driver Board are provided for this purpose. The serial driver board must be removed to select these strap positions. The following illustration indicates the available positions :





Appendix 3

Beginning with 411S serial # 430 (Serial Driver Assembly A5578A) Indicator lights are available of the Module Front Panel.

Serial Driver Operation Indicators

Although the Serial Status Register provides comprehensive indications of the status of a serial highway operation four indicators are provided on the front panel to provide a general status for a serial operation.

These indicators are as follows:

READY (Green): This indicator when illuminated indicates that a serial highway clock is present at the D Port Input and if operation is selected for Bit Serial Mode that the receiver is in Byte Sync. Should Byte Sync be lost in Bit Mode or the clock stop for more than approximately 2 Milliseconds the indicator will be turned off.

BUSY (Yellow): This indicator when illuminated indicates that a serial operation in is progress. The light will remain on for the duration of the serial operation for a single cycle or the entire block if in enhanced block transfer mode. The light illumination is stretched to assist is seeing a single operation.

TP BAD (Red): This stretched indicator is illuminated whenever a transverse parity error occurs in the received serial byte stream. Unlike the RPE bit in the Serial Status Register which indicates a transverse parity error only within the received serial highway message, the TP BAD indicator monitors transverse parity within as well as between messages. This is valuable in providing indications on the quality of the serial highway signals. A occasional flashing TP BAD indicator may indicate a noisy highway caused by a bad cable , connector or highway transmitter. Serial operation may seem to operate OK only because the occasional error is outside of a message but in general overall error rates will be poor.

TO (Red): This indicator , TIMEOUT, is illuminated whenever a serial Time-out occurs as a result of a serial operation. The indicator is set if a time-out occurs but will not be cleared until the beginning of the next serial operation. This allows the results of a single operation or a halt on error to provide the fact that a Time-out had occurred. The indicator is also stretched to provide indication of time-out during repetitive operations.

Switch settings used at PPPL