OPERATOR'S MANUAL

MODEL 6810
WAVEFORM RECORDER

January 1990

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INTRODUCTION

READING THIS SAVES TIME

This manual provides installation and operation instructions for the 6810 Waveform Recorder System. It's organized such that technical density builds through ensuing chapters. Your knowledge of modular waveform recording systems should determine where you begin.

Chapter 1 introduces the 6810 in its working environment. This "System" approach adds perspective for the First-time User who could benefit from a detailed overview. For Users with little or no programming experience, we propose our optionally available WAVEFORM-CATALYST® Software as the turnkey solution to your digitizing needs. Chapter 1 also covers module installation, cable attachments, and making signal connections to the 6810.

Chapter 2 contains operating instructions for programming the 6810 module, addressing both CATALYST Users and GPIB<=>CAMAC Programmers. The first half covers WAVEFORM-CATALYST operation. A special "Getting Started: PC Control Using WAVEFORM-CATALYST Software" section contains step-by-step instructions to get CATALYST Users up and running quickly. Next are detailed instructions for operating WAVEFORM CATALYST software.

The second half details CAMAC Operation. A brief introduction of CAMAC precedes "6810 CAMAC Operation". A "6810 CAMAC Command Summary," and "6810 CAMAC Command Details" follow. Special sections on "VERIFY SETUP" command and "TRIGGER and DUAL SPEED CLOCK TIMING" are also included.

Chapter 3 contains a Functional Description of the 6810 and a Block Diagram. Comprehensive 6810 Specifications also appear here.

Appendix A is a Glossary and Appendix B contains a comprehensive programming example wherein LeCroy's 8901A GPIB to CAMAC interface controls a 6810. Appendix C contains a list of suggested 6810 driver controls. Appendix D contains an ASYST program. A selected Index is also included.

UNPACKING AND INSPECTION

LeCroy recommends that the shipment be thoroughly inspected immediately upon delivery. All material in the container(s) should be checked against the enclosed Packing List and shortages promptly reported to the carrier. If the shipment is damaged in any way, please notify the carrier immediately. If the damage is due to mishandling during shipment, you must file

a damage claim with the carrier. Your regional LeCroy field service office can assist with this. LeCroy tests all products 100% before shipping. LeCroy ships all products in packaging designed to protect against reasonable shock and vibration.

Always identify an instrument's specific version by the Engineering Change Number (ECN) on its back panel.

WARRANTY

LeCroy warrants its instruments to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturer's warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Factory or an authorized service facility within the warranty period, only if the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations. All replaced parts and products become the property of LeCroy Corporation.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

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LeCroy Corporation will gladly answer your questions. Call your regional field service office or ATS Sales and Service Division, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977-6499, (914) 578-6038.

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DOCUMENTATION UPDATES

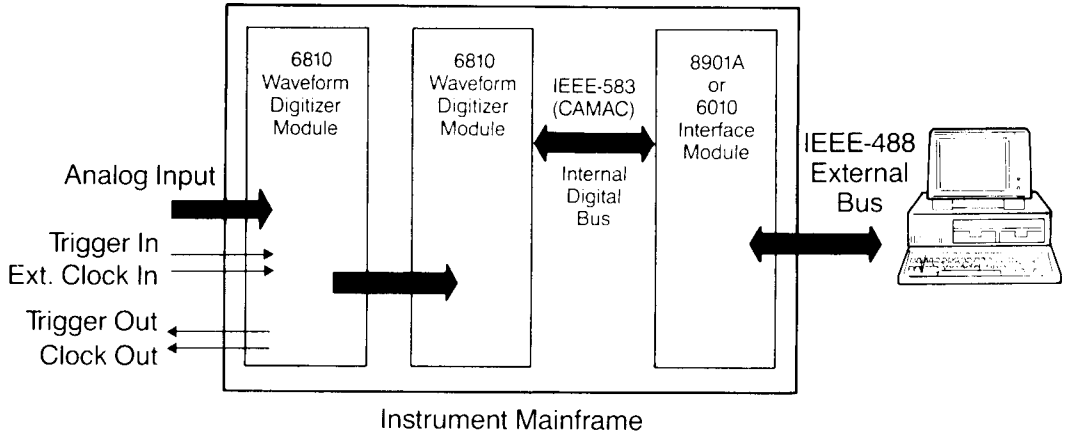
LeCroy continually improves the performance of its products. Addenda may appear in this manual's back sleeve along with any errata.

1 INSTALLATION

PRODUCT DESCRIPTION

6810 Waveform Recorder System Overview

The LeCroy 6810 Waveform Digitizing/Recording system captures entire single-shot waveforms using digital storage techniques. Converting analog waveforms into digital data simplifies waveform analysis and allows storage on floppy disks and hard copies on printers. The system modularity allows channel and memory expansion, and operation with other waveform recorders or accessory modules to match specific applications such as: power monitoring, high voltage testing, noise and vibration testing, geology/seismology monitoring, ballistics/explosives testing, materials studies, biomedical research, power supply testing and other ATE, sonar, radar, ultrasonics, and magnetic media testing.



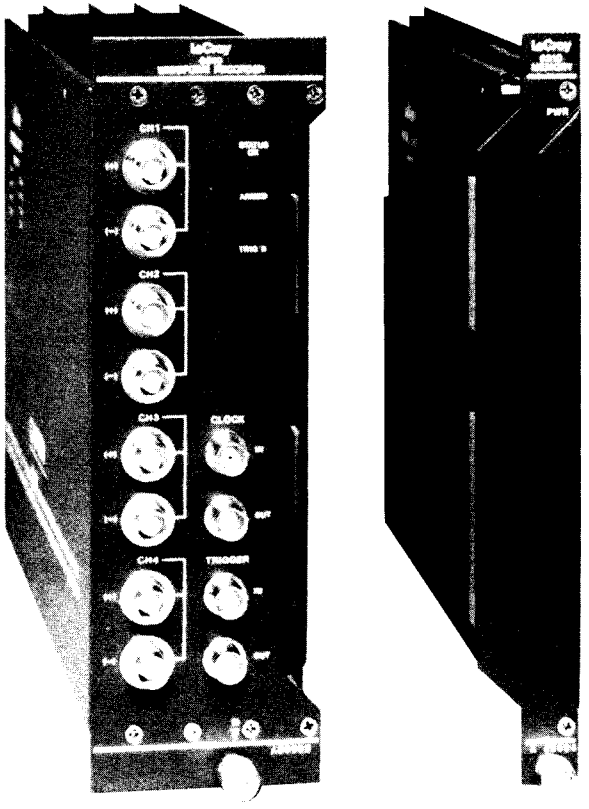
System Architecture

Figure 1

6810 Waveform Recorder

A complete independent recording system, the Model 6810 Waveform Recorder module measures DC to 2.5 MHz signals. The 6810 is a 4-channel, 12-bit waveform recorder with a digitizing and sample rate of up to 5 Megasamples/sec. The 6810's 12-bit analog-to-digital converter provides vertical resolution of one part in 4096 or .025%. Sampling rates can be slowed down

and sped up in the same waveform record using the module's Importance Sampling feature. Each of the four differential input channels provides full scale ranges from 400 mV to 100 V full scale eliminating the need for external signal conditioning.



6810 Waveform Recorder
Figure 2

The 6810 features a built-in 512 ksample memory which is expandable to 8 Megasamples (in 512 ksample increments) by adding the 6310 memory expansion module (See "Adding 6310 Memory Module[s]" page 15). The 8 megasample system supplies a full 8 seconds of continuous recording time at 1 megasample/sec sample rate or more than 6 minutes at 20 ksamples/sec.

The 6810 memory can be divided into a maximum of 1024 segments. Each segment requires a separate trigger to initiate recording. Thus, numerous pulses can be recorded quickly without recording the deadtime between pulses. In this segmented memory mode, the 6810 can record up to 4880 segments per second (5 Ms/sec, 1024 point segment).

The segmented memory mode also helps to precisely reconstruct the timing of intermittent waveforms. The 6810 records the trigger-to-trigger times from segment to segment. The trigger time stamp buffer shows up to 72 minutes between triggers with 1 msec resolution.

All active 6810 input channels use the same trigger. The 6810 module will trigger when the trigger source meets specific waveform conditions or when a software trigger command occurs. Either an external trigger input, the Channel 1 signal, or the Channel 2 signal can act as the trigger source. The 6810 supplies slope, window, and hysteresis triggering.

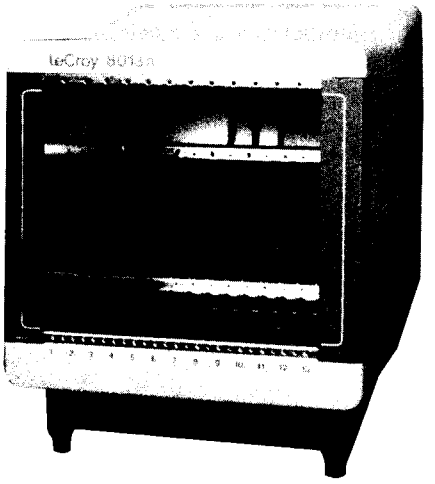
The 6810 conforms to the IEEE-583 Standard (CAMAC). This modularity prevents system obsolescence and ensures simple expandability. The 6810 is totally compatible with the full line of LeCroy modular digitizers and other instrumentation. Other digitizers can augment the system to cover an even wider range of sample rates.

Turnkey Configuration

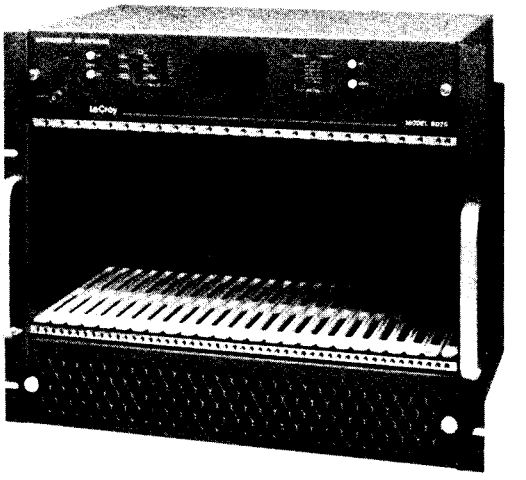
The Model 6810 Waveform Recorder can be purchased in a turnkey 4-channel Century Series™ 2005 Starter System. Or the 6810 module itself can be added into an existing Century Series System for expansion. The Century System includes one 6810 module, an 8013A benchtop mainframe, an IEEE-488 Standard GPIB to CAMAC interface, a GPIB cable and PC-based WAVEFORM-CATALYST™ Oscilloscope software.

IEEE-583 Standard (CAMAC) Instrument Mainframes

LeCroy Benchtop Model 8013A and Rackmount Model 8025 meet all requirements of the CAMAC Standard (IEEE-583), assuring unrestricted choice of modules from LeCroy or second-source CAMAC suppliers. They house the 6810, 6310, and other LeCroy plug-in instrument modules. The 8013A benchtop accepts instruments in combinations of up to 11 single width plug-ins when using a 2 slot controller module. The 8025 rackmount accommodates up to 23 instrument modules when using a 2 slot controller. Both single and multiwidth plug-ins can be accommodated.



8013A



8025

LeCroy Instrument Mainframes
Figure 3

Versatility, user customization, and expandability are the prime advantages of LeCroy CAMAC based systems. Many more functions than could be practically or economically combined in a single instrument are available by selecting the appropriate LeCroy instrument and accessory modules.

PROGRAMMING ENVIRONMENTS

WAVEFORM CATALYST™

WAVEFORM CATALYST™ Software converts an IBM PS/2 or Compaq III/386 and LeCroy digitizers into multi-channel waveform data acquisition systems. The software controls, acquires, displays, averages, histograms, saves/recalls to/from disk, and prints waveforms.

6920-DL DIGITIZER DRIVER LIBRARY and ASYST 3.1

The 6920-DL provides English-like programming commands for LeCroy digitizers and accessories, making all CAMAC (IEEE-583) and GPIB (IEEE-488) commands totally transparent to the user.

ASYST Scientific software converts an IBM PS/2 or Compaq III/386 and LeCroy digitizers into waveform analyzers. Analysis includes +, −, /, x, area under curve, differentiation, filtering, FFT, IFFT, correlation, pulse parameters, curve fitting, interpolation, etc.

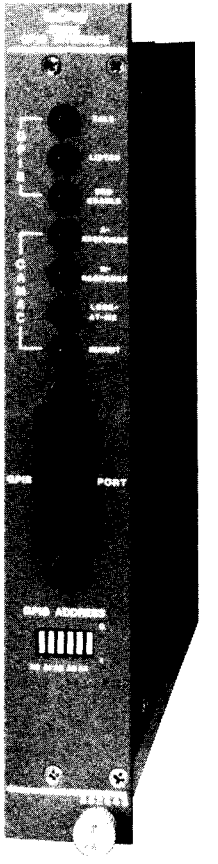
IEEE-488 (GPIB) to IEEE-583(CAMAC) Interface

The 6810 Waveform Recording System employs either the 8901A or 6010 IEEE-488 (GPIB) to IEEE-583 (CAMAC) Interface module. All 6810 functions (gain, offset, coupling, etc.) are programmable and can be controlled remotely. The GPIB to CAMAC interface provides bidirectional communication. A host computer can download control and setup commands to the 6810 and upload waveforms from the 6810. The 8901A interface uploads at up to 225 Ksample/sec; the 6010 at up to 300 Ksample/sec.

8901A GPIB to CAMAC Interface

The 8901A converts a CAMAC mainframe with up to 23 individual instruments into a standard GPIB listener/talker. The 8901A features exceptionally high throughput. Its block transfer

mode allows transfer of all data from a CAMAC module upon receipt of a single talk command at rates up to 500 kilobytes/ sec. The 8901A is fully compatible with LeCroy's Series 6900 WAVEFORM CATALYST Software. Thus, remote control, data transfer, and simple program instruction of LeCroy instrument modules can be achieved employing the user's host controller.



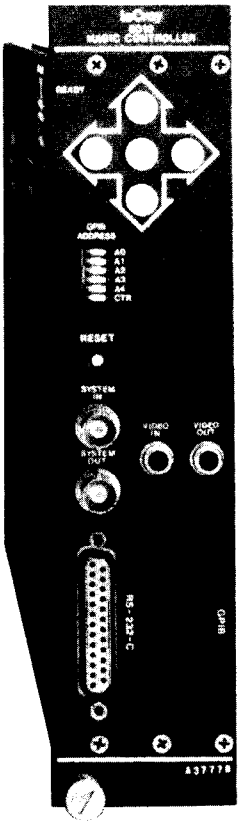
8901A Interface Module

Figure 4

6010 Manual and GPIB to CAMAC Interface

The 6010 MAGIC Controller has been designed to be compatible with the user's host, whether it be a mainframe computer, dedicated instrument controller, personal computer or

RS-232-C terminal. During GPIB operation, the 6010 manages all necessary IEEE-488 protocol, and is both a talker and listener on GPIB. The 6010 can also be accessed via its bidirectional RS-232-C serial port. Users may opt to use both serial and parallel ports during system operation, using the serial RS-232-C port for module setup (keyboard terminal or host) and the parallel GPIB interface for data transfers and interrogation.

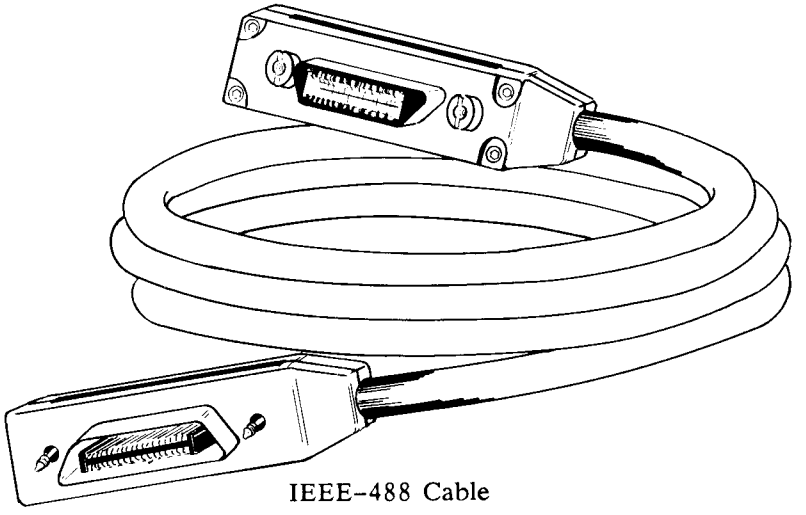


6010 Interface Module

Figure 5

IEEE-488 Cable

An IEEE-488 cable connects the host computer to the CAMAC controller. The cable, often referred to as "bus," contains 16 bi-directional lines to which 15 instruments (including a "controller") can be connected. During operation, the bus lines transfer commands and data to and from the computer to the CAMAC controller and whatever other modules are housed in the CAMAC mainframe.



IEEE-488 Cable

Figure 6

Instrument Controller

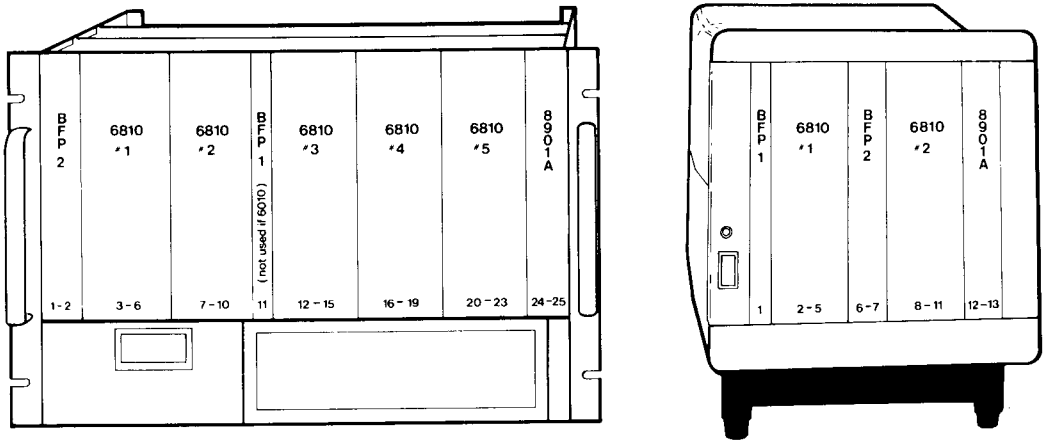
The 8901A and 6010 interfaces are compatible with any IEEE-488 bus controller. However, when using WAVEFORM-CATALYST or ASYST 2.01 Scientific Software, the Instrument Controller must be an IBM PC/XT/AT/PS2 or Compaq III/386.

Note: See WAVEFORM-CATALYST Operator's Manual (Version 2.6 or higher) for a list of compatible multifunction boards, graphics boards, GPIB, expanded memory boards, computers, and printers.

LeCroy's Model 8901A GPIB to CAMAC interface requires the two rightmost slots; LeCroy's Model 6010 GPIB to CAMAC interface module requires the three rightmost slots.

Note: You can install either one or two 6810 modules in an 8013A mainframe or up to five in a 1434A or 8025 mainframe. The mainframe slot pointed to by the arrow on a 6810's front panel is the 6810's "CAMAC N slot number". During bus operation the GPIB to CAMAC interface addresses this CAMAC slot to communicate with the 6810.

To ensure optimal component cooling, install the 6810(s) over cooling fan(s).



Preferred 6810 Installation Slots in 1434A, or 8025, and 8013A Mainframes

Figure 7

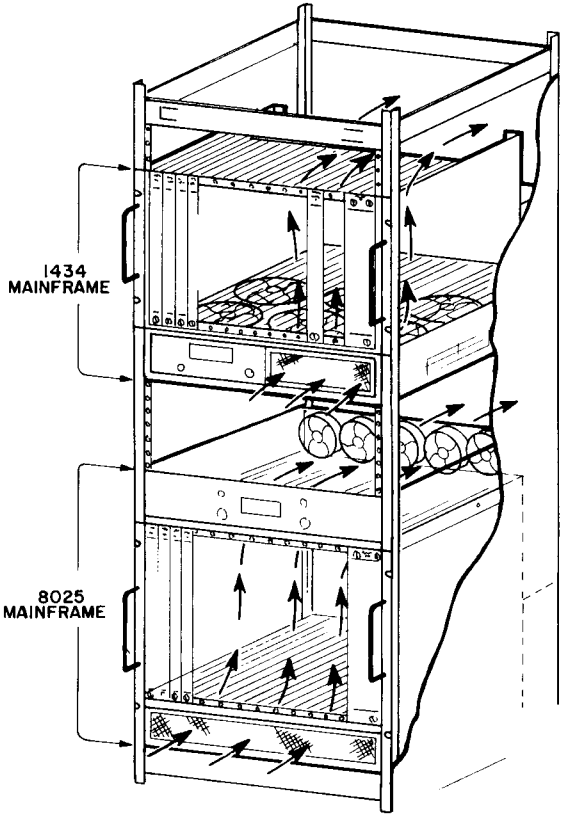
As you slide the module into the mainframe, carefully align its instrument rails with the card cage.

Tighten (clockwise) the thumbscrew on the 6810's lower front panel to draw the module's interface connectors into the mainframe's backplane. Conversely, loosening the thumbscrew retracts the module's interface connectors from the backplane.

Note: When installing a 6810 module in a Model 8013A Benchtop Mainframe, pressing with an upward motion against the 6810's upper front panel to slightly raise the module eases finger tightening.

Ensure that the mainframe has sufficient overhead clearance to permit adequate airflow. *Do not obstruct ventilation.* Blank front

panels (Model BFP–1, BFP–2) can be installed in adjacent slot locations to prevent air flow from bypassing the modular instruments.



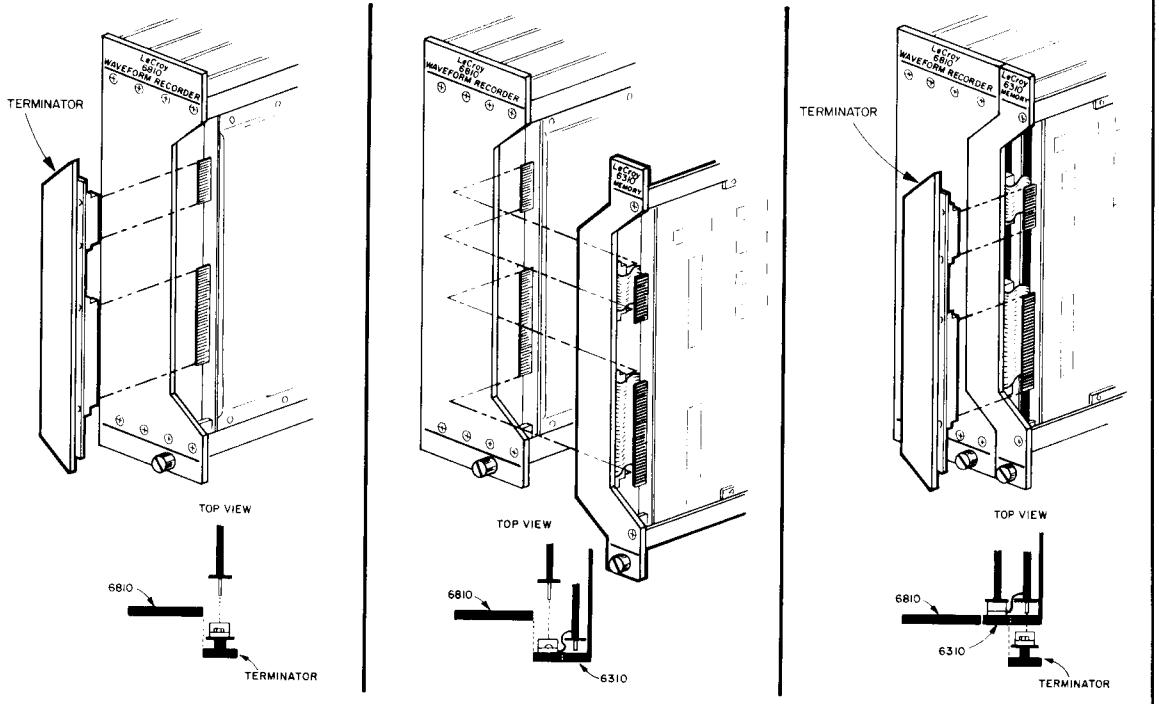
Airflow Path of the 1434 and 8025 Mainframes
Figure 8

Adding 6310 Memory Module(s)

The 6810 provides a built–in 512k sample memory which is expandable to 8 megasamples (in 512k sample increments) by adding 6310 memory expansion modules. The exclusive interlocking mechanical design of the 6810 and 6310 allows simple memory expansion without external cabling.

Prior to 6310 installation WITH POWER OFF, the slot to the right of the 6810 must be made vacant. For example, if the 6810 is housed in slots 5, 6, 7, and 8, slot 9 must be vacant.

To install a 6310 Memory Module, unplug the 6810–5 terminator board from the 6810 front panel to expose connectors as shown in Figure 9.



Interlocking Memory Module Connectors
Figure 9

Slide the 6310 into the next slot, interlocking its corresponding connectors with those exposed on the 6810 front panel. Then, tighten (clockwise) the thumbscrew located on the 6310's lower front panel to draw the module interface connectors into the backplane. Additional 6310 modules interlock with one another in like manner.

Note: The rightmost 6310 must have a 6810–5 terminator installed to ensure proper operation.

Installing the 8901A or 6010 GPIB to CAMAC Interface Modules

The rightmost slot in any CAMAC Standard mainframe is reserved for the CAMAC interface control module.

With the power off, insert the 8901A in the two rightmost slots in the CAMAC mainframe. Tighten (clockwise) the thumbscrew on the 8901A's lower front panel. Tightening this screw draws the module's interface connectors into the mainframe's backplane. Conversely, loosening the thumbscrew retracts the module's interface connectors from the backplane.

The 6010 module occupies the three rightmost slots in the CAMAC mainframe and is fastened by tightening the thumbscrew as described above.

Interconnect the GPIB cable to the appropriate connectors on the computer and the front panel of either the 8901A or 6010 interface module.

MAKING SIGNAL CONNECTIONS TO THE 6810

You can connect up to four signals to the 6810. These signals can be differential inputs, single-ended inputs, or grounded. Each input mode is set up using programmable relays which are opened and closed via CAMAC bus commands. These commands independently configure the input modes of each channel. Thus, each channel can be configured differently. For example, on a single 6810 module, channel one could be in differential input mode, channel two in single-ended inverting mode, channel three in single-ended non-inverting mode, and channel four in differential mode.

WARNING: Since the 6810 chassis is grounded for safety, connecting the input probe shield clip or the shielding on a coaxial input cable to non-isolated high voltage sources (e.g. power line) will cause irreparable damage to the 6810 circuit boards. Connecting to non-isolated voltages greater than 70 V might cause arcing and damage to the 6810 and the probe. Connecting to a low non-isolated voltage will induce currents in the shield which might couple into the signal path to generate an erroneous voltage and degrade the measurement accuracy.

CONNECTING FOR LOW NOISE MEASUREMENTS

The following connections will optimize 6810 noise rejection for typical DC to 2.5 MHz applications. Listed from most to least effective, each details wiring methodology and recommended use.

NOTE: These recommendations assume the noise sources to be both wideband radiated (EMI) and conducted. Therefore, they do not apply to low frequency range instruments, such as voltmeters.

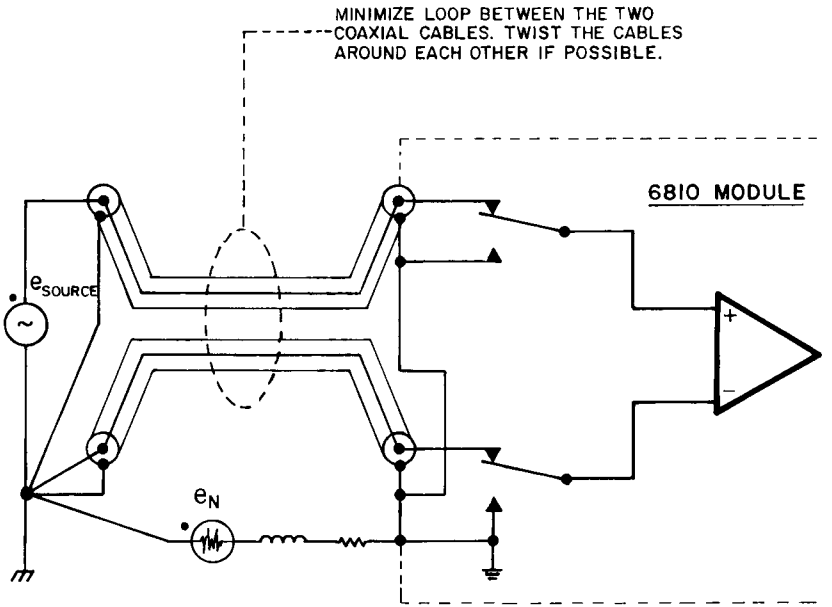
DIFFERENTIAL INPUT MODE

Use the differential input mode for waveform measurements made relative to a non-ground level or to reduce noise in ground referenced measurements. For example, differential mode measures across a transducer but rejects the transducer bias voltage which is common to both inputs. It also rejects magnetic field induced, common mode, line frequency noise.

The differential input mode uses both the non-inverting (+) and inverting (–) BNC inputs simultaneously. Identical signal levels on both inputs cancel and the 6810 digitizes a ground output level. In this manner, common mode signals get rejected.

Only differences in voltage show up as digitized positive or negative signals. When the non-inverting input contains a more positive signal than the inverting input, the digitized signal is positive. When the inverting input contains a more positive signal than the non-inverting input, the digitized signal is negative.

Generally, differential input mode provides the best noise rejection for either grounded or floating measurements:



- SHIELDS GROUNDED AT SAME SOURCE GROUND POINT.
- HIGH FREQUENCY NOISE MINIMIZED BY CABLES.
- MEDIUM FREQUENCY NOISE DEPENDS ON 6810 COMMON MODE REJECTION AND GROUND LOOP INDUCTANCE DIFFERENCES.
- LOW FREQUENCY NOISE DEPENDS ON 6810 COMMON MODE REJECTION AND CABLE SHIELD RESISTANCE DIFFERENCES.

Differential Connection

Figure 10

Since coaxial shields filter high frequency noise, the 6810 uses coaxial cables for the two differential inputs. Both of the cable shields should be connected to earth ground at the measurement point to prevent noise pickup at the probe.

Since the 6810 chassis is grounded for safety, this probe ground connection will cause a ground loop. However, coaxial shield inductance is high and usually filters high frequency ground loop and electrostatic noise. This "filter" cutoff frequency is roughly 500 Hz. The differential amplifier in the 6810 rejects lower frequency common mode noise. The input coaxial cables should

be the same length to prevent common mode signals from becoming differential errors.

Voltage Range Selection

To select the correct range for differential input mode operation:

1. Estimate or measure the maximum common mode voltage (Vcm). If Vcm > 5 V peak, then use the 10 V, 25 V, 50 V, or 100 V range. If Vcm > 125 V peak, then attenuate both input identically. Common mode voltages exceeding 5V on the 400 mV, 1 V, 2 V, or 4 V ranges, or exceeding 125 V on the upper four ranges will cause gradually increasing harmonic distortion.
2. Estimate or measure the maximum differential mode voltage (Vdm). Choose the next higher voltage range to prevent waveform clipping and gross harmonic distortion.

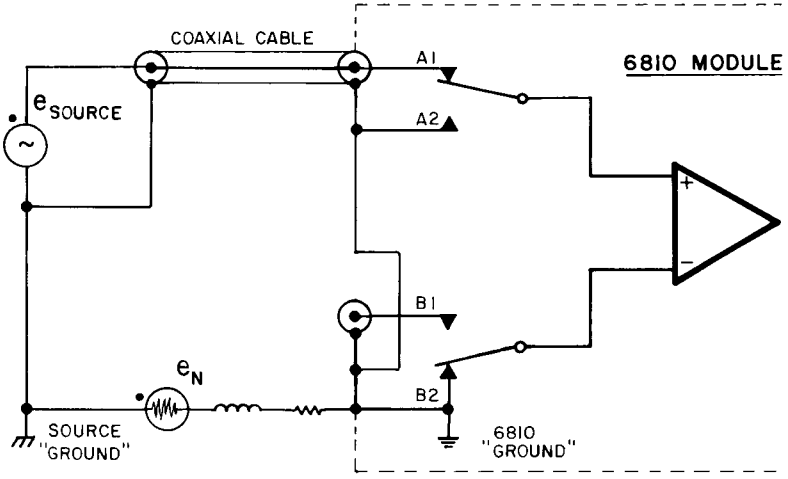
$$\vec{Vcm} = \frac{\vec{V(+)} + \vec{V(-)}}{2}; \qquad \vec{Vdm} = \vec{V(+)} - \vec{V(-)}$$

NOTE: The 6810 input offset adjustment allows use of the full range no matter whether your signal is symmetrically bipolar (equally positive going and negative going), unipolar positive, or unipolar negative. The 6810 settings default to zero offset, which means optimized for bipolar inputs. If your signal is unipolar or non-symmetrical, use the offset to prevent clipping of the input signal.

SINGLE-ENDED MODES

Use the single-ended mode for simplified ground-referenced measurements. It is easier to connect one probe than the two required for differential measurement.

The 6810 front panel holds two single-ended input BNC connectors, an inverting and a non-inverting, for each channel. The 6810 will digitize a unipolar positive input connected through the non-inverting (+) BNC connector as a unipolar positive signal. It will digitize the same unipolar positive input as a unipolar negative signal if connected through the inverting (-) input BNC.



- SHIELD GROUNDED AT SOURCE GROUND.
- HIGH-FREQUENCY NOISE MINIMIZED BY CABLE.
- LOW-FREQUENCY NOISE DEPENDS ON CABLE SHIELD RESISTANCE.
- MEDIUM FREQUENCY NOISE DEPENDS ON INDUCTANCE OF GROUND LOOP FORMED BY CABLE SHIELD AND GROUND CONNECTION CONTAINING e_N.

Single Ended Connection

Figure 11

For single-ended connections (*i.e.*, referenced to chassis/earth ground), attach a standard oscilloscope probe or coaxial cable to either the non-inverting (+) or the inverting (-) BNC. The impedance (capacitive and resistive) should match the 6810 input impedance (see specifications) as closely as possible. A good match will minimize overshoot and undershoot when digitizing pulse edges.

NOTE: Be sure the front panel input BNC connection matches the programmed mode (inverting or non-inverting, single-ended). The selected mode shunts the unused input to chassis ground through a 1 MΩ resistor. If the probe/cable connection is accidentally made to the shunted BNC, then the digitizer will not internally trigger on this channel. Manual triggers will only digitize a grounded signal.

Connecting the probe tip shield to earth ground near the measurement provides the best noise rejection for single-ended

measurements. Unfortunately, wideband conducted noise can always combine with the signal when using the single-ended mode. Single-ended mode can be more accurate than differential mode measurements if the loop formed by the two differential probe cables cannot be minimized or if the two cables vary much in length.

If the unit under test (UUT) contains an earth ground reference point, then connect the 6810 probe shield there. If the UUT is isolated (floats) from ground by an isolated power supply, then the 6810 probe shield connection can establish a UUT ground reference point. While connected, the UUT will not float, it will be ground referenced, and the 6810 measurement will be relative to the connection point.

Voltage Range Selection

To select the correct range for single-ended input mode operation:

1. Estimate the signal amplitude level.
2. Choose the range with the next higher voltage value.

For example, if you are measuring a +7 V CMOS logic signal, then choose the 10 V range.

NOTE: The 6810 input offset adjustment allows use of the full range no matter whether your signal is symmetrically bipolar (equally positive going and negative going), unipolar positive, or unipolar negative. The 6810 settings default to zero offset, which means optimized for bipolar inputs. If your signal is unipolar or non-symmetrical, use the offset to prevent clipping of the input signal.

GROUNDED INPUT MODE

Use the grounded input mode in conjunction with a manual (software) trigger to determine the ground level position on a display monitor when using WAVEFORM-CATALYST™ or some other oscilloscope emulation software package. In most cases, the noisiest measurement will be single-ended with the probe shield unattached. Both wideband conducted and high frequency radiated noise can erroneously combine with the signal.

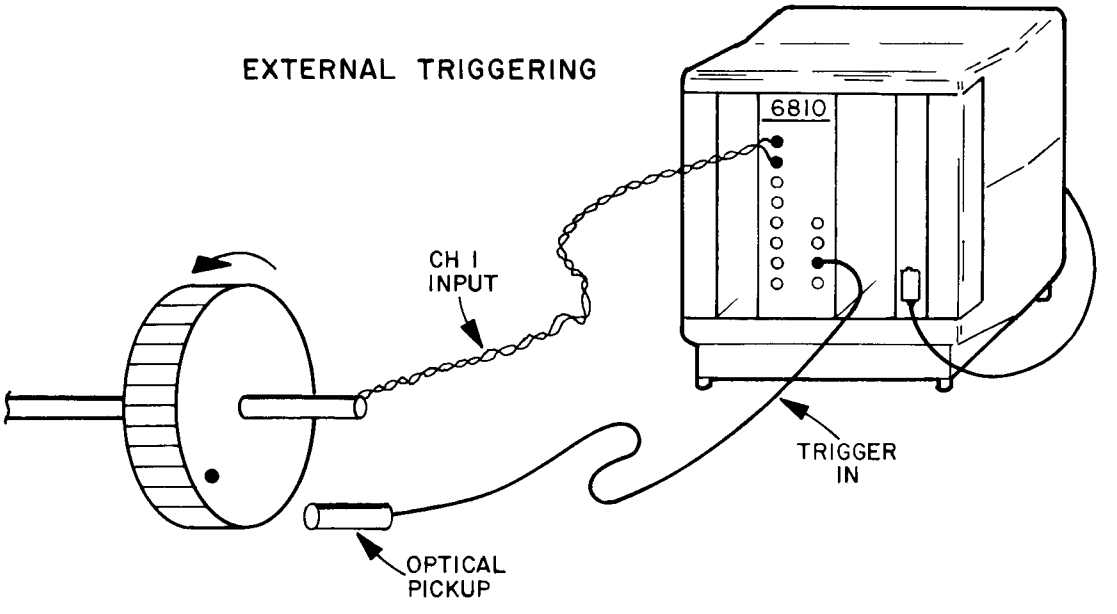
In the grounded input mode, relays short both the non-inverting (+) and the inverting (-) inputs to chassis (ground) through 1 MΩ resistors.

MAKING TRIGGER INPUT CONNECTIONS TO THE 6810

If the signal on Channel 1 or Channel 2 provides an adequate trigger input, then use the internal trigger and select one of the inputs for trigger pickoff. Internal triggering requires no external trigger connection. If you need more than four channels of simultaneous waveform acquisition triggered by a single event or you need to trigger on an external event other than the signal itself, then use the external trigger connection.

Waveform averaging, for example, usually requires a trigger source other than the signal itself. If the signal itself is noisy, then it will not provide a stable trigger point. Averaging under these conditions would severely reduce the recorded signal bandwidth.

Another example, analyzing vibration on rotating machinery, requires that the trigger point be synchronized with the shaft position. Synchronous data enables accurate fault diagnosis.

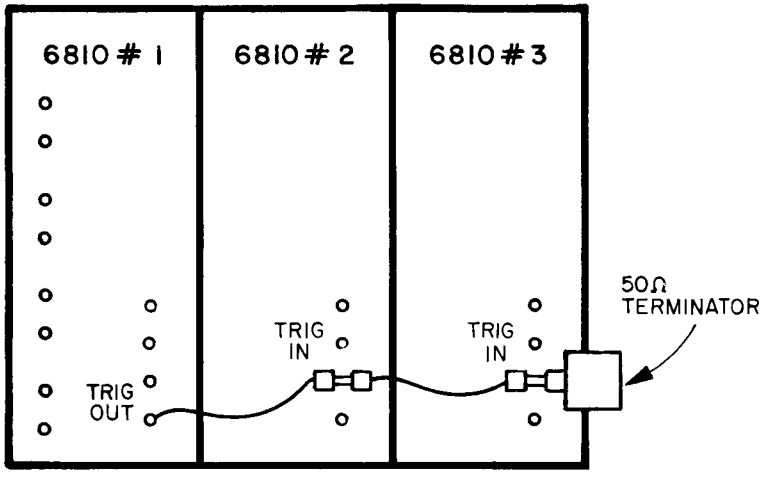


External trigger setup diagram – rotating mechanical application

Figure 12

Multichannel applications demanding synchronous sampling of more than four channels necessitate triggering more than one 6810 digitizer module from the same signal. External triggering provides the key: one module acts as the master and the rest as slave modules. The trigger signal, either internal or external, gets generated in the master 6810. A conditioned trigger output from the master (Trigger Out BNC) Tee's to each of the slaves. The cable should be terminated by its characteristic impedance at the last module.

The "Trigger Out" source can drive a 50 Ω load; the "Trigger In" input impedance is 1 MΩ. Therefore, the "Trigger Out" can drive numerous parallel slave modules.



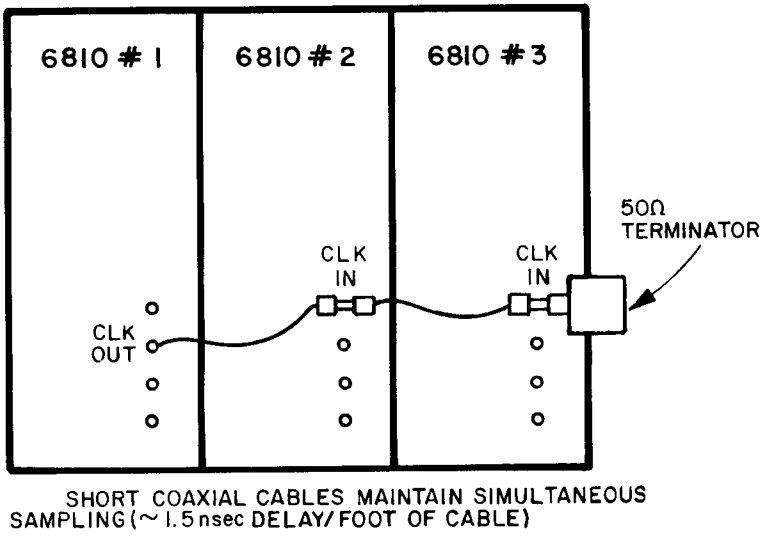
12 Channel Simultaneous Acquisition Setup

Figure 13

MAKING CLOCK INPUT CONNECTIONS TO THE 6810

The external "Clock In" connector lets the 6810 sample synchronously with a TTL-level oscillation on the Unit Under Test. It also provides the means for multichannel synchronizing sampling using several 6810 modules.

To synchronize several 6810 clocks, one 6810 acts as a clock master. The buffered clock output from this master ("Clock Out") is Tee'd to each of the slaves. The "Clock Out" source can drive a 50 Ω load; the "Clock In" impedance is 100k Ω. Therefore, the "Clock Out" can drive numerous parallel slave modules. The cable should be terminated in its characteristic impedance at the last module.



12 Channel Synchronous Sampling Setup
Figure 14

If asynchronous sampling between several 6810 modules or between a 6810 module and the Unit Under Test is acceptable, then the 6810 internal clock modes will serve your needs. External clock input connections will not be necessary.

2 OPERATION

INTRODUCTION

This chapter provides instructions for programming the 6810 module. The first two sections describe WAVEFORM-CATALYST operation. "Getting Started: PC Control Using WAVEFORM-CATALYST™ helps you get started measuring waveforms quickly. *(NOTE: hereafter, text references to CATALYST are synonymous with WAVEFORM-CATALYST.)* Following proper component configuration and hardware/software setup, a real time example is presented which demonstrates how to display a simple waveform. "Operating the 6810 with WAVEFORM-CATALYST" presents detailed instructions for using CATALYST software.

The next sections detail CAMAC Operation. A brief introduction to CAMAC protocol precedes "6810 CAMAC Operation". The "6810 CAMAC COMMAND_COMMAND SUMMARY" and "6810 COMMAND DETAILS". An elaboration on "VERIFY SETUP" command, F(18)A(6), and a special section on "TRIGGER and DUAL SPEED CLOCK TIME" are also included.

GETTING STARTED

PC Control Using WAVEFORM CATALYST Software

This CATALYST example helps you get started displaying waveforms on your PC quickly. It requires that you complete three tasks:

Configure System Components,
Install CATALYST,
and Display a digitized sine wave.

List of Equipment

Prior to setup, you'll need the following equipment:

IBM PC or compatible configured as follows:
2 disk drives
512k RAM memory
IBM color/graphics board or IBM Enhanced Graphics Adapter
Intel Math coprocessor
PC-DOS 2.0 of greater
Video Monitor
National Instruments GPIB-PC Interface (Model PC2 or PC2A)
WAVEFORM-CATALYST program diskettes*

Model 8013A, Model 1434A, or Model 8025 CAMAC Instrument Mainframe or equivalent

Model 8901A or 6010 GPIB to CAMAC Controller (Either controller module can be used. Instructions to set the GPIB

Address Switch for each appear in "Configure System Components.")

6810 Waveform Recorder Module
IEEE-488 GPIB Cable
Function Generator (sine wave output)
BNC Cable

**See WAVEFORM-CATALYST User's Manual (Version 2.6) for a list of compatible multifunction boards, graphics boards, computers, and printers.*

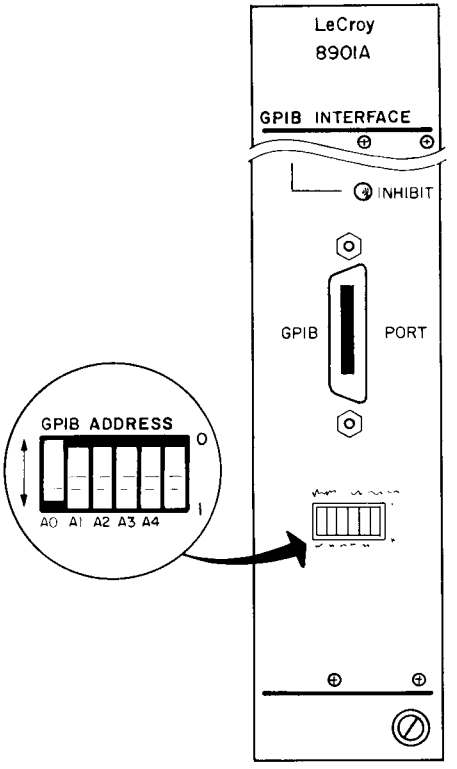
Configure System Components

1. If not already resident, install National Instruments GPIB card in an empty computer slot following the National Instruments Installation manual.
2. If using a printer, connect it to the main parallel interface on the personal computer. Be sure the printer configuration switch matches the WAVEFORM-CATALYST configuration (selected from the SETUPCAT installation program).
3. If using any other peripherals (such as a hard disk), connect them per the manufacturer's directions.

NOTE: Before proceeding, execute the diagnostics provided with the computer and National Instruments to ensure correct assembly and working order.

4. Complete this step and skip step 5 if using an 8901A GPIB to CAMAC Interface. If using a 6010 GPIB to CAMAC Interface, skip to step 5.

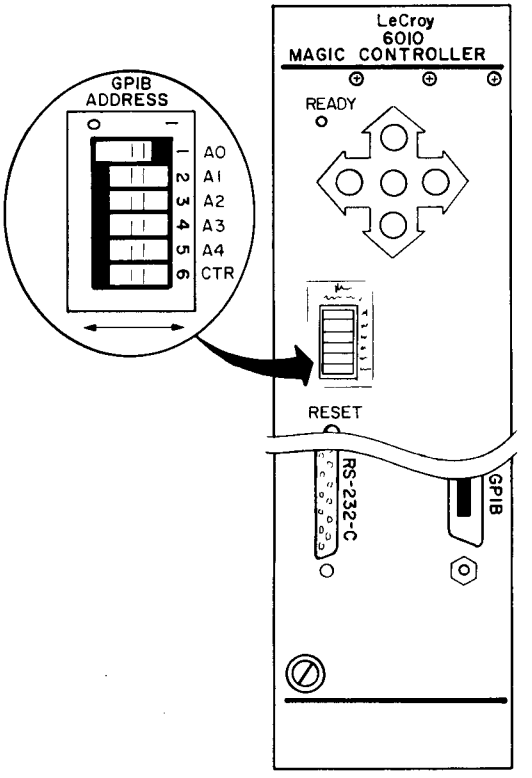
   Each device connected to the GPIB must have a unique address which the system controller uses to communicate with it. (WAVEFORM-CATALYST addresses must be from 1 to 15). The Model 8901A's address is set by DIP switches located under the GPIB connector on the front panel. These switches are labelled A0, A1, A2, A3, A4 (representing values of 1, 2, 4, 8, and 16 respectively). Valid GPIB addresses are 1 to 31. The factory preset GPIB address switch setting of 1 is used in our example. Make sure your 8901A GPIB address matches the one in the figure:



8901A GPIB Address Switch Setting of 1

Figure 15

5. Each device connected to the GPIB must have a unique address which the system controller uses to communicate with it. (WAVEFORM-CATALYST addresses must be from 1 to 15). The Model 6010's address is set by DIP switches located above the BNC connectors on the front panel. The switches are labelled A0, A1, A2, A3, A4, CTR (representing values of 1, 2, 4, 8, and 16 respectively). Valid GPIB addresses are 1 to 31. The factory preset GPIB address switch setting of 1 is used in our example. Make sure your 6010 GPIB address matches the one in the figure:



6010 GPIB Address Switch Setting of 1

Figure 16

6. Install the 6810 module in slots 7 through 10 of the CAMAC instrument mainframe. Review Chapter 1 module installation information.

WARNING: Do not attempt to install a module while the mainframe is powered on. Doing so will cause damage to the module's internal circuitry.

The 6810's front panel arrow will point to slot number 9, the 6810's CAMAC N slot number. During bus operation, the GPIB to CAMAC interface addresses this CAMAC slot to communicate with the 6810.

7. WITH THE POWER OFF install either the 8901A or 6010 GPIB to CAMAC Interface in the mainframes's rightmost

slots. The 8901A requires the crate's two rightmost slots, the 6010 the three rightmost slots. Review Chapter 1 module installation information.

8. Attach the GPIB cable to the ports on the GPIB to CAMAC Interface module and the computer.
9. POWER ON the CAMAC mainframe.

Install CATALYST

Following are instructions for setting up WAVEFORM–CATALYST to operate from your hard disk. If your system uses two floppy diskette drives, skip this section and complete the steps to "Setup CATALYST operation from floppy diskettes." Otherwise, complete this section and skip to "Display a Sine Wave."

Place CATALYST on your hard disk

NOTE: If the disk is not formatted or the operating system is not on it, refer to your DOS manual for appropriate instructions.

1. Power on the computer.
2. When DOS prompt C> appears, place the CATALYST Boot Disk in Drive A, and type A: Press **[ENTER]**. The DOS prompt should be A>.
3. Type **SETUPCAT C:,g**

   where g = 2 for National Instrument's GPIB 2 card, 2A for NI's GPIB 2A or IBM's GPIB card. Press **[ENTER]**.
4. Follow directions printed on the screen.
5. Once setup is complete, remove this disk and "boot" the computer (simultaneously press **[CTRL]**, **[ALT]**, and **[DEL]** keys) from the hard disk.

Setup CATALYST Operation From Floppy Diskettes

Following are instructions for setting up CATALYST to operate from floppy diskettes. This method is recommended only if you do not have a hard disk:

1. Power–on the computer with a DOS disk in drive A.
2. Enter date and time at prompt. Press **[ENTER]**.
3. When the DOS prompt A> appears, copy the CATALYST boot and Program diskettes. To do so:
   a. Type **DISKCOPY A: B:** and press **[ENTER]**.
   b. Remove DOS disk and insert CATALYST Boot Disk in Drive A.
   c. Insert formatted blank disk in Drive B and press **ANY KEY**.

d. When copy is complete, answer **Y** to the prompt "copy another?"

e. Remove both disks and label new disk CATALYST Boot Disk.

f. Insert CATALYST Program Disk in Drive A, insert blank disk in drive B and press **ANY KEY**.

g. When copy is complete, answer **N** to "more copies?", remove both disks and label new disk CATALYST Program Disk.

4. Place new copy of CATALYST Boot Disk in Drive A.

5. Type **SETUPCAT B:,g**

   where g = 2 for National Instruments GPIB 2 card, 2A for NI's GPIB 2A or IBM's GPIB card. Press **[ENTER]**.

6. Follow directions printed on the screen.

7. Once setup is complete, "boot" the computer (press the **[CTRL]**, **[ALT]**, and **[DEL]** key simultaneously) with the CATALYST Boot Disk in Drive A.

Display a Sine Wave

Some parameter values used in our example are preconfigured factory settings. Others require modification. (If you begin this segment of the example from the C:> prompt, invoke WAVEFORM-CATALYST by typing **CAT** and pressing **[ENTER]**.)

1. Press **L** to list modules.

2. When the list of modules appears under the Waveform Display Screen, press the number that corresponds to the 6810 module.

3. Using the arrow keys to highlight parameters, configure the 6810 Setup menu as follows:

NOTE: To change a setting, press E(dit), type in the desired value, and press [ENTER].

NAME: Module 1 = A1 to A4, Module 2 = B1 to B4 is the default factory setting; it is used in this example.

NOTE: This examples requires only one 6810 module; therefore, ignore B1 through B4 settings.

ACQUIRE: Set to **YES** under A1 only. To change a setting, press E(dit), type in the desired value, and press **[ENTER]**.

STORE: Set to **NO** or the system will automatically store waveforms to your PC disk drive after each acquisition.

PROCESS: Set to **NO**. This parameter is used for advanced user written FORTRAN routines to post process the waveform data.

GPIB ADDR: The GPIB address and Slot number must be assigned for all channels of a given module regardless of whether those channels are set to acquire or not. In this example set A1 through A4 channels to GPIB address **1**.

SLOT: As indicated above, our example requires that the 6810 module be placed in slots 7, 8, 9, and 10. Set A1 through A4 to **7** through **10** respectively.

CHANNEL NUMBER: Do not change. The Channel number must always be **1** through **4.**

FULL SCALE VOLTAGE RANGE: Set to **10 V** for Channel 1.

OFFSET: Set Channel 1 Offset to **0**.

COUPLING: Set Channel 1 Coupling to **+AC**.

MEMORY SIZE: Set Memory Size to **512k**.

SEGMENT SIZE: Set Segment Size to **4k** samples.

PERIOD: Set Channel 1 Period to **.2 μsec** equivalent to 5 megasamples/sec (period = 1/sample rate)

SET TRIGGER: Set Channel 1 Trigger to **YES**.

SET CLKMODE: Set Channel 1 Clockmode to **YES**. You are now finished with the primary menu selections. Your monitor screen should match the following:

SETUP MODULE 6810

		A	B	C	D	E	F	G	H	I	J
1	NAME	A1	A2	A3	A4			B1	B2	B3	B4
2	ACQUIRE	YES	NO	NO	NO			NO	NO	NO	NO
3	STORE	NO	NO	NO	NO			NO	NO	NO	NO
4	PROCESS	NO	NO	NO	NO			NO	NO	NO	NO
5	GPIB ADDR	1	1	1	1						
6	SLOT	7	8	9	10						
7	CHANNEL #	1	2	3	4			1			
8	FULL SCALE V	10	2	2	2			2			
9	OFFSET VOLTS	0	0	0	0			0			
10	COUPLING	+ AC	+DC	+DC	+DC			+ DC	+ DC	+ DC	+ DC
11	MEMORY SIZE	512K						512K			
12	SEGMENT SIZE	4K						128K			
13	PERIOD	.2us						.2us			
14	SET TRIGGER	YES						NO			
15	SET CLKMODE	YES						NO			

All modules Enter Goto Help Next Previous Read Write
press space to return

Example CATALYST Setup Menu Screen
Figure 17

4. Next press **[SPACE BAR]**. You will be prompted to enter trigger and clock mode settings. The setup menu lines for trigger and clock mode have two parts: the options are displayed in parentheses, and the present setting is displayed on the far right. For example, in the following menu line, pressing **2** and **[ENTER]** will set the trigger coupling to AC:

   coupling (0=DC, 1=HFR, 2=AC, 3=LFR) presently = AC ?

NOTE: Pressing [ENTER] without making a selection leaves the parameter unchanged.

The menu lines will appear, one at a time, on the lower screen. As each line appears, enter the number or value which matches the selections used in our example:

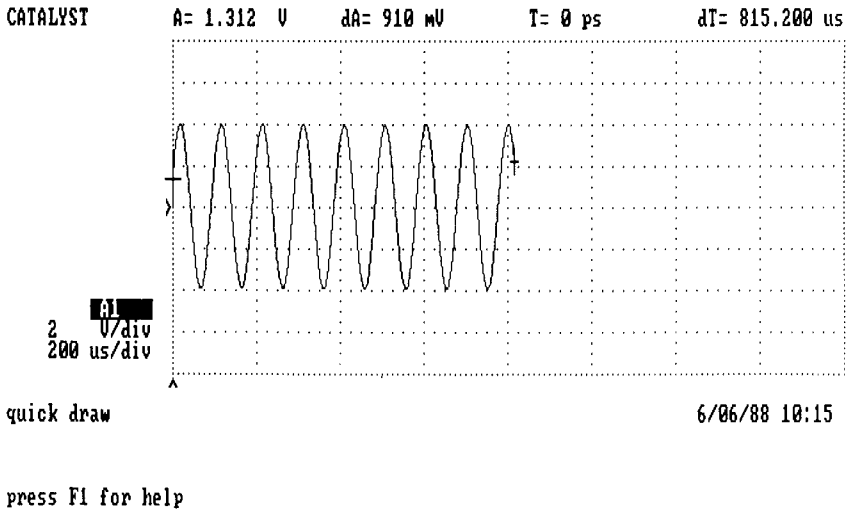
OPTIONS	SELECTIONS used in example
coupling	AC
slope	+
source	ch1
upper trigger level	1
delay	0
Trigger holdoff enable	Y
dual clock mode	0
Number of segments	1
Time stamp res	10 μsec

The actual menu lines are depicted below:

coupling (0=DC, 1=HFR, 2=AC, 3=LFR) presently = AC ?
slope (0=+, 1=–, 2=window, 3=+h, 4=–h) presently = + ?
source (0=ext, 1=ch1, 2=ch2, 3=manual) presently = ch1 ?
upper trigger level (volts) presently = 1 ?
delay (in eights: –8 to 247) presently = 0 ?
Trigger holdoff enable (Y/N) presently = Y ?
dual clock mode (0–3) presently = 0 ?
Number of segments presently = 1 ?
Time stamp res (0=1 μs, 1=10 μs...4=10 μs) presently = 10 μs ?

After the final menu line is displayed and the Time stamp resolution is selected, press **[ENTER]** to reinvoke the waveform display screen.

5. Turn on the function generator and set a sine wave output of approximately 10 kHz, 8 V peak-to-peak.
6. Connect the BNC cable from the function generator to +input Channel 1 on the 6810's front panel.
7. Define trace 1 on the display by pressing **1**. Type **A1** and press **[ENTER]**.
8. Press **S** (single trigger) to arm the 6810 for a single trigger. The 6810 will acquire and display the captured waveform, a sine wave. It remains on the screen, as it has been digitized.



Captured Sine Wave

Figure 18

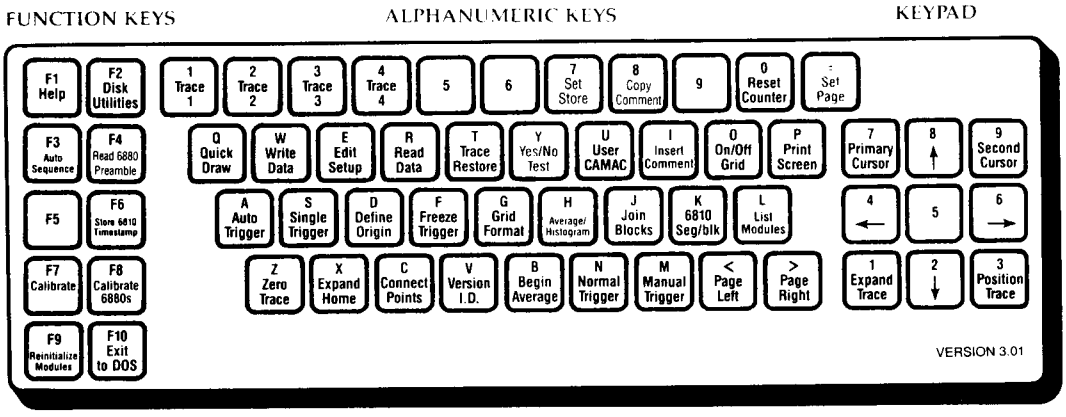
9. To permanently store the waveform to disk, press **W**. At prompt "enter name of file:" type in your selected file name and press **[ENTER]**. At prompt "enter module name:" type **A1** and press **[ENTER]**. The data is now stored on disk.

10. To recall the data, press **R**.
    At prompt "enter trace number (1-4):" press **1**.
    At prompt "enter name of file:" type in the filename you selected in step 9 and press **[ENTER]**.
    At prompt "enter label for trace:" type **A1** and press **[ENTER]**. The message "reading from disk" will appear on the screen, as the system is recalling data from disk.

11. Press **[F10]** key to exit CATALYST and return to the DOS prompt. If after exiting you wish to re-enter CATALYST and recall the digitized waveform, type **CAT** and press **[ENTER]**. When the WAVEFORM-CATALYST logo appears, repeat step 10.

OPERATING THE 6810 WITH WAVEFORM-CATALYST

The 6810 Waveform Recorder can be operated using an IBM PC XT, AT or strict compatible running WAVEFORM-CATALYST software (Versions 2.6 or later) connected to the Model 8901A or 6010 GPIB controller. WAVEFORM-CATALYST provides control over 6810s or other modular instruments in up to 15 separate instrument mainframes, controlling up to 300 input channels when using 25-slot rackmount instrument mainframes. WAVEFORM-CATALYST provides easy-to-learn single-keystroke commands which effectively turn a waveform recorder(s) and IBM PC into a digitizing oscilloscope. The WAVEFORM-CATALYST "Quick Reference Guide" shown in Figure 19 depicts the single keystroke commands:



WAVEFORM-CATALYST Quick Reference Guide

Figure 19

WAVEFORM-CATALYST SETUP MENU

This section explains how to establish 6810 measurement parameters using the WAVEFORM-CATALYST Setup Menu. To access the 6810 Setup menu, press the L(ist Modules) key and the number which corresponds to the 6810. The screen (Figure

2) is the default factory shipped menu which is stored in the file named SD6810.CAT. To modify the menu:

1. Adjust the menu parameters to fit your application.
2. Press **W** key to write the file to disk.
3. At prompt "enter filename:", name the file and press **[ENTER]** (or Return) key to change the default.

To create alternate 6810 setup menus, perform the above steps, changing the filename. To replace the default with an alternate setup file:

1. Press **R** key to read the alternate file from disk.
2. At prompt "enter filename:" type the alternate setup file-name and press **[ENTER]**.

NOTE: WAVEFORM-CATALYST's 6810 help screen lists the important points for WAVEFORM-CATALYST to control the 6810. To access the help screen(s) from the 6810 setup menu, press H.

SETUP MODULE 6810

		A	B	C	D	E	F	G	H	I	J
1	NAME	A1	A2	A3	A4			B1	B2	B3	B4
2	ACQUIRE	YES	NO	NO	NO			NO	NO	NO	NO
3	STORE	NO	NO	NO	NO			NO	NO	NO	NO
4	PROCESS	NO	NO	NO	NO			NO	NO	NO	NO
5	GPIB ADDR	1	1	1	1						
6	SLOT	7	8	9	10						
7	CHANNEL #	1	2	3	4			1			
8	FULL SCALE V	10	2	2	2			2			
9	OFFSET VOLTS	0	0	0	0			0			
10	COUPLING	+ AC	+DC	+DC	+DC			+ DC	+ DC	+ DC	+ DC
11	MEMORY SIZE	512K						512K			
12	SEGMENT SIZE	4K						128K			
13	PERIOD	.2us						.2us			
14	SET TRIGGER	YES						NO			
15	SET CLKMODE	YES						NO			

All modules Enter Goto Help Next Previous Read Write
press space to return

Example CATALYST Setup Menu Screen

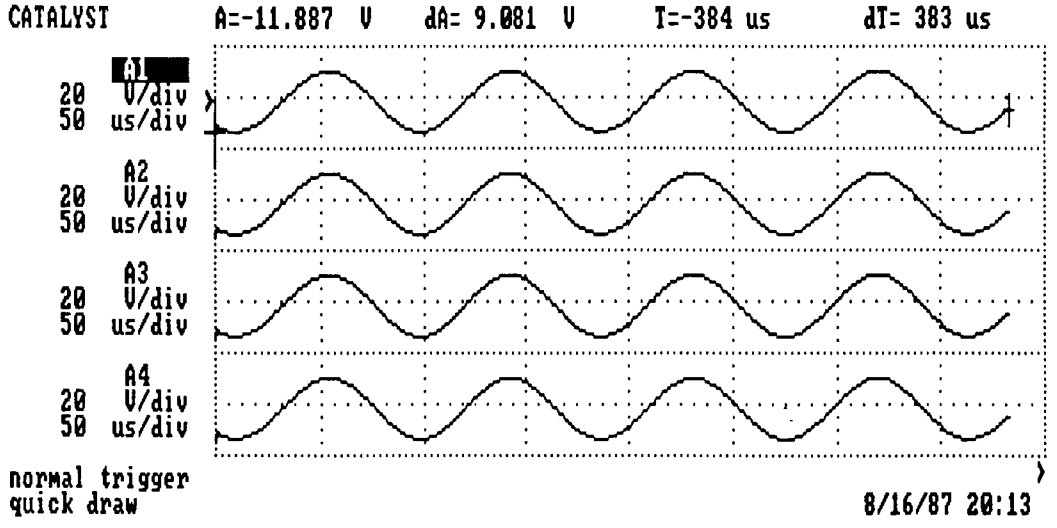
Figure 20

The above menu lists the 15 setup parameter functions; each is described in detail below. Also provided are the default setting, range of settings, and the parameter's direct result on the 6810's operation.

NAME

Each 6810 measurement channel is named separately as shown in the first line of the 6810 setup menu. Default names are A1...A4 and B1...B4. Input channels' names cannot exceed four characters. The name specified for the input channel precedes each displayed waveform. To assign the first 6810 input channel to Trace 1 using the default name of A1:

1. Type **1**
2. Type **A1**
3. Press **[ENTER]**



6810 Channels Displayed Using Default Names
Figure 21

ACQUIRE

Each 6810 input channel is enabled by setting Acquire to **YES** for that channel. Press **N**(ext) or **P**(revious) key to toggle between NO (the default setting) and YES.The 6810 operates in the 1-Channel, 2-Channel, and 4-Channel modes:

To enable the 1-Channel mode, set ACQUIRE to YES for Channel 1 only.

To enable the 2-Channel mode, set ACQUIRE to YES for Channel 1 and 2.

To enable the 4-Channel mode, set ACQUIRE to YES for all input channels.

NOTE: Setting Acquire "YES" for Channels 1, 2, and 3 only will not enter the 6810 into 3-Channel mode. 3-Channel mode is not a supported 6810 feature; invoking 3-Channel defaults the instrument to 2-Channel operation.

STORE

Setting Store "YES" copies the waveform for the applicable input channel to disk after each waveform update (when the waveform data is transferred to the computer's \DATA subdirectory using incremental numeric filename extensions). For example, if Channel 1 (specified as A1) is triggered 3 times with Store set to YES, the FILES A1.1, A1.2 and A1.3 are stored in the DATA subdirectory.

NOTE: to reset file extension numbers to 1, use the 0 (Reset Counter) key.

PROCESS

The Process feature helps experienced programmers write code to process the displayed data. When Process is enabled (=YES), a routine named "USER1" processes data each time it is read in from the specified input channel. Therefore, to use Process parameter, the processing routine USER1 must be written. The calling sequence for USER1 is:

CALL USER1 (INBUF, DHDR, BLOCK)
Where INBUF is an 8 Kbyte data buffer, DHDR is a display parameter array,
BLOCK is the current block number.

Once the processing routine has been written and compiled, the object file must be copied to the object code link disk and the program should be relinked.

GPIB ADDRESS

To determine the 6810's GPIB address, check the GPIB address switch on your instrument mainframe controller/interface module (models 8901A and 6010). Valid inputs for the GPIB address range from 1 to 15. To increment the GPIB address by 1, press the N(ext) key. Decrement the GPIB address by 1 by pressing the P(revious) key.

NOTE: All four 6810 channels must be specified with same GPIB address.

SLOT

For WAVEFORM-CATALYST to correctly interpret the "Look At Me" (LAM) signal from the 6810 Waveform Recorder module, the slot indicated by the N on the 6810 front panel must be assigned to channel 3. Channel 1 is represented by N-2, channel 2 by N-1 and channel 4 by N+1. For example, if the 6810 N marker is in slot 8, the 6810 occupies slots 6, 7, 8 and 9 and should be assigned as the respective slots for channels 1 through 4.

CHANNEL #

The channel default settings from left to right are 1 2 3 4.

NOTE: Never change the order of these channels.

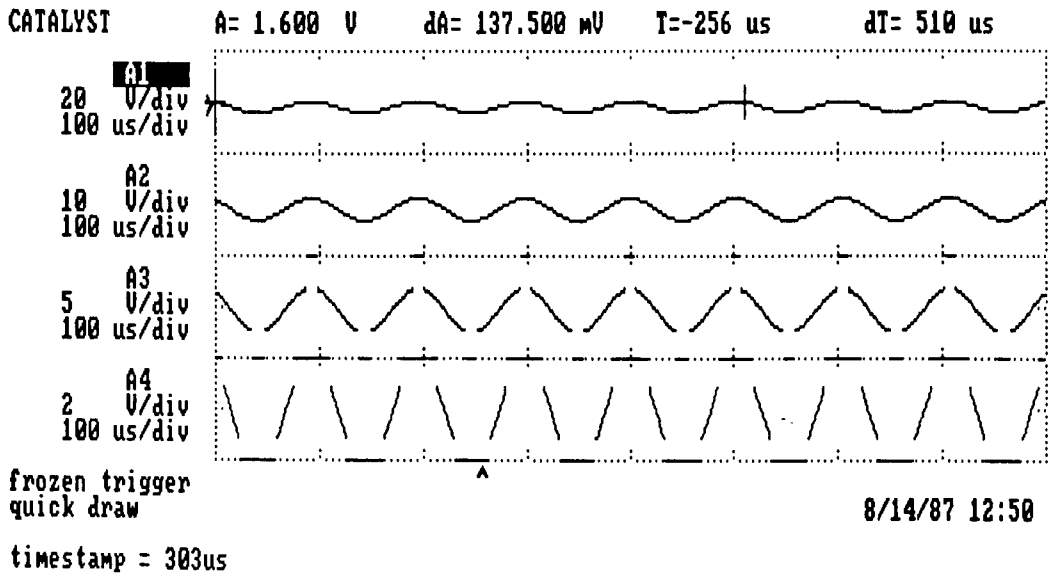
FULL SCALE V

Menu option 8 lets you modify the input full scale voltage range on a per channel basis to allow different input ranges for each active channel. A 2 V full scale input range for a channel allows a maximum of ±1 V signal with no offset. Valid parameter input values are:

400 mV; 1 V; 2 V; 4 V; 10 V; 25 V; 50 V; 100 V

To increment/decrement through the valid voltage ranges, press the N(ext)/P(revious) key.

When an input voltage range is set too high, the magnitude of a measured signal may be smaller than necessary for viewing minute changes in the waveform's magnitude. To expand the signal vertically, press 1 (numeric key pad) to invoke WAVEFORM-CATALYST into the Expand Trace mode. Next press the up arrow [↑] to expand the trace. The trace can also be expanded by retaking the measurement using an input voltage range which better approximates the measured waveform's peak-to-peak value. Retaking the measurement is always the better alternative since expanding the display does not improve the vertical resolution (ability to see minute changes in the waveform's magnitude) like lowering the input voltage range. Figure 22 shows the same waveform measured using four different input voltage ranges. The 6810 provides 12-bit vertical resolution. Take advantage of this resolution by using the input voltage range which best approximates the waveform's magnitude.



4 Input Channels with 4 Different Input Ranges

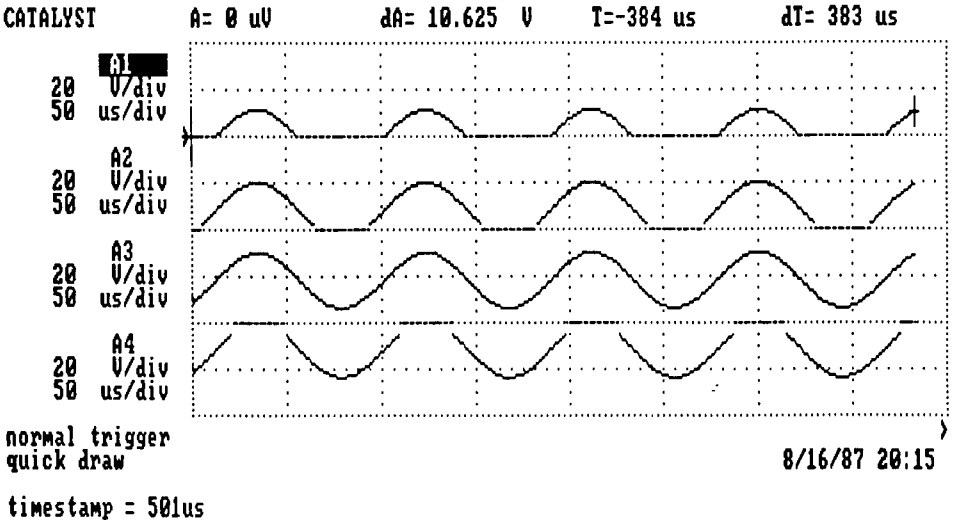
Figure 22

OFFSET

When the input signal is bipolar, *e.g.*, ±2 V, the offset should be set for 0 V. If the input is unipolar positive, unipolar negative, or offset bipolar, the offset should be set for a value which, when added to the input signal, makes the resultant bipolar. Following are some examples:

Full Scale V Range	Input Signal	Offset	Resultant
4 V	−2 V to +2 V	0 V	−2 V to +2 V
10 V	0 V to +10 V	−5 V	−5 V to +5 V
1 V	−1 V to 0 V	+.5 V	−.5 V to +.5 V
50 V	−10 V to +40 V	−15 V	−25 V to +25 V

NOTE: If offset is larger than Full Scale Voltage range, the offset defaults to 0V.



Same Waveform Measured Using Four Different Offsets
Figure 23

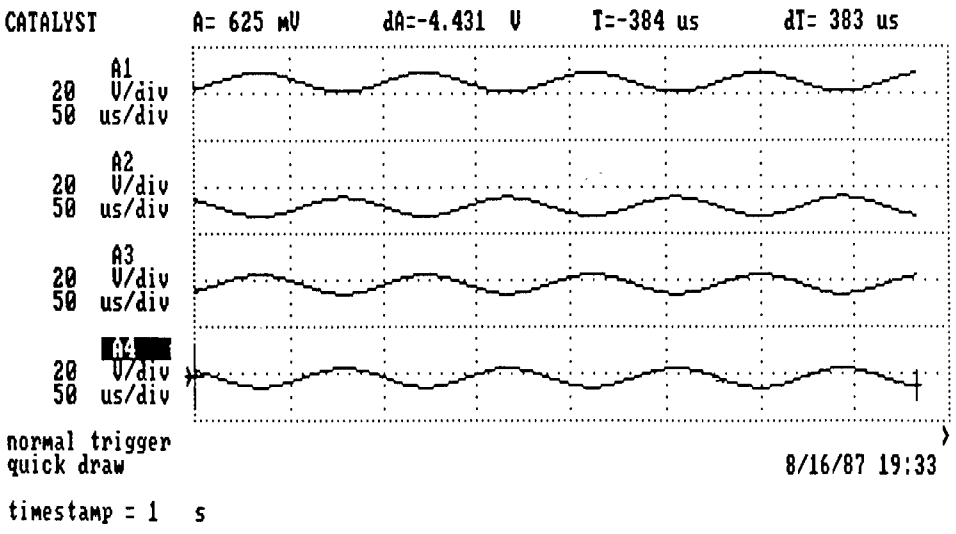
COUPLING

Use the Coupling parameter to set the coupling mode for the inverting and/or non-inverting input for each channel separately. Coupling modes are:

1. +DC – Non-inverting DC coupled / inverting disabled
2. +AC – Non-inverting AC coupled / inverting disabled
3. -DC – Inverting DC coupled / Non-inverting disabled
4. -AC – Inverting AC coupled / Non-inverting disabled
5. d DC – Both inputs DC coupled
5. d AC – Both inputs AC coupled
6. GND – Both inputs disabled

Figure 23 depicts the same signal measured using four different offsets. The signal's DC offset shows the difference between AC and DC coupling. Channel 1 (A1) signal is measured using the non-inverting input in the DC coupled mode. (Notice how the DC offset from the signal source is apparent.). Channel 2 (A2) signal is measured using the inverting input in the DC coupled

mode. Channel 3 (A3) signal is measured using the non-inverting signal in the AC coupled mode. Channel 4 (A4) signal is measured using the inverting input in the AC coupled mode.



Non-inverting/Inverting and DC/AC Coupling Demo

Figure 24

NOTE: Memory Size, Segment Size, Period, Set Trigger, and Set Clkmode are only valid in the Channel 1 column. Information in Channels 2, 3, and 4 is not used.

MEMORY SIZE

This parameter refers to the total amount of memory attached to the 6810, including its internal 512k samples. The 6810's memory size can increase in 512k sample increments using 6310 memory expansion modules; *i.e.*, 512k samples, 1M, 1.5M, 2M . . . to 8M). *Note: After adding memory, you must update this parameter to reflect the current memory size.*

SEGMENT SIZE

Use segment size to control the number of samples stored in memory after each trigger event. The segment size depends on the number of active (ACQUIRE = YES) channels (1, 2, or 4) and the number of segments recorded per channel. Each input channel must have the same segment size and the same number of segments. The segment size set for channel 1 is the segment size used for all active 6810 channels. The number of segments (programmable when SET CLKMODE is YES) for channel 1 is the number of segments used for all active channels. Segment sizes can be set to the following values:

1 ksamples; 2 ksamples; 4 ksamples; 8 ksamples; 16 ksamples; 32 ksamples; 64 ksamples; 128 ksamples; 256 ksamples; 512 ksamples; 1 Msamples; 2 Msamples; 4 Msamples; 8 Msamples.

NOTE: Ensure that the 6810 setup configuration uses less or equal memory than is installed in the system. The maximum memory available depends on the number of 6310 Expansion Memory Modules connected to the 6810. The available memory depending on the number of connected 6310s is:

# of Connected 6310s	Amount of Memory
0	512K
1	1M
2	1.5M
3	2M
4	2.5M
5	3M
6	3.5M
7	4M
8	4.5M
9	5M
10	5.5M
11	6M
12	6.5M
13	7M
14	7.5M
15	8M

The maximum memory must always be less than or equal to the segment size times the number of segments times the number of active channels.

PERIOD

Use line 11 in the 6810 setup menu to set the (f1) sample rate. The sample rate is the same for all four measurement channels. WAVEFORM-CATALYST uses the Period value from Channel 1 for all active channels. Valid inputs for the Period parameter are:

PERIOD	Sample Rate
.2 µsec	5 Msample/sec (Only One channel active)
.5 µsec	2 Msample/sec (One or Two channels active)
1 µsec	1 Msample/sec
2 µsec	500 ksample/sec
5 µsec	200 ksample/sec
10 µsec	100 ksample/sec
20 µsec	50 ksample/sec
50 µsec	20 ksample/sec
.1 msec	10 ksample/sec
.2 msec	5 ksample/sec
.5 msec	2 ksample/sec
1 msec	1 ksample/sec
2 msec	500 S/sec
5 msec	200 S/sec
10 msec	100 S/sec
20 msec	50 S/sec
50 msec	20 S/sec
EXT.	External Clock enabled*

**(Note: Cannot be power-up default setting)*

Slow the sample rate by pressing P(revious); accelerate it by pressing N(ext). When the Period is set to "EXT." make sure that the EXT PERIOD parameter is set to approximate the frequency of the signal being input to the CLOCK IN connector on the 6810's front panel.

EXT. parameter (External Clock Enabled) allows access to the period of the external clock signal connected to the 6810's Clock In connector. To enter External Clock mode, set the Period parameter (line 11) to "EXT.",and when the setup menu is exited (by pressing [space bar]) the user will be prompted. The external clock signal must be a TTL signal of 5 MHz or slower and be connected to the Clock In connector. Valid inputs for the Ext Period parameter are periods of .2 µsec and larger.

SET TRIGGER

If Set Trigger is "yes", and the setup menu is exited (by pressing [space bar]), WAVEFORM-CATALYST displays the following question prompts.

NOTE: Set Trigger "yes" cannot be power-up default setting.)

Each question, followed by its current setting, is accessed by pressing [ENTER].

coupling (0=DC,1=HFR,2=AC,3=LFR) presently = DC ?
slope (0=+,1=-,2=window,3=-h,4=+h) presently = + ?
source (0=ext,1=chan1,2=chan2,3=manual) presently = ch1 ?
upper level (V) presently = 0 ?
lower level (V) presently = 0 ? - not asked when slope=0 or 1
Delay (in eighths: -8 to 247) presently = 0 ?
Trigger holdoff enable (Y/N) presently = Y?

NOTE: Except for the Trigger Holdoff enable which defaults to YES, pressing the "return" leaves the question parameter unchanged.

NOTE: The Set Trigger parameters for the channel 1 column apply to all four 6810 input channels. Channel 1 is the only channel that causes the questions shown above to appear when exiting the 6810 setup menu.

Coupling: Use the Coupling parameter to set the coupling type for the 6810's Trigger In connector. The four coupling modes are:

0 - DC Coupling

1 - High Frequency Reject (cutoff=6500 Hz)

2 - AC Coupling

3 - Low Frequency Reject (cutoff=6500 Hz)

NOTE: If coupling is DC but the trigger source is an AC coupled input channel (channel 1 or 2), the trigger signal is AC coupled.

Slope: The five slope modes are:

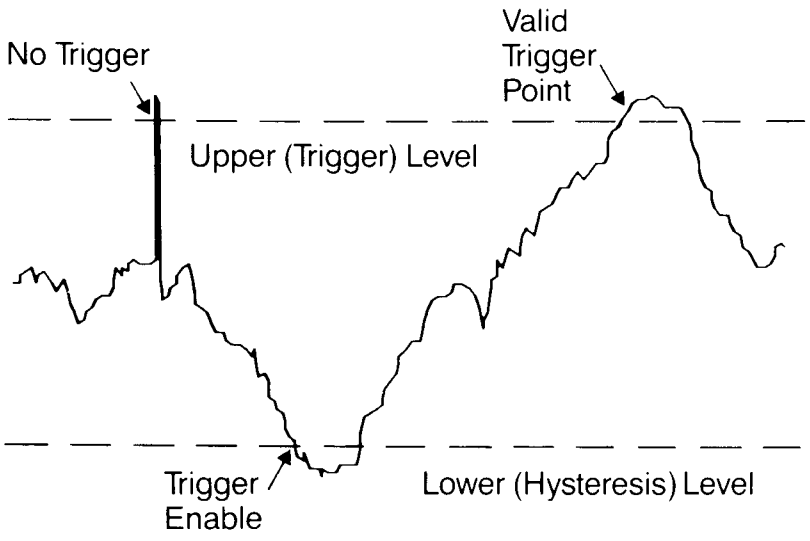
0 - Positive Slope: The 6810 triggers when a rising edge of the signal from the trigger source crosses the trigger threshold (upper level).

1 - Negative Slope: The 6810 triggers when a falling edge of the signal from the trigger source crosses the trigger threshold (upper level).

2 - Window Triggering: The 6810 triggers whenever the signal exits the window formed by the upper and lower trigger thresholds (upper and lower level respectively).

NOTE: Make sure that UPPER LEVEL is greater than LOWER LEVEL.

3 - **Negative Hysteresis:** The 6810 triggers whenever the signal passes completely through the region formed by the upper and lower levels. When operating in this mode, the lower level functions as a hysteresis threshold and generates a hysteresis event, arming the module when a falling edge of the signal crosses it. A trigger occurs when the signal continues through the region and crosses the trigger threshold (formed by the upper level). *A Hysteresis event must occur before each trigger event for the 6810 to trigger.* Hysteresis triggering helps discriminate between noise spikes and the signal when triggering on signals with large amounts of noise.

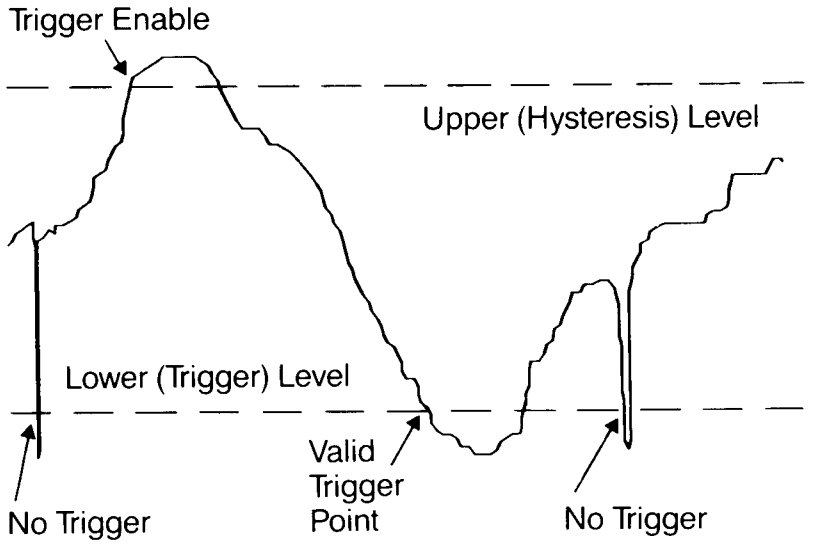


Negative Hysteresis

Figure 25

4 - **Positive Hysteresis:** The 6810 triggers whenever the signal passes completely through the region formed by the upper and lower levels. When operating in this mode, the upper level functions as a hysteresis threshold and generates a hysteresis event and arms the module when a rising edge of the signal crosses it. A trigger occurs when the signal continues

through the region and crosses the trigger threshold (formed by the lower level). *A hysteresis event must occur before each trigger event in order for the 6810 to trigger.* Employing hysteresis triggering discriminates between noise spikes and the signal when triggering on very noisy signals.



Positive Hysteresis

Figure 26

Source: The four valid trigger sources are:

0 = ext – TRIGGER IN signal used as trigger source.
1 = chan1 – Channel 1 Pickoff used as trigger source.
2 = chan2 – Channel 2 Pickoff used as trigger source.
3 = manual – All signal trigger sources (Channel 1, Channel 2 and TRIGGER IN) are disabled. 6810 can only be triggered manually.

INTERNAL TRIGGER LEVELS

In CATALYST, the 6810's programmed internal trigger level refers to the input signal. CATALYST takes the programmed offset into account and adjusts the trigger levels to match the input signal.

Upper Level

The upper level is programmed in volts.

Positive Slope (+) – The upper level functions as a positive slope selective trigger threshold.

Negative Slope (–) – The upper level functions as a negative slope selective trigger threshold.

Window – The upper level functions as a positive slope selective trigger threshold. Make sure that upper level is greater than lower level.

Negative Hysteresis (–h) – The upper level functions as a positive slope selective trigger threshold providing a hysteresis event has occurred on the lower level since the last trigger event.

Positive Hysteresis (+h) – The upper level functions as a positive slope selective hysteresis threshold.

Lower Level

The lower level is programmed in volts. Always make sure that the lower level is less than the upper level.

Positive Slope (+) – The lower level is not used in this mode and the user is not queried for its value.

Negative Slope (–) – The lower level is not used in this mode and the user is not queried for its value.

Window – The lower level functions as a negative slope selective trigger threshold.

Negative Hysteresis (–h) – The lower level functions as a negative slope selective hysteresis threshold.

Positive Hysteresis (+h) – The lower level functions as a negative slope selective trigger threshold providing a hysteresis event has occurred on the upper level since the last trigger event.

DELAY

Trigger delay can be set as Pre or Post–trigger delay. Pretrigger can be specified from 8/8 to 0/8 of the segment size. The trigger can be delayed from 1/8 to 247/8 of the segment size. To obtain the trigger delay time, multiply the fractional Delay parameter times the segment length times the current sample period.

Trigger Holdoff enable?(Y/N): Use trigger holdoff enable to disable trigger events that occur while recording pretrigger data.

When enabled (Y), triggers which occur while the specified length of pretrigger data are being collected are ignored. When disabled (N), a trigger occurring during the collection of pretrigger data is honored, so the segment would have less than the specified length of pretrigger data. The beginning of the pretrigger data will be "garbage."

SET CLKMODE

If Set Clkmode is "yes", and the setup menu is exited (by pressing [space bar]) WAVEFORM-CATALYST displays the following question prompts.

NOTE: Set Clockmode "yes" cannot be power-up default setting.)

Each question, followed by its current setting, is accessed by pressing **[ENTER]**.

1. dual clock mode (0-3) presently = 0 ?
2. post-trigger near length presently = 0 ? Not asked if clock mode is 0 & 2
3. f2 sample period presently = 2 µsec ? Not asked if clock mode is 0
4. Number of segments presently = 1 ?
5. Time stamp res (0=1 µsec, 1=10 µsec...4=10 msec) presently = 10 µsec ?

NOTE: Pressing [ENTER] key without addressing the prompt leaves that particular function unchanged.

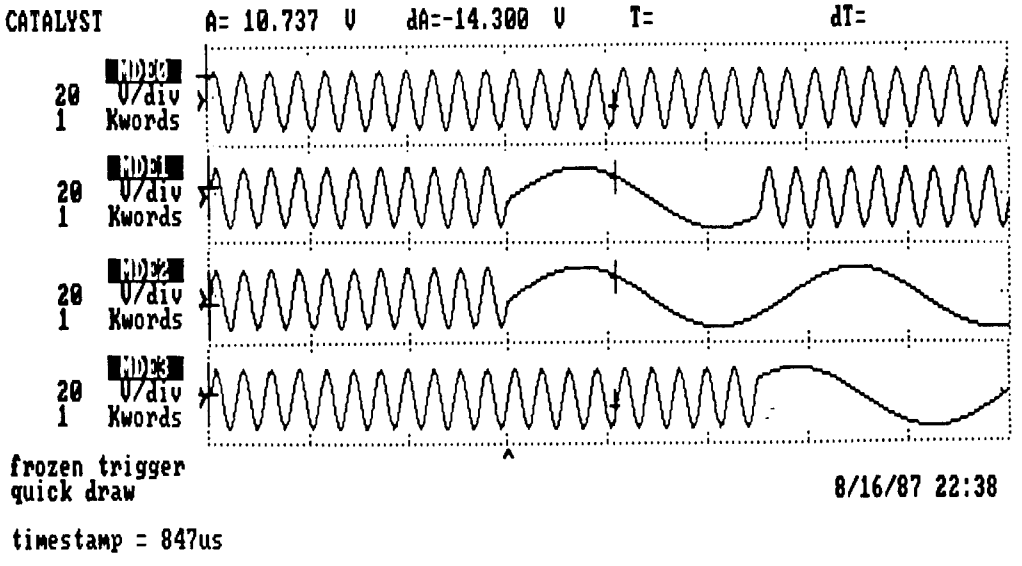
NOTE: The SET CLKMODE parameters for the channel 1 column apply to all four 6810 input channels. Channel 1 is the only channel that causes the questions shown above to appear when exiting the 6810 setup menu.

dual clock mode: Use the 6810 dual clock mode to change the sample rate twice within the same waveform segment. The four dual clock modes are:

Mode	Pretrigger Data	Post-trigger Near Data	Post-trigger Far Data
0	Single Timebase (f1) for entire segment		
1	f1	f2	f1
2	f1	f2	f2
3	f1	f1	f2

Figure 27 depicts the same waveform measured in all four dual clock modes. The f1 sample rate (Period) is 2 µsec and the f2

sample rate is .2 μsec. Pretrigger data is contained in the segment's first 3/8 (384 samples). The post-trigger near length (see below) is 320 samples.



Same Waveform Measured Using All Dual Clock Modes

Figure 27

Post-trigger near length?: The post-trigger near length specifies the second timebase change point (the first change point being the trigger point). It is expressed in samples after the trigger point and ranges from 1 sample to the segment length minus pretrigger samples.

NOTE: The post-trigger near length question is not presented when in dual clock mode 0.

f2 sample period: The f2 sample period is used (and asked by WAVEFORM CATALYST) only when operating in dual clock modes 1, 2, and 3. f2 can be greater than, less than or equal to f1 (specified by PERIOD in the main 6810 setup menu). Valid inputs for f2 are:

.2 μsec – (1 Active Channel only); .5 μsec – (1 or 2 Active Channels only); 1 μsec; 2 μsec; 5 μsec; 10 μsec; 20 μsec; 50 μsec; .1 msec; .2 msec; .5 msec; 1 msec; 2 msec; 5 msec; 10 msec; 20 msec; 50 msec.

Note that the Ext clock is not a valid f2. Also, the Ext Clock is not a valid f1 in Dual Clock Mode 1, 2, or 3.

Number of segments: The number of segments can range from 1 to 1024. This parameter stores the trigger number required after the arm command before data is read out to the remote computer. Each trigger causes the recording of only one segment (for all active channels). The number of segments is the same for all active input channels.

NOTE: when setting the number of segments, do not set the 6810 in a state which requires more memory than is configured and installed in the system. The number of segments times the segment length times the number of active channels must not exceed the total system memory installed (using the 6310 Expansion Memory Module).

Time stamp res? (0=1 μsec,1=10 μsec...4=10 msec): The initial time stamp measures the time from ARM to the first segment's trigger. Each following time stamp measures the time from a preceding segment's trigger to the next segment's trigger. Valid time stamp resolutions are:

Entered Value	Time Stamp Resolution	Maximum (32 bits)
0	1 μsec	71.58 min.
1	10 μsec	11.93 hours
2	100 μsec	4.97 days
3	1 msec	49.71 days
4	10 msec	16 months

This parameter sets the minimum allowable time between counts when recording the time between valid triggers. The counter records the time from the previous segment's trigger (or arm for the first segment's trigger) and saves the value in memory.

ADDING MORE 6810 SETUP CAPABILITIES

The setup menu provides control over two separate 6810 Waveform Recorders (not necessarily in the same instrument mainframe). To control more than two 6810s, add other 6810 setup menus using the WAVEFORM-CATALYST BUILDCAT utility.

WAVEFORM-CATALYST Buildcat Utility

To create a buildcat subdirectory, you need the following:

a. All WAVEFORM-CATALYST Program and Library diskettes, Version 3.00 or higher.

b. Microsoft FORTRAN Compiler Version 4.0 or 4.1

c. HALO '88 graphics package.

To personalize the ten modules listed in the "List Modules" menu:

1. Create a subdirectory on your fixed disk called bldcat: c:\> md\bldcat <ENTER>.

2. Copy mkbcdir.bat from function library diskette 1 into directory bldcat:

   c:\> copy a:mkbcdir.bat c:\bldcat\mkbcdir.bat <ENTER>.

3. Change directory to access bldcat: c:\> cd\bldcat <ENTER>.

4. Type mkbcdir and follow the screen prompts:

   c:\bldcat> mkbcdir <ENTER>.

5. Ensuing screen prompts require that three CATALYST diskettes be copied from drive A:

   a. CATALYST PROGRAM DISK

   b. CATALYST LIBRARY DISK 1

   c. CATALYST LIBRARY DISK 2

After inserting a diskette and pressing any key to continue, its necessary files will automatically copy into the bldcat subdirectory.

6. Following the instructions in your Microsoft Fortran Compiler Manual, version 4.0 or 4.1, install the compiler making sure to create a LARGE library (LLIBFOR7.LIB).

7. Copy HALOF.LIB and HALODVXX>OBJ from your HALO '88 graphics package:

   c:\bldcat> copy a:HALOF.LIB c: <ENTER>.

   c:\bldcat> copy a:HALODVXX.OBJ c: <ENTER>.

CREATING CATALYST PROGRAM DISKETTES

Run buildcat from the bldcat subdirectory and follow the screen prompts. A CATALYST program will be created for:
C:\bldcat> buildcat

INTRODUCTION TO CAMAC

The 6810 waveform digitizing system uses both the IEEE-583 (CAMAC) bus and the IEEE-488 (GPIB) bus for instrument setup and waveform data transfer. The 6810 itself slides into a CAMAC backplane. Therefore, programming across the GPIB often requires additional knowledge of the CAMAC dataway and CAMAC programming codes.

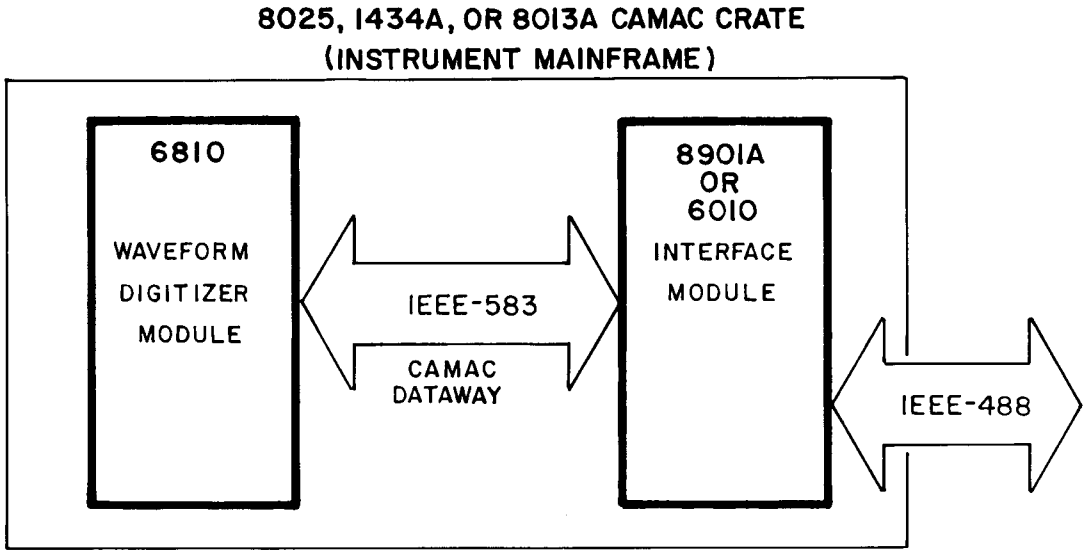


Diagram of 6810/CAMAC/IEEE-488
Figure 28

CAMAC

Common interpretation of the acronym CAMAC is "Computer Automated Measurement And Control." CAMAC does "enable" computer control over multiple measuring instruments. However, strictly speaking, CAMAC is a hardware standard which defines a crate (instrument mainframe), dataway (communication bus on an internal backplane), and the plug-in modules. The CAMAC standard covers both the electrical and physical specifications.

The mainframe (crate) houses the modules and provides them with power. The CAMAC Controller communicates with the 6810 module(s) across the crate's backplane (IEEE-583 bus). The CAMAC command lines setup the 6810 and instruct it to receive data on the write lines. The command lines also instruct the 6810 to send back waveform data on the read lines.

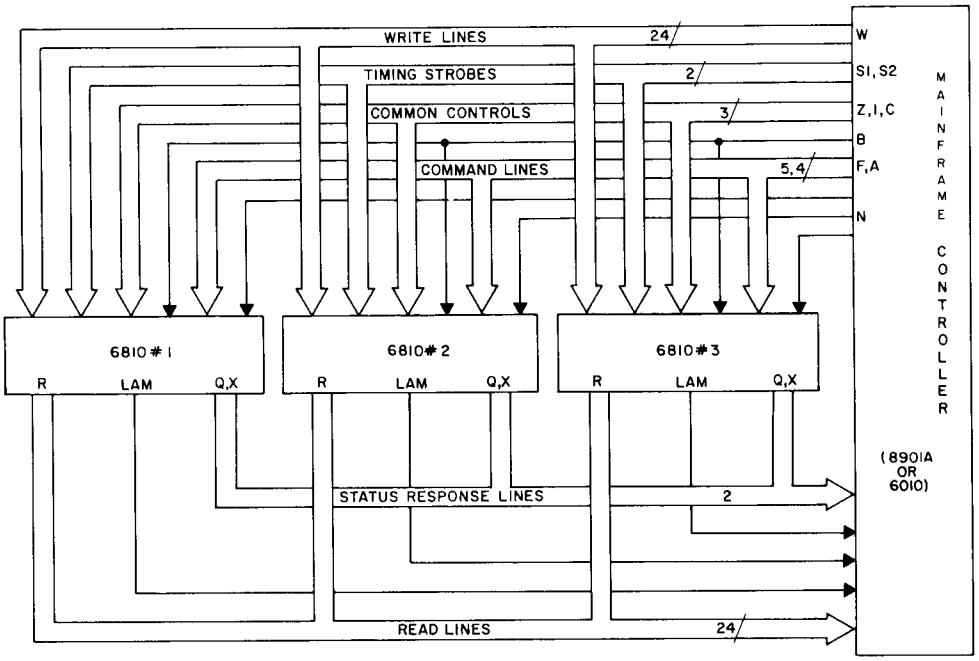


Diagram of CAMAC Dataway Lines for three 6810 Modules and a Mainframe Controller

Figure 29

The CAMAC Dataway

The IEEE-583 Bus, often called the CAMAC Dataway, is a series of bus and individual lines on the crate backplane. The CAMAC dataway links 86-pin sockets, one for each module slot. The dataway includes:

* 24 Read and 24 Write data transfer lines,
* one address line for each module station,
* nine module control lines (five F, four A),
* four global control lines: Initialize (Z), Inhibit (I), Clear (C), and dataway Busy (B),

- a service request line for each module station ("Look At Me" or LAM),
- two module status response lines (Q, X),
- two strobe signal lines (S1, S2).

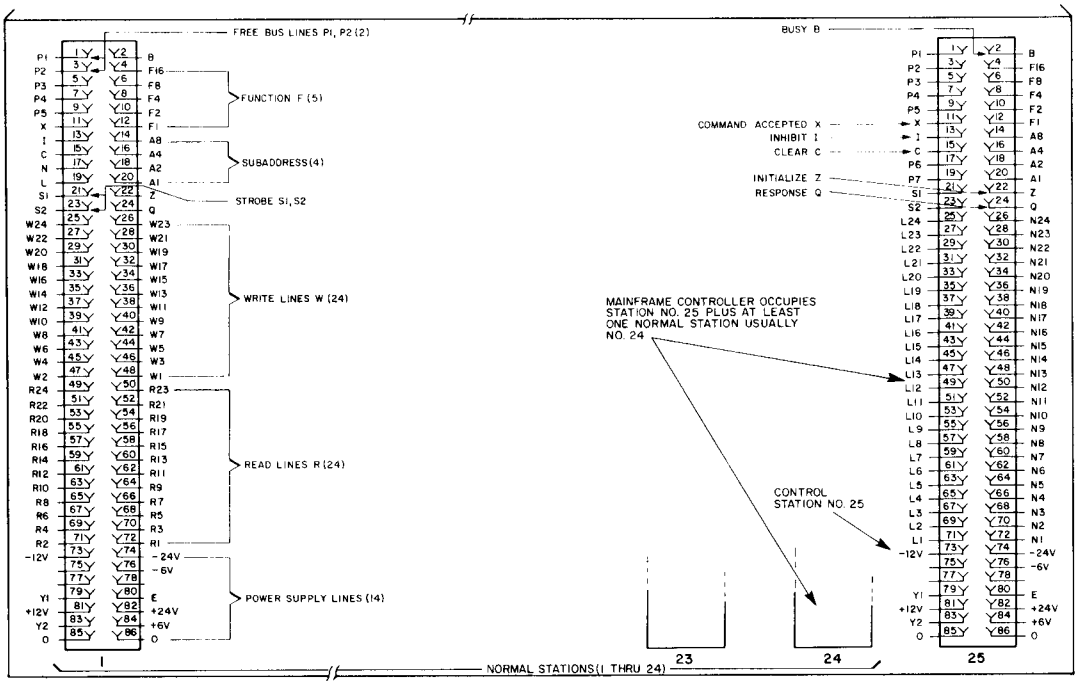


Diagram of the CAMAC Backplane (IEEE-583 Bus)

Figure 30

Dataway Commands

A command consists of signals on the Dataway lines which specify:

N one unique module (via a dedicated line to each individual station [slot]),

A a sub-section of the specified module (via the four subaddress bus lines), and

F the function to be performed (via the five function bus lines).

N Station Number refers to the slot number in which the module is installed. A dedicated N line extends from the

CAMAC Controller to each station in the crate; these lines are not a common bus. The station numbers correspond to those printed on the crate. They are numbered from the lefthand end as viewed from the crate front, beginning with Station 1.

The F and A lines form a common bus to all the stations. Together they address the module to perform a particular function. For example, F(9)A(0) "arms" the 6810 module to accept a trigger.

The CAMAC controller subaddresses a module section via the four "A" bus lines (A8, A4, A2, A1). Simultaneously, the controller sets the signals on five function bus lines (F16, F8, F4, F2, F1) to define actual tasks performed at the specified subaddress in the selected module.

Dataway Operation

In a typical operation, the Controller issues a CAMAC command to specify a station number (N), a subaddress (A), and a function code (F). The command signals are accompanied by a signal on the Busy bus line, which is available at all slots, to indicate the presence of a Dataway operation. In response, the module subaddress will acknowledge a valid command accepted (X response) and act on the command.

If the command requires data transfer, read (R) or write (W) lines will also be used. Thus complete commands will take two general forms:

1) N, F, A

2) N, F, A, W or N, F, A, R

In sending CAMAC commands to a CAMAC controller from a host computer, the letters are replaced by numeric data. In describing or defining the CAMAC commands, the numeric data is placed in parentheses along side the letters for identification. For example, F(9)A(0)N(4) represents the command which would "arm" the 6810 module installed in CAMAC station 4.

The host computer, or GPIB controller, sends the CAMAC controller setup commands and requests for waveform data. It sends these instructions as N,F,A format CAMAC commands. Each CAMAC controller requires these commands in different format: The Model 6010 requires ASCII commands and the 8901A requires binary commands. The CAMAC controller converts these GPIB commands into CAMAC dataway commands.

When a module recognizes a Read command from the CAMAC controller, it establishes data signals on the dataway Read lines. When the CAMAC controller recognizes a Write command from

the GPIB controller, it establishes data on the dataway Write lines. To execute the data transfer, the CAMAC controller then generates two timing signals, strobes S1 and S2, in sequence on separate dataway lines. The strobes act as a clock to transfer data from the dataway into modules (on Write commands) and into the controller (on Read commands).

Any module can request attention via its individual Look–At–Me (LAM) line. For example, the 6810 waveform digitizer can generate a LAM when its memory is full. However, CAMAC will not allow assertion of any LAM line during any dataway operations. Dataway activity is indicated by the presence of the Busy signal.

The four global control lines (Z, I, C, and B) operate on all installed modules. The Initialize (Z) signal has absolute priority over all other signals or controls. It resets all installed modules to a default state. The Inhibit (I) signal inhibits any dataway activity. The Clear (C) line clears selected module registers. Dataway Busy (B) informs modules that a dataway operation is in progress.

All installed modules share control of status response lines, Q and X. A "Q" response from the addressed module indicates a valid data transfer occurred. For example, when reading out digitized waveform data, the 6810 will set Q = 0 to indicate end of memory. An "X" response from the addressed module indicates the last command sent was valid and accepted.

6810 CAMAC OPERATION

This section explains general 6810 operation via CAMAC. For further details, see the "6810 CAMAC COMMAND DETAILS."

Power up Procedure

Upon powering up the instrument housing, the "STATUS OK" LED on the 6810 front panel lights and remains on to verify a valid 6810 setup:

1. if the checksum of the setup information in the battery backed up RAM is correct (*i.e.*, it is the same setup as before the last power down), and
2. if all the setup parameters pass the "verify" tests.

Note: If the LED turns off, either the setup information changed from the previous verification or use (checksum incorrect) or the verify tests failed. The verify tests can fail for one of two reasons:

1) The setup was changed and power was shut off before the checksum was recomputed. Only "VERIFY" F(18)A(6) initiates a verification procedure and computes the checksum.
2) The internal tests failed. If the LED is out on power up, run "verify" F(18)A(6). If it passes, the hardware is functioning correctly. Check the saved setup.

The state of this LED can be read from CAMAC (See VERIFY SETUP section for details.)

Setup and arm procedure:

1. Set 6810 operating parameters - gains, offsets, clock speeds, number of active channels, etc. Then issue the VERIFY SETUP command F(18)A(6) to ensure the setup is valid. Check the result via CAMAC by reading the status byte.
2. Send F(9)A(0) to "arm" the module. The 6810 will take several milliseconds to complete the arm sequence, during which time CAMAC commands to the module will be ignored. Optionally: CAMAC I (Inhibit) can be asserted to inhibit triggers prior to "arming" several modules, then cleared to allow triggers to be recognized by all the modules simultaneously.
3. Supply the module with the required number of triggers to fill the specified number of segments, either using external signals or triggering via CAMAC (F(25)A(0)). To abort digitizing before all the triggers arrive, send F(25)A(1). If enabled with F(26)A(0), the module will assert its CAMAC LAM (Look At Me) line when all specified segments are filled.

Normal Waveform Readout Sequence

The 6810 has the ability to readout data in one of two modes:

Channel Segment Readout

1. To read data from a selected channel and segment:

   Prior to the first read, send F(16)A(5) W(readout offset "block" size), F(16)A(6) and F(16)A(7) to establish an offset from the beginning of the segment to the first sample to be read out.

2. Send F(18)A(channel#)W(segment#) to prepare for data readout from the specified channel and segment. The 6810 will calculate the first sample address from the trigger address, the trigger delay, and the "readout offset".

3. If desired, readout the trigger time interval (timestamp) for this segment using F(2)A(1).

4. Read waveform data using F(2)A(0). Q=1 is returned on all cycles for which valid data is returned. Therefore after reading the last valid word (end of segment), F(2)A(0) will return Q=0. After completion of read out, issue an abort read command (F(25)A(1)) before sending further CAMAC commands.

Note: You need only perform step 1 once. Steps 3 and 4 can occur in any order.

Block Read Sequence

Block readout sequence is not recommended for general use. This method sets up the 6810 for readout faster than the channel segment readout method, but it reads out data with the channels interlaced. (It provides a physical memory dump – The readout might not begin at the segment boundary. The first pretrigger sample might not be the first sample read out.). To locate the first sample of pretrigger, it is necessary to know where the trigger occured within each segment [see F(18)A(5)].

Reading waveform data:

1. Send F(16)A(5), F(16)A(6), and F(16)A(7) to specify the block readout size (The number of words sent before Q=0).

2. Send F(18)A(5) W(start#) to specify the starting address where W = start address in 1kword blocks. For example, if W=8, then the next F(2)A(0) will read sample number 8192 from memory.

3. Read sample data with F(2)A(0). Q=1 will be returned for each sample read. After the requested number of samples have been read, any further reads will return Q=0. After completion of read out, issue an abort read command, F(25)A(1), before sending further CAMAC commands.

Reading setup, trigger time intervals, or stop addresses:

This information is needed to determine the first sample of pretrigger data for each segment and the time between triggers.

1. Send F(18)A(0), F(18)A(11), or F(18)A(10) accordingly to enable block read of the appropriate item. *(Note: Block read of setup may begin with any item and proceed for any number of items, as described in the "6810 CAMAC COMMAND SUMMARY" section.)*
2. Read with F(2)A(1) the desired length of data. Note that Q will allways be 1. If the requested number of segments were not filled (*i.e.*, an abort was issued), then the time interval count and the stop address following the last valid segment will be set to maximum values (2^32–1 [4 billion] and 2^24–1 [16 million], respectively).

6810 CAMAC COMMAND SUMMARY

To enable independent 6810 feature control, each feature (for each channel, if appropriate) is set up by a different CAMAC command. Therefore, a large number of extremely straightforward commands exist.

Most 6810 setup information is programmed by F(16) and F(17), in conjunction with A(0) through A(15). F(19) programs a few items. Setup commands write the least significant eight CAMAC W lines directly into a battery backed up memory which the 6810's microprocessor can read. For example, a "write" using F(17)A(3) would "setup for read" using F(1)A(3). F(2)A(1) would perform the "read".

All setup items can be read back as a block or individually. [See F(18)A(0) for more information on "block read".] Individual items are accessed by sending an F code sixteen less than the code used to write the desired item (to set up the address), then an F(2)A(1) to read the item. Successive F(2)A(1)s will read the following items in the same order as the block read. For example, a "write" using F(17)A(3) would "setup for read" using F(1)A(3). F(2)A(1) would perform the "read".

F(18) contains mostly "prepare to read" commands. Please see the Section *CAMAC COMMAND DETAILS* for further information about "prepare to read" commands. F(2)A(0) reads the time data. Other items (time stamps, stop addresses, setup) are read out by F(2)A(1).

F(18)A(6) and F(18)A(7) are not "prepare to read" commands. F(18)A(6) causes a status byte to be generated which shows any reason a setup may not be acceptable, and attempts to fix the setup. This status byte may be read back. See the section *Verify Setup* and the description of F(2)A(6) in *CAMAC COMMAND DETAILS* for more information. F(18)A(7) causes several internal diagnostic tests to be run. See the section *CAMAC COMMAND DETAILS* for further information about this command.

CAMAC commands other than F(16), F(17), F(18), and F(19) directly control the digitizing hardware, *i.e.*, arm, trigger, or abort; control LAM, and read out data. These commands are listed at the end of this summary.

Note that F(9)A(0) (arm) and most of the "prepare to read" commands take longer than one microsecond to complete. Most CAMAC commands are locked out during this time. Those that aren't are listed at the end of this summary. The commands that take longer than one microsecond to complete (and therefore cause CAMAC lock out) are marked with an asterisk. After

one of these commands is sent, further CAMAC commands (except those noted below) are locked out until the 6810 is ready. They will have no effect and will return Q=0 if attempted during lock out. Use F(11)A(0) to test whether the 6810 has locked out CAMAC.

Please see the following section, *6810 CAMAC COMMAND DETAILS,* for more information on each command.

Write: F(16)A(n). Set up for read back: F(0)A(n), where "n" is one of:

0 Time Stamp Resolution
1 Channel 1 Sensitivity
2 Channel 2 Sensitivity
3 Channel 3 Sensitivity
4 Channel 4 Sensitivity
5 "Block size" for data readout (use before first read)
6 Offset in "blocks" for "read channel #", low byte
7 Offset in "blocks" for "read channel #", high byte
8 Trigger Holdoff enable
9 Trigger Slope
10 Trigger Coupling
11 Trigger Level (upper level for window trigger)
12 Trigger Lower Level for window trigger
13 Trigger Source
14 Low byte, Post-trigger "near" number of samples
15 High byte, Post-trigger "near" number of samples

Write: F(17)A(n). Set up for read back: F(1)A(n), where "n" is one of:

0 Number of Active Channels (= # words / sample)
1 Channel 1 Analog input Offset
2 Channel 2 Analog input Offset
3 Channel 3 Analog input Offset
4 Channel 4 Analog input Offset
5 Channel 1 source and coupling
6 Channel 2 source and coupling
7 Channel 3 source and coupling
8 Channel 4 source and coupling
9 Trigger delay
10 Number of samples per segment
11 Low byte, Number of segments
12 Hi byte, Number of segments
13 Dual Timebase Mode
14 F1 clock code
15 F2 clock code
[F(2)A(1), actually reads the data]

Write: F(18)A(n); (no read back on "prepare to read" commands), where "n" is one of:

0 Prepare to read setup
1 Prepare to read Channel 1 *
2 Prepare to read Channel 2 *
3 Prepare to read Channel 3 *
4 Prepare to read Channel 4 *
5 Prepare to block read from memory *
6 Verify Setup * / Set up for read of status = F(2)A(6)
7 Internal diagnostic tests *
10 Prepare to read trigger address
11 Prepare to read time stamp

Write: F(19)A(n). Set up for read back: F(3)A(n), where "n" is one of:

1 Block write setup registers
2 Active Memory size

Other CAMAC commands:		OK when CAMAC locked out?
F(2)A(0)	Block read data	Yes
F(2)A(1)	Block read registers	No
F(3)A(0)	ID	Yes
F(8)A(0)	Test LAM set and enabled	Yes
F(9)A(0)	Arm *	No
F(9)A(1)	Reset	Yes
F(10)A(0)	Clear LAM	Yes
F(11)A(0)	Test CAMAC lock out	Yes
F(24)A(0)	Disable LAM	Yes
F(25)A(0),A(1)	Trigger, Abort	Yes
F(26)A(0)	Enable LAM	Yes
F(27)A(0)	Test LAM set	Yes

* = causes CAMAC lock out, see note above.

6810 CAMAC COMMAND DETAILS

SETUP COMMANDS

The following commands send setup information to the 6810. On each command, the lower eight bits of the W lines (write data) are saved by the 6810 in battery backed up memory.

When the 6810 is armed, it first verifies that all setup information is legal and attempts to correct illegal states. This action generates a status byte which can be read. "Verify Setup" is available as a separate CAMAC command which can be used at any time to generate this status byte. See "VERIFY SETUP" for more information on this command.

Because of the 6810's internal architecture and the CAMAC requirement that the instrument take no irreversible action before S1 and have output ready by S1, reading back the setup is accomplished by two commands, one to set up the address inside the 6810 and the other to actually read out. All items written by F(16) are addressed by F(0), and all items written by F(17) are addressed by F(1). The memory size, programmed by F(19)A(2), is addressed by F(3)A(2). The item addressed is read out by F(2)A(1). For example, you program the memory size using F(19)A(2) to be 64k. To read out this programmed value, you must first address its register using F(3)A(2). Then perform F(2)A(1) to read out the information. Successive F(2)A(1)s will read out the values which follow as described for F(18)A(0), prepare to read setup, below. Unless the "verify setup" routine has run, the setup read back by F(2)A(1) will be exactly the bytes sent with the last corresponding F(16), F(17), or F(19) command.

NOTE: In all cases below, the word "sample" refers to data from all active channels, which are sampled simultaneously. At a given sampling rate, a given number of samples takes the same time to acquire regardless of number of active channels. Also, the number of words occupied by a segment is the number of samples multiplied by the number of active channels.

The required settings on the W lines for each setup command follow. These settings are returned on the R lines when read back.

F(16)A(0)W(n)

Time Stamp Resolution

n	Resolution	Maximum time (32 bits)
0	1 μsec	71.58 minutes
1	10 μsec	11.93 hours
2	100 μsec	4.97 days
3	1 msec	49.71 days
4	10 msec	over 16 months

This command sets the time per 'tic' of the counter recording the time between valid triggers. The counter's value records the time from the previous segment's trigger (or arm, for the first segment) to this segment's trigger. The record is saved for each segment. These values can be block read or read individually with each segment. See "Prepare to Read" commands, below.

F(16)A(c)W(n)

Channel n Sensitivity, c = 1 through 4

n	volts/LSB	Full Scale p-p
0	100 μV	409.6 mV
1	250 μV	1.024 V
2	500 μV	2.048 V
3	1 mV	4.096 V
4	2.5 mV	10.24 V
5	6.25 mV	25.6 V
6	12.5 mV	51.2 V
7	25 mV	102.4 V

F(16)A(5)W(n)

Block Length - length is $2^n \times 1024$, where n = 0, 1, 2, 3,... words. Examples of n values:
0 = 1K, 1 = 2K, 2 = 4K, ... 13 = 8 Megawords

This command is used in conjuction with F(16)A(6) and F(16)A(7) in one of two ways:

1. When executed prior to F(18)A(5), prepare to read, F(16)A(5) determines the block size in words that can be read by F(2)A(0) before Q=0 is returned. F(16)A(5) and F(16)A(6), F(16)A(7) determines the number of these blocks.
2. When executed prior to F(18)A(1-4), prepare to block read, F(16)A(5) determines the block size and F(16)A(6), F(17)A(7) determines the number of blocks to skip before the first word is read out.

NOTE: a read sequence can always be aborted,(see F(25)A(1) below). Also note that, like other settings, this setting is only

brought into the microprocessor's memory from the battery backed up CAMAC setup memory on "arm" [F(9)A(0)] or "verify" [F(18)A(6)]; changing this setting does have an effect until one of these commands is received.

F(16)A(6)W(LSB) "number of blocks", low byte

F(16)A(7)W(MSB) "number of blocks", high byte

For example, for 258 blocks, LSB=2, MSB=1.

Unlike any other setup commands, the two bytes entered by these commands are read directly from the battery backed up setup memory every time a "read channel n" command is received. This two byte number, multiplied by the block size, gives the number of samples to skip before the first sample to be read out.

NOTE: if the offset is greater than or equal to the segment size, the offset is not applied. This command is useful for computers that must read the data in small blocks and have considerable overhead associated with reading each block. The readout offset may be used to skip hundreds of blocks, at a time cost of only two CAMAC cycles. To read data from start of segment, simply set these values to zero–no offset.

F(16)A(8)W(n) Trigger Holdoff enable

n = 0	no holdoff
n = 1	holdoff enabled

When enabled, triggers which occur while the specified length of pretrigger data are being collected are ignored. When disabled, a trigger occurring during the collection of pretrigger data would be honored, so the segment would have less than the specified length of pretrigger data. The beginning of the pretrigger data will be "garbage".

Note: the 6810 saves the address of the sample during which trigger was received, see the section "Dual Speed Clock Timing" for details. Also note that if the CAMAC trigger command F(25)A(0) is received while pretrigger data is being collected and holdoff is enabled, it is not ignored. Holdoff has no meaning if no pretrigger information is desired.

F(16)A(9)W(n) Trigger Slope

n	slope
0	positive slope
1	negative slope
2	window trigger
3	positive slope trigger with neg hysteresis
4	negative slope trigger with pos hysteresis

If positive slope is set, the trigger "edge" occurs when the selected trigger signal rises through the trigger level set by F(16)A(11). If negative slope is set, the trigger edge occurs when selected trigger signal falls through the level set by F(16)A(11). The other trigger modes use both the trigger "upper" level, set by F(16)A(11), and the trigger "lower" level, set by F(16)A(12). If window trigger is selected, then the trigger edge occurs when the selected trigger signal either rises through the level set by F(16)A(11) or falls through the level set by F(16)A(12). Therefore, window trigger can generate a trigger whenever the selected signal leaves the amplitude range between the two thresholds. The hysteresis trigger modes produce a trigger at either the upper or lower level as selected, but then will not accept another trigger until the signal has exceeded the other level. When the "arm" command F(9)A(0) is received, the trigger circuitry is set in a state as if a trigger had just occurred. This ensures that the first trigger will be subject to hysteresis constraints, if any.

F(16)A(10)W(n) Trigger Coupling

n	coupling
0	DC
1	AC, high frequency reject
2	AC
3	AC, low frequency reject

The 3 dB point of both the low and high pass filters is approximately 6500 Hz.

F(16)A(11)W(n) Trigger "Upper" Level (positive slope level for window trigger and hysteresis trigger modes; the only level used for simple positive or negative slope modes.) n = eight bit offset binary fraction of full scale setting [see F(16)A(1 through 4) above]. When the trigger source is the External trigger input, n = an eight bit fraction of ± 5 V. Offset binary means n=0 is minus full scale, n=255 is plus full scale. See F(16)A(9) for information on how this level is used.

F(16)A(12)W(n)

Trigger "Lower" level (Negative slope trigger level for window trigger and hysteresis trigger modes). n = same as for F(16)A(11). See F(16)A(9) for information on how this level is used.

F(16)A(13)W(n)

Trigger Source

n	source
0	External trigger input
1	Channel 1
2	Channel 2
3	(CAMAC trigger, F(25)A(0), only)

F(16)A(14)W(LSB)

Low byte, Post-trigger "near" number of samples

F(16)A(15)W(MSB)

High byte, Post-trigger "near" number of samples

These bytes must be set if dual timebase mode 1 or 3 is used. The number of post-trigger "near" samples can be 4 to 65534. *Example:* To select 300 samples Post-Trigger Near, send F(16)A(14) W(44) and F(16)A(15) W(1). See F(17)A(13), below, for more information on the dual clock modes, and the section *TRIGGER and DUAL SPEED CLOCK TIMING* for details on the timing of clock speed transitions.

F(17)A(0)W(n)

Number of Active Channels

n	# channels	Maximum sampling speed
1	1	5 MHz
2	2	2 MHz
4	4	1 MHz

F(17)A(1 through 4)W(n)

Channel n Offset, n = 1 through 4

n is an 8-bit offset binary number which ranges from -50% to +50% of the full scale p-p voltage setting [see F(16)A(1-4)]. For example, if full scale voltage = 4.096 V p-p:

n=0 means -50% of 4.096 V or -2.048 V and input is unipolar +

n=128 means 0% of 4.096 V or 0 V and input is symmetrically bipolar

n=255 means +50% of 4.096 V or 2.048 V and input is unipolar -

F(17)A(5)W(n) Channel 1 Source and Coupling

F(17)A(6)W(n) Channel 2 Source and Coupling

F(17)A(7)W(n) Channel 3 Source and Coupling

F(17)A(8)W(n) Channel 4 Source and Coupling

n	Meaning
0	Non-inverting input, DC coupled.
1	Non-inverting input, AC coupled.
2	Inverting input, DC coupled.
3	Inverting input, AC coupled.
4	Differential input, DC coupled.
5	Differential input, AC coupled.
6	Both inputs internally grounded, DC coupled
7	Both inputs internally grounded, AC coupled

Differential input means that both inverting and non-inverting inputs are active. Inputs present a 1 MΩ input impedance even when internally grounded.

F(17)A(9)W(n) Trigger Delay

Number of eighths of a segment from trigger to the first sample in each segment. Any value of n will be valid. n is interpreted as ranging from -8 to +247. Values less than 0 give pretrigger data, values greater than 0 delay the trigger. Some valid examples are:

-8 All data is pretrigger. Recording in the segment stops at trigger.

-3 3/8ths of each segment pretrigger.

0 All post-trigger, recording starts at trigger.

+n After the trigger, the 6810 collects (n+8)/8 times the segment length of data. The last 8/8ths of data are kept.

F(17)A(10)W(n)

Number of Samples per Segment

n	# samples/segment	n	#samples/segment
0	1K (1024)	7	128K (131072)
1	2K (2048)	8	256K (262144)
2	4K (4096)	9	512K (524288)
3	8K (8192)	10	1Meg (1048576)
4	16K (16384)	11	2Meg (2097152)
5	32K (32768)	12	4Meg (4194304)
6	64K (65536)	13	8Meg (8388606)

Note that a setting of 13 is only possible in one channel mode and 12 is possible on one or two channel mode. See the section "VERIFY SETUP" for information concerning the checks applied to this setting.

F(17)A(11)W(LSB)

Low Byte, Number of Segments

F(17)A(12)W(MSB)

Hi Byte, Number of Segments

The number of segments can be set from 1 to 1024. This number of triggers will be required after each arm command; each trigger will cause the recording of a segment. The number of segments × samples/segment × number of active channels = total memory used per acquisition.

Example: To collect 300 segments following each arm command, send F(17)A(11)W(44) and F(17)A(12)W(1). Please see the Section "Verify Setup" for information concerning the checks applied to this setting.

F(17)A(13)W(n)

Dual Timebase Mode

n	pretrigger	Post-trigger "near"	Post-trigger "far"
0	----- single timebase at f1 -----		
1	f1	f2	f1
2	f1	f2	f2
3	f1	f1	f2

Each segment can be considered as three parts: pretrigger data, the first n samples of post-trigger data, and the rest of the post-trigger data. The dual timebase mode selects the sampling clock for each of these parts, as shown above. 0 means that all data is acquired using a single timebase, at the f1 clock. The other modes permit "importance" sampling. f1 and f2 may be any timebase.

See F(16)A(14) and F(17)A(9) for information on specifying the lengths of the three parts of each segment.

See *TRIGGER and DUAL SPEED CLOCK TIMING* for more information.

F(17)A(14)W(n)

f1 Sampling Clock Code

n	Rate	n	Rate
0	External clock	9	10 KHz
1	20 Hz	10	20 KHz
2	50 Hz	11	50 KHz
3	100 Hz	12	100 KHz
4	200 Hz	13	200 KHz
5	500 Hz	14	500 KHz
6	1 KHz	15	1 MHz
7	2 KHz	16	2 MHz - 2 Chans only
8	5 KHz	17	5 MHz - 1 Chan only

NOTE: the maximum permitted sampling clock depends on the number of active channels, see F(17)A(0). All active channels are sampled simultaneously at all speeds. If this setting is 0 all sampling is done at the external clock rate. The settings of the dual clock mode and the f2 clock rate have no effect.

F(17)A(15)W(n)

f2 Sampling Clock Code

Same coding as f1 (except 0 is invalid for f2), see F(17)A(14).

Note that in dual timebase modes f1 and f2 must not both be greater than or equal to 2 MHz.

F(18)A(7)

Internal Diagnostic Tests

These tests are not system tests, but verify the lowest level of functionality of the digital controlling hardware. They thoroughly test microprocessor access to the dual ported RAM which holds setup programmed from CAMAC, the microprocessor's internal RAM, and calculate a checksum of the control program ROM. This command takes several milliseconds to complete. Use F(11)A(0) to wait for completion. After this command executes, the following is true:

1. the setup is preserved.
2. the "STATUS OK" LED is on if the dual ported RAM tested OK; otherwise, it is off.
3 Six F(2)A(1)'s can be issued to read the following result report: Bytes 1,2: Count of errors in dual ported RAM, high byte first. Byte 3: Pattern of errors in dual ported RAM. Any bit position in which an error ever occurred is set to

"1" in this byte. Bytes 4,5: Checksum of program ROM, high byte first. Byte 6: Count of errors in the microprocessor's internal RAM. This count remains at 255.

NOTE: these bytes are stored into the dual ported RAM to be made available over CAMAC. If the "STATUS OK" LED is not on after F(18)A(7) is executed, the dual ported RAM has errors and the values in these bytes may be compromised. Other dependencies: If the control program checksum is incorrect, all tests may be compromised. If the microprocessor's internal RAM has errors, the dual ported RAM test results might be compromised – the test uses three bytes of the internal RAM. The ROM checksum and the internal RAM test do not use the internal or dual ported RAM, only the microprocessor's registers and, of course, the program ROM.

F(19)A(1)W(BYTE)

Block Write Setup, Registers

This command can be used after F(18)A(0) or any other command which can set up an address for F(2)A(1). It writes successive bytes into successive addresses less than 4096 in the dual ported RAM in the Setup memory. Note that it is possible to write beyond the end of the setup information and eventually overwrite the stop trigger addresses using this command. This command does not provide any time savings when using either the LeCroy 8901A or 6010 CAMAC controllers, but it does simplify programming. A single loop repeating this one command permits a setup value array to be sent to the 6810.

F(19)A(2)W(n)

Active Memory size n corresponds to the total active memory in units of 512k. Since 512k words of memory is built into the 6810, W is one greater than the number of 6310 memory modules attached, as follows:

n	Memory size
0	No checking (see explanation below)
1	512k (internal memory only)
2	1 Meg
3	1.5 Meg
4	2 Meg
5	2.5 Meg
6	3 Meg
7	3.5 Meg
8	4 Meg
9	4.5 Meg
10	5 Meg
11	5.5 Meg
12	6 Meg
13	6.5 Meg

14	7 Meg
15	7.5 Meg
16	8.0 Meg

The 6810's microprocessor cannot sense available memory. This command is available so that this information can be entered into the battery backed up memory as part of the setup. When the arm command F(9)A(0) is received, or when the "verify setup" command F(18)A(6) is received, the 6810 checks that the requested number of segments at the requested segment size will fit in the specified amount of memory. If not, the 6810 will force the number of segments (not the segment size) down to a number that fits in the available memory. It also checks that at least one segment will fit in memory. If code 0 is specified for memory size, the 6810 never performs the checks described above. This permits the "arm" command to complete a few dozen micro seconds faster.

NOTE: "Verify Setup", F(18)A(6), is described in its own section, below.

READ COMMANDS

All "prepare to read" commands which setup to read digitized data take longer than 1 μsec to complete. They are handled by the 6810's built-in microprocessor. After the command is sent, further CAMAC commands which require microprocessor service or attempt to access the battery backed up setup information are locked out until the 6810's microprocessor is busy. They will return Q=0 if attempted during lock out. Use F(11)A(0) to test whether the 6810 has locked out CAMAC and wait for the completion of the "prepare to read" commands.

Data is read using F(2)A(0). Q=1 is returned whenever valid data is returned. After the last sample has been read, further F(2)A(0) cycles return Q=0.

NOTE: Do not issue F(2)A(0) to the 6810 after issuing a "Prepare To Read Digitized Data" command, until CAMAC lockout is deasserted [F(11)A(0) returns Q = 1].

NOTE: Prepare to read digitized data commands are ignored when the main address counter is enabled because they would load a new address into the main address counter. The main address counter is enabled while digitizing and during data readout. Therefore, to avoid reading all sought data and to send another "prepare to read data" command, issue the abort command first; see F(25)A(1) for details.

The commands prepare to read setup, trigger times, and stop addresses do not require microprocessor intervention; therefore,

they complete within one full speed CAMAC cycle. These commands load an appropriate address into counters which address the battery backed up memory where the items are stored. These items are read with F(2)A(1), which increments the counters.

Note that any setup command as well as intersegment service while digitizing loads a new address into these counters; F(2)A(1) would then read the byte last accessed. F(2)A(1) always returns data and Q=1. The user must know how many bytes to read.

F(18)A(0) Prepare to Read Setup

This causes address 1 to be the next address read out of the setup memory. The bytes read by F(2)A(1) will be in the following order:

0	Time Stamp Resolution Code
1	Channel 1 Sensitivity
2	Channel 2 Sensitivity
3	Channel 3 Sensitivity
4	Channel 4 Sensitivity
5	"Block size" for Data Readout
6	Offset for "read channel #", Low Byte
7	Offset for "read channel #", High Byte
8	Trigger Holdoff enable
9	Trigger Slope
10	Trigger Coupling
11	Trigger Level
12	Trigger Low Level for Window Trigger
13	Trigger Source
14	Low Byte, Post-trigger "near" Length
15	High Byte, Post-trigger "near" Length
16	Number of Active Channels
17	Channel 1 Offset
18	Channel 2 Offset
19	Channel 3 Offset
20	Channel 4 Offset
21	Channel 1 Source and Coupling
22	Channel 2 Source and Coupling
23	Channel 3 Source and Coupling
24	Channel 4 Source and Coupling
25	Trigger Delay
26	Number of Samples per Segment
27	Low byte, Number of Segments
28	High byte, Number of Segments
29	Dual Timebase Mode
30	f1 Sampling Clock Code

31 f2 Sampling Clock Code
32 Memory Size Code
33 Status – Error Code from Verify Setup
34 Checksum – complement of sum mod 256 of preceding bytes.
35 State of "setup OK" and "armed" LEDs. (0=both off, 16=status O.K., 32=armed, 48 = both on. Updated when these LEDs change.)
36–41 Results from F(18)A(7). Please see the description of that command, above.

Reading beyond this point will eventually reach the trigger addresses, stored starting at address 1024.

F(18)A(c)W(n)

Prepare to Read Channel "c", "Segment n"

(Note: upon receiving this command, CAMAC is locked out.) This command takes less than 2 msec to complete, whereupon CAMAC is re-enabled. Then send F(2)A(0). Wait for completion of this command using F(11)A(0).) This command prepares to read out channel data channel specified on the A lines from the segment specified on the W lines. "c" may be 1 through 4, but should not exceed the number of channels which were active when the data was acquired. n may be 0 through 1023, but should not exceed the number of segments acquired. The 6810 calculates the first sample address to read out from the trigger address, the trigger delay, and the "readout offset" (see F(16)A(5)). After this command completes, F(2)A(0) will read the desired data and F(2)A(1) will read the four byte trigger time interval recorded for this segment; see F(18)A(11) for more information about the trigger time interval.

F(18)A(5)W(n)

Prepare to Read from Specified Address

n = start address in 1 kbyte blocks, *i.e.*, if n = 8 then the next F(2)A(0) will read sample number 8192 from memory.

NOTE: F(16)A(5) must be sent before this command is first used. (Note: upon receiving this command, CAMAC is locked out. This command takes less than 500 μsec to complete, whereupon CAMAC is re-enabled and F(2)A(0) can be sent. Test for completion of this command using F(11)A(0).)

The data memory layout is very simple. The first segment starts at address zero and ends at (segment length × number of channels) minus one. The second segment starts in the following byte and ends at 2×(segment length × number of channels)– 1, etc. Within each segment data for each sample is stored in consecutive words, channels 1 through the number active, in order. It is

necessary to read the trigger addresses to know where the trigger occurred within each segment since the trigger address may be anywhere within a segment. The trigger address shows the contents of the main address counters when trigger was recognized, but trigger is actually honored only on a four sample boundary (where the lowest two bits of the address are zero). Please see *TRIGGER and DUAL SPEED CLOCK TIMING* for more information.

F(18)A(10) Prepare to Read Trigger Addresses.

This command causes address 1024 to be the next address read out of the setup memory by F(2)A(1). The trigger addresses are stored sequentially for each segment starting at this address in the battery backed up "setup" memory. Each is three bytes long. These values are the contents of the main address counters at the next End Of Conversion pulse after trigger was recognized. Each three byte value is read out low byte first. Due to hardware constraints, the trigger is not necessarily honored at this instant; that is, the post-trigger sample count does not begin. The address at which trigger is honored can be determined from the trigger address. Please see the section "Trigger Timing" for more information. If less than 1024 segments are acquired, three bytes of all ones are present after the last valid trigger address. Note that reading beyond the last valid trigger address does not get to the trigger time intervals, but wraps from address 4095 to 0.

F(18)A(11) Prepare to Read Trigger Time Intervals.

This command causes address 4096 to be the next address read out of the setup memory by F(2)A(1). The trigger times are stored sequentially for each segment starting at this address in the battery backed up "setup" memory. Each value is four bytes long. Each four byte value is the count of the time increments specified by F(16)A(0) between the previous segment's trigger and this segment's trigger, except the first four byte value is the time from arm to the first segment's trigger. Each four byte value is read low byte first. If less than 1024 segments are acquired, four bytes of all ones are present after the last valid trigger time interval.

OTHER CAMAC COMMANDS

F(2)A(0) Read Data

Returns 12 bits of data in the twelve least significant bits of the CAMAC dataway. Returns Q=1 when valid data is returned. An

F(18)A(1, 2, 3, 4, or 5) command should precede the first F(2)A(0). **Warning:** do not issue this command while digitizing.

NOTE: readout of digitized data must either end or be aborted. See F(25)A(1) below.

F(2)A(1) Read Registers

Returns one byte of data in the eight least significant bits of the CAMAC dataway. Returns Q=1 when valid data is returned. A setup command or F(18)A(0, 10, or 11) command should precede the first F(2)A(1). Will not function while CAMAC is locked out; returns Q=0 in that case. **Warning:** do not issue this command while digitizing.

NOTE: readout of registers never needs to be aborted.

F(3)A(0) ID

Returns twelve bits of data in the least significant bits of the CAMAC dataway. The value of these 12 bits should be 6810.

F(8)A(0) Test if 6810 has set LAM, and if LAM is enabled

Returns Q=1 if the instrument is currently asserting LAM on the CAMAC dataway, otherwise returns Q=0. See also F(27)A(0), below.

F(9)A(0) Arm

(Causes CAMAC lock out) This command causes the 6810 to set up for acquisition, and commence taking data. The time from decode of F(9)A(0) until the completion of this sequence is approximately 2.0 milliseconds. The "ARMED" LED lights and CAMAC is re-enabled on the first sampling clock after the arm sequence is completed *[NOTE: if the LED does not light, you have selected "external sampling clock" and are not supplying one; see F(9)A(1) below]*. After the unit is armed and CAMAC is re-enabled, F(25)A(1) may be used to ABORT digitization on the next sampling clock.

F(9)A(1) Reset

Resets the 6810's microprocessor, disables the Main Address Counter, etc. After approximately 100 milliseconds, the 6810 will "wake up" as if it had just been powered on. Any digitization or readout in progress is aborted.

F(10)A(0)	Clear LAM
F(11)A(0)	Test Lockout. Returns Q=1 if CAMAC lockout is *not* in effect, Q=0 if CAMAC access to the dual ported setup RAM is locked out.
F(24)A(0)	Disable LAM Disables the assertion of LAM by this instrument on the CAMAC dataway.
F(25)A(0)	Trigger This command triggers the unit from the CAMAC dataway.
F(25)A(1)	Abort Disables the Main Address Counters, thus ending either digitization or readout of digitized data on the next clock. *NOTE: To abort data readout, it is necessary to send one more F(2)A(0) which causes "clock" to counters after sending F(25)A(1).*
F(26)A(0)	Enable LAM Allows LAM condition to assert LAM on dataway; if not enabled, 6810 will only assert LAM internally. Enables the 6810 to conditionally assert the Look At Me line on the CAMAC dataway. LAM is generated when acquisition is completed; that is, when the last waveform memory segment has been filled.
F(27)A(0)	Test if 6810 has set LAM, regardless of LAM ENABLE. The 6810 returns Q=1 if it has asserted LAM. Otherwise, it returns Q=0. *Note: if F(26)A(0) has not been issued to the 6810, then the LAM will only be asserted internally.*
F(18)A(6)	Verify setup (Causes CAMAC lockout) This command MUST be issued after setting operating parameters or the 6810 cannot be guaranteed to be in the selected parameter modes when the module is armed F(9)A(0). Please see the separate "VERIFY SETUP" section which follows.
F(2)A(6)	Setup to read the status from last Verify Setup command, F(18)A(6). After this, the next F(2)A(1) reads the status byte produced from the last "verify" of the setup due to F(18)A(6).

Note: F(18)A(6) verifies the setup and reads the status byte. It is not necessary to issue F(2)A(6) immediately after F(18)A(6) in order to read back the status byte.

VERIFY SETUP

The setup programmed from CAMAC is held in battery backed up RAM. It is accessible from CAMAC at the full 1 MHz speed. Whenever this setup data is read out of the battery backed up RAM for use within the 6810, the setup is verified, any anomalies are corrected, and the corrected setup is written back to the battery backed up RAM.

Primarily, the "verify" routine ensures that the 6810 cannot be put into an anomalous state. It also can be a convenience for the user in several ways. *For example:*

- If the number of segments is programmed as 1024, the maximum number of segments possible will always result (assuming that the memory size has been programmed).
- If the number of samples per segment code is programmed as 13 (8 Megasamples), the maximum number of samples possible in one segment will always result (assuming that the memory size has been programmed).
- If either f1 or f2 or both are set to 5 MHz, the highest possible clock speed for the selected number of channels will always result.

Only VERIFY SETUP F(18)A(6), causes verification to occur.

VERIFY SETUP has one non-obvious function: as soon as the setup is verified, the gain, offset, and coupling settings are put into effect. This causes relay closures. Relays take several milliseconds to debounce.

VERIFY writes a status word and a checksum to the CAMAC accessible RAM along with the corrected setup. At power on, the setup is read from this battery backed up RAM and verified in order to set the "STATUS OK" LED. The checksum is the complement of the sum (modulo 256) of the bytes that preceded it.

The status byte indicates what, if anything, was corrected by the verification routine. The bits in the status byte have the following meanings:

Bit 0: Illegal value – some item was set to a value which can never be valid.

Bit 1: Sampling clock speed set too high for number of active channels

Bit 2: Setup would have caused clock speed toggle between 5 and 2 MHz, which is impossible.

Bit 3: Post-trigger "near" number of samples exceeded the total post-trigger length.

Bit 4: Number of segments × number of samples per segment × number of channels exceeded programmed memory size.

Bit 5: Number of samples per segment × number of channels = # words of memory per segment exceeded memory size.

Bit 6: "Upper" and "Lower" trigger levels were reversed.

Bit 7: unassigned, always 0.

If several items were corrected, several bits in the status byte may be on. At any time, F(2)A(6) may be issued to cause the next F(2)A(1) to read the status byte produced from the last "verify" of the setup.

NOTE: F(18)A(6) also performs this action, i.e., it is not necessary to issue F(2)A(6) immediately after F(18)A(6) in order to read back the status byte.

While verification is in progress the "STATUS OK" LED on the 6810's front panel lights and CAMAC is locked out. This command takes between 3 and 3.5 msec to complete. You may test completion using F(11)A(0). When verification is completed, the LED stays on if the setup was correct as entered from CAMAC and has not been changed in any way. If the LED goes out, something has been corrected. The status byte can be read to find out what corrections were necessary, if any. Or, the complete setup can be read back to find which values were changed.

NOTE: once a setup is verified, it will pass all tests if verified again. Therefore, if VERIFY SETUP does not leave the "STATUS OK" LED lit and you wish to read out the status byte, you must read it before issuing either VERIFY SETUP again or the status byte will change to zero.

Verification performs the following checks in this order:

1. Check settings which range from 0 to something for out of range settings. If a setting is out of range, it is replaced with the default value. The checks are:

WHAT	MAXIMUM	DEFAULT - meaning
Time stamp resolution	4	4 - 10 msec
Trigger slope	4	0 - Positive slope
Trigger coupling	3	2 - AC

Trigger Source	3	0 - External trigger
Samples per segment	13	0 - 1024
Dual clock mode	3	0 - clock 1 only
f1 frequency	17	14 - 500 KHz
Memory size	16	0 - No checking
pretrigger trig holdoff	1	1 - enabled
Gain, channels 1..4	7	4 - 10.24 V F.S.
Block Read size	12	2 - 4K samples
Coupling, chans 1..4	7	0 - (+) input, DC

Because the setup is held in battery backed up RAM, these tests will all be passed if each item has ever been set properly.

2. Number of active channels must be 1, 2, or 4; other settings are never valid. Default is next higher valid number of channels, except settings higher than 4 default to 4.

3. If f2 will be used (f1 is not set to external and clock mode is not set to 0 = clock 1 only) then check that f2 setting is between 1 and 17; other settings are never valid. If the f2 setting is invalid the dual clock mode is defaulted to f1 only.

4. Number of segments must be 1 to 1024. Other settings are never valid. Default is 1 segment.

5. If dual clock mode is 1 or 3 (so the clock speed is supposed to change after the first 'n' samples of post-trigger, called the post-trigger "near" length), check that the post-trigger "near" length is at least 4. Settings less than 4 are never valid. Default is 100.

6. Check that the segment size, which is specified in logical samples, multiplied by the number of words per logical sample (*i.e.*, the number of active channels) is less than or equal to the memory size. If the memory size code is zero, the memory size is assumed to be 8 Megawords. On error, segment size is defaulted to memory size.

7. If the dual clock mode is not 0 (both clocks will be used), check that f1 and f2 are not both either 2 MHz or 5 MHz and not the same. The 6810 cannot toggle between 2 MHz and 5 MHz. On error, the dual clock mode is defaulted to 0 = f1 only.

8. If the trigger slope/mode is window or hysteresis trigger, check that the "upper" trigger level is actually above or the same as the "lower" trigger level. If not, reverse them.

9. If the memory size code is not zero, check that the number of samples per segment × number of channels multiplied by

the number of segments will fit in the programmed memory size. On error, the number of segments defaults to the maximum number that will fit.

10. Check that both f1 and f2 are less than or equal to the maximum clock speed available for the requested number of channels. Default for either is the maximum permitted clock speed for the requested number of channels.
11. Check that the post-trigger "near" number of samples is less than the total post-trigger length. If not, post-trigger near length is defaulted to total post-trigger length minus 64 samples.

After these checks, the "STATUS OK" LED goes out if any bits in the status byte are on. The updated LED state is copied back to the battery backed up RAM together with the verified setup.

TRIGGER and DUAL SPEED CLOCK TIMING

The next three sections, *Extra Post-Trigger Sampling, Dual Speed Clock Switching,* and *Trigger Dead Time Between Segments,* contain information to help you correctly interpret the timing relationship between the trigger and the collected samples.

Extra Post-Trigger Sampling

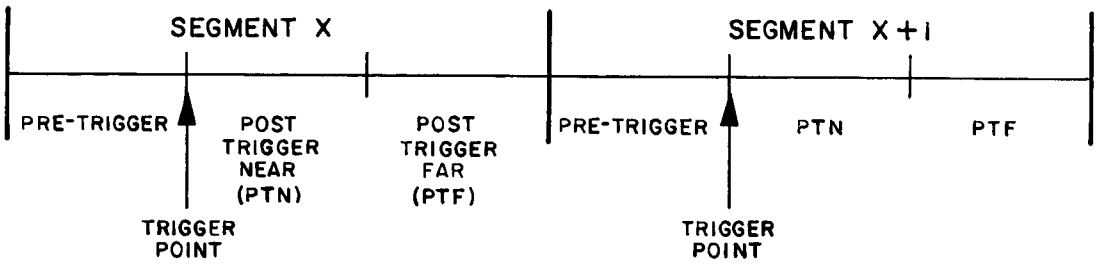
Each segment acquired by the 6810 is a "circular buffer"; that is, after it is filled the next sample overwrites the first sample, etc. "Trigger" commences the number count of the post-trigger samples desired. After the appropriate number of post-trigger samples are acquired, the segment ends and the process is repeated with the next segment (if any). Constraints imposed by our system restrict the address on which a segment can end. Therefore, up to ten extra words are written to the memory.

NOTE: This worst case is possible only in 5 MHz, one channel, multi-segment operation. These extra post-trigger samples overwrite what would be the first pretrigger samples.

The "channel segment readout" commands, F(18)A(1) through F(18)A(4), read out the data as if the number of pretrigger and post-trigger samples were recorded precisely as requested. Therefore, the trigger address will be at the correct position, and the time relative to trigger can be calculated. The extra post-trigger samples appear as the first samples read out. Up to the first ten samples read out from each segment in one channel mode, or the first five samples in two channel mode, or the first two samples in four channel mode should be considered invalid.

Dual Speed Clock Switching

The clock can switch between f1 and f2 at three places: trigger, end of the first n samples of post-trigger, and end of the segment.



Segmented Memory using Dual Speed Clock

Figure 31

The dual clock mode, set by F(17)A(13), determines which of these three points cause a clock switch. If the clock rate remains the same, no unusual timing occurs at that point. In dual clock mode 0, the clocks never switch.

Because the trigger is asynchronous to the sampling clock, a one sample uncertainty exists in the trigger timing relative to the previous or next sample. This is true for any sampled system. Therefore, avoid clock switching at the event of interest and execute it either just before or after the point of interest. A typical use of the dual speed clock concerns capturing an event with a brief very fast beginning followed by a long "decay", where the entire event is too long to be sampled at the high rate. Dual clock mode 3 (pretrigger and first n samples of post-trigger at f1, the remainder of post-trigger at f2) would likely be used with f1 fast and f2 substantially slower. In this case the clocks switch after the first n samples of post-trigger and at the end of each segment. Note that dual clock mode 3 does not switch clock speeds at the trigger point.

Dual clock modes 1 (f1-f2-f1) and 2 (f1-f2-f2) cause a clock switch at trigger. Therefore, in these cases the trigger should precede the event of interest.

Dual Clock Switching at Trigger

The following information concerns calculating the time between events on opposite sides of a clock switch. Avoid such a situation when the highest timing accuracy is required.

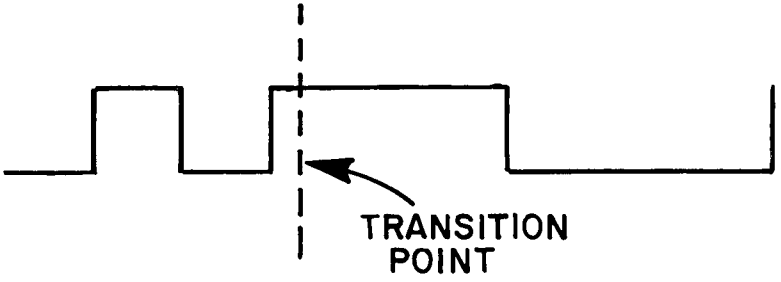
1. Switching from any low clock speed (1 MHz or slower) to 2 MHz or 5 MHz

   The last cycle of the low speed clock is aborted and the high speed clock commences within a few hundred nanoseconds. For example, if there are "n" samples pretrigger, the time between all samples from number 0 to (n–1) is at the low speed clock; the time between sample n and n+1 and all after is at the high speed clock; and the time between sample (n–1) and n is an indeterminate period which will be less than that of the low speed clock.

   NOTE: The high speed clock should persist for a time equal to at least one half cycle of the low speed clock.

2. Switching from any speed 1 MHz or slower to any other speed 1 MHz or slower.

   The clock period can only be changed at a transition. If the trigger address points to sample "n", then the time between samples 0 to n is determined at the first clock rate, the time between samples n+1 and all after is determined at the second clock rate, and the time between samples n and n+1 is either. The probability that the time from n to n+1 will be the second clock period is determined by the first clock. The probability is very high if the first clock rate is 20 KHz or below.



Clock Period Change Occurs only at Transition Point
Figure 32

3. Switching from 2 MHz or 5 MHz to any speed 1 MHz or slower

   When the high speed clock is at a high level, the clock is switched to the low speed clock, which is assumed to be

stopped at a high level, and the low speed clock is begun. (The assumption will always be met if the high speed clock has been selected for a time equal to or greater than a half cycle of the low speed clock.)

The "pipeline" from clock generation to End Of Conversion is over 500 nsec. Therefore, one more 2 MHz clock pulse or two more 5 MHz clock pulses are "in the pipe" and cannot be recalled when the switch occurs. For example, if the trigger address points to sample "n" and f1 = 5 MHz, then the time between samples 0 to n+2 is 200 nsec, the time between n+3 and all after is at the second clock period, and the time between n+2 and n+3 is unknown (either rate).

Dual Clock Switching After "Post-Trigger Near"

The one sample uncertainty of trigger relative to next sample also applies to this transition, since it occurs at a user specified number of samples post-trigger. However, since this transition can be predicted [that is, the post-trigger near (PTN) count is known], the pipeline effects mentioned above are compensated for automatically by the 6810.

1. Switching from any speed 1 MHz or slower to 2 MHz or 5 MHz.

   As above, the last cycle of the low speed clock is aborted and the high speed clock commences within a few hundred nanoseconds. The abort comes when the signal Sampling Clock corresponding to the last PTN sample is counted, typically about 500 nsec after the start (rising edge) of the low speed clock cycle.

2. Switching from any speed 1 MHz or slower to any other speed 1 MHz or slower.

   As noted above, the decision to switch clocks is generated when the signal Sampling Clock corresponding to the last PTN sample is counted. This is typically about 500 nsec after the start (rising edge) of the low speed clock cycle. This cycle will complete, and clock cycles after that will be at the second clock speed. The time between the last PTN sample and the next sample after that will still be determined by the first clock.

3. Switching 2 MHz or 5 MHz to any speed 1 MHz or slower.

   When the high speed clock is at a high level, the clock is switched to the low speed clock, which is assumed to be stopped at a high level, and the low speed clock is begun. (The assumption will always be met if the high speed clock has been selected for a time equal to or greater than a half cycle of the low speed clock.)

Dual Clock Switching at End of Segment

The clock switch at the end of segment always occurs during those few samples which are overwritten by the extra post-trigger samples discussed above. These samples should be ignored, so this clock transition is of no concern.

Trigger Dead Time Between Segments

At the end of each segment, the 6810 must read and save the Trigger Address and the Trigger Time Interval for that segment. Trigger is inhibited until these actions are completed, about 160 microseconds. During this time the next segment's pretrigger data (if any) is being collected.

3 THEORY OF OPERATION

FUNCTIONAL DESCRIPTION

6810 Block Diagram

The basic 6810 is a four-wide CAMAC module containing an input signal-conditioning board, an ADC board, a control board, and a memory board.

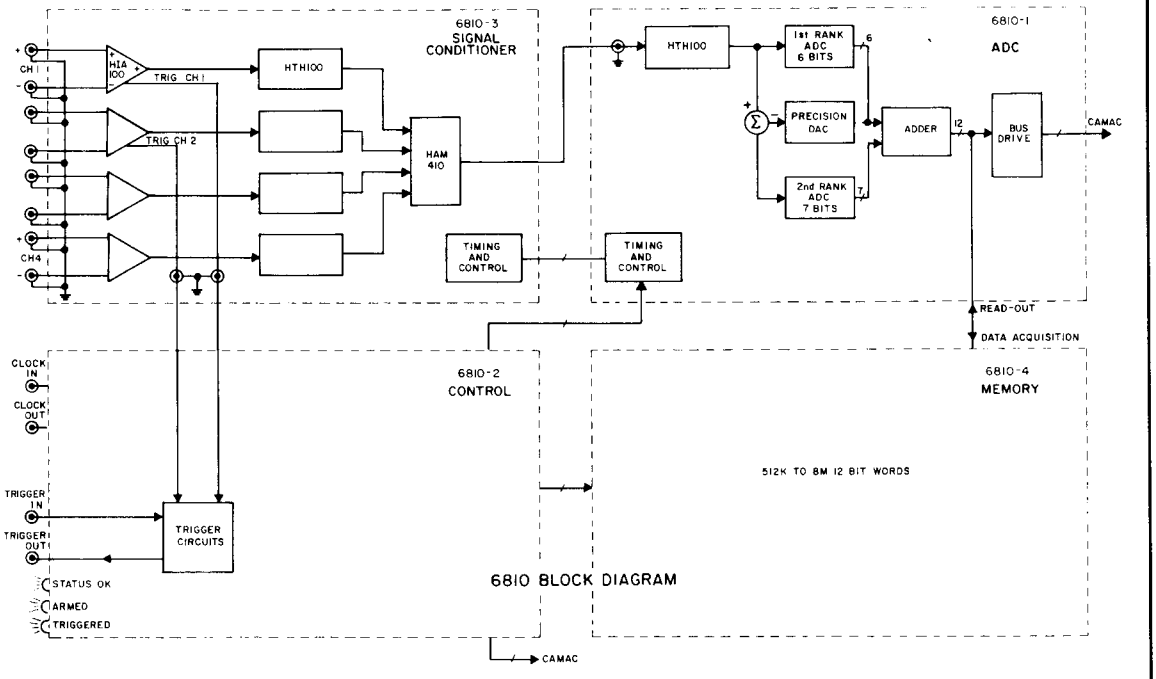
The signal-conditioning board (-3) accepts one to four differential inputs, scales them in programmable gain amplifiers, simultaneously samples the amplifier outputs, and then multiplexes the outputs into the ADC board (-1). The 6810 can run in a 1, 2, or 4 channel mode with maximum sampling rates of 5, 2, and 1 MHz respectively.

After the ADC board resamples the signal from the -3 board, it goes through a two-pass conversion of 6 bits and then 7 bits to generate the final 12 bit output. This output is sent to the memory board (-4) on a bidirectional data bus.

The memory board contains 512k words per board and can be expanded to a maximum of 8 Mwords with up to fifteen 6310 Memory Modules. When the data in the memory are read out, they go to the -1 board on the same data bus as was used in acquisition. Bus drivers then transfer the information to the CAMAC dataway.

The control board (-2) accepts the control information from the Controller module in the CAMAC mainframe. The sampling clock is also generated on the -2 board. The external clock input goes to this board, and the "Clock Out" signal for running multiple 6810's is also generated here. Both an external trigger input and a trigger output for running multiple modules go to and from the -2 board. The only indicator lights on the 6810 are mounted on this board. There is a status check light, a light showing that the unit is armed and ready to be triggered, and a light showing that it has been triggered.

There are no other input/output connections to the 6810 than those shown in the following block diagram. All the boards take their power from the CAMAC mainframe.



6810 Block Diagram

Figure 33

SPECIFICATIONS

6810 AND 6310

All specifications refer to the guaranteed minimum performance of the entire 6810/6310 digitizing system. All selectable parameters are IEEE-583 (CAMAC) bus programmable.

Total Dynamic Accuracy

Signal Frequency	Signal-to-Noise Ratio	Harmonic Distortion
200 kHz	67 dB	-70 dB
1.0 MHz	66 dB	-68 dB
2.5 MHz	62 dB	-62 dB

Performance measured by comparing a digitized bipolar 95% FS sinewave using internal 5 MHz clock against ideal results.

Analog Inputs

Connectors: 2 BNC type coaxial per channel (+ and –)

Quantity: 1,2 or 4 input channels, simultaneously sampled

Channel Isolation: 66 dB minimum between any two channels

Input Modes:
1. Differential (both + and – active)
2. Non-inverting (+ active, – grounded)
3. Inverting (– active, + grounded)
4. Both connectors grounded

Command Mode Rejection Ratio (differential input mode):

0.4 V, 1 V, 2 V, 4 V ranges: 66 dB @ DC, 50/60 Hz, 400 Hz
63 dB @ 100 kHz

10 V, 25 V, 50 V, 100 V ranges: 54 dB @ DC, 50/60 Hz, 400 Hz 51 dB @ 50 kHz

Common Mode Voltage: 125 V max. on 10 V, 25 V, 50 V, and 100 V ranges
5 V max. on 0.4 V, 1 V, 2 V, and 4 V ranges

Bandwidth: DC to 2.5 MHz minimum

Pulse Response: Tr <120 nsec, with <5% overshoot

Coupling: AC or DC

Input Impedance: 1 MΩ, 40 pF

Voltage Range: Selectable in 8 steps

Full scale Input voltage	Sensitivity
400 mV	100 μV
1 V	250 μV
2 V	500 μV
4 V	1 mV
10 V	2.5 mV
25 V	6.25 mV
50 V	12.5 mV
100 V	25 mV

Overload Protection: ±100 V AC or DC continuous

Overload Recovery Time: 1 μsec to within ±1.5% from a 3× full scale, 10 μsec duration input

DC Gain

Non-linearity: ±0.1% maximum of full scale

Offset: Up to ±50% full scale. Selectable in 256 steps

Timebase

Selectable Internal Sample Clock Rates:

5M samples/sec*
2M samples/sec**
1M samples/sec
500k samples/sec
200k samples/sec
100k samples/sec
50k samples/sec
20k samples/sec
10k samples/sec
5k samples/sec
2k samples/sec
1k sample/sec
500 samples/sec
200 samples/sec
100 samples/sec
50 samples/sec
20 samples/sec

*1 channel mode only **1 or 2 channel modes only

Dual Timebase: Four modes 2 selectable timebase changes within each memory segment. Sample rate changes at trigger point and 'N' samples after the trigger point in any combination:

Mode	Pre-trigger	Post-trigger Near	Post-trigger Far
0	rate 1	rate 1	rate 1
1	rate 1	rate 2	rate 1
2	rate 1	rate 2	rate 2
3	rate 1	rate 1	rate 2

Sample rate 1 and rate 2 may be any of the internal rates
Clock In disabled in dual timebase mode, Clock Out available

Clock In: BNC connector

Any external frequency from DC to 5 MHz. Must be a 74 High Speed CMOS series TTL compatible signal

Clock Out: BNC connector

Buffered internal sample clock
50 Ω drive capability
Short circuit protected
40 nsec maximum propagation delay

Analog-to-Digital Conversion

Resolution: 1 : 4096 (12 bits)

Aperture Uncertainty: <50 psec @ 5 MHz internal clock rate

Triggering

Minimum Trigger Signal Duration: 50 nsec

Trigger Source: Selectable from either external (Trigger In), internal, or manual (bus command)

Trigger In: BNC connector ;1 MΩ input impedance; Protected to ±50 V; Range from -5 V to +5 V

Internal Trigger: Pickoff from channel 1 or 2
Range from - Full scale to + Full scale

Trigger Level: 256 steps across range
1 level for single slope trigger modes
2 independent levels for window and hysteresis modes

Trigger Modes: Positive slope
Negative slope
Window
negative hysteresis
positive hysteresis

Trigger Coupling: DC; AC

Low frequency reject (-3 dB @ 36kHz, 20 dB/decade roll off)

High frequency reject (-3 d/b @ 36 kHz, 20 dB/decade roll off)

Trigger Not Accepted During:

1. Programmed "Trigger Disable"
2. Pre-trigger recording when "Trigger Holdoff" enabled
3. Post-trigger recording
4. First 160 micro seconds after last post-trigger sample in the previous memory segment

Trigger Out: BNC connector

Trigger signal for synchronized multiple 6810 operation

50 Ω drive capability

Short circuit protected

80 nsec max propagation delay

Pretrigger: Portion of memory filled with waveform data occurring before valid trigger condition

Selectable in 1/8ths of the memory segment length from 0/8 (no pretrigger data, 100% post trigger) to -8/8 (100% pretrigger data).

Delayed Trigger: Time delay from valid trigger condition to the start of memory segment recording. Selectable time T=(L)(S)(P) where:

L=selectable memory segment length fractions (1/8 to 247/8)

S=number of samples per memory segment

P=sample interval

Example: Sampling at 1MS/sec with a segment length of 4096 samples and a delay trigger setting of 19/8 yields 9.73 msec delay after the trigger before recording begins.

(1 μsec/sample)(4096)(19/8)=9.73 msec

Time Stamps: The elapsed time from Arm to first Trigger, from first Trigger to second Trigger, and so on, each value stored in a buffer

Applies when number of channel memory segments >1

1024 time stamp buffers (bus readable as a block)

32-bit resolution

Selectable time sensitivity:

Sensitivity (1 bit)	Maximum Representable Time Before Buffer Rollover (32 bits)
1 μsec	71.58 minutes
10 μsec	11.93 hours
100 μsec	4.97 days
1 msec	49.71 days
10 msec	>16 months

Waveform Memory

Internal: 512k samples

Expansion: Additional 512k samples per each Model 6310 Memory module 8M samples maximum total memory via 15 Memory modules Total memory required for application = (S)(G)(C) where:

S=number of samples per memory segment
G=number of memory segments
C=number of active channels (1, 2, or 4)

Segmentation: Memory divided into segments; separate trigger for each segment, records only to end of segment for each trigger

Selectable pretrigger/post-trigger percentage; percentage same for all segments on all channels

Dual timebase for each segment, same mode for all segments

Number of Segments: Selectable in binary increments from 1 to 1024

Segment Size: Selectable in binary increments from 1024 samples to the full memory length

Segment Record Rate: Sample rate divided by samples per segment 4880 segments/sec maximum (5 Megasample/sec, 1024 sample segment)

Readout:
1. Entire active memory
2. Any active channel's memory
3. A memory section starting at any particular segment sample point (Offset command) and terminating at any other sample point in active channel memory (Abort command)

Readout Rate: 225 ksample/second maximum via LeCroy 8901A IEEE-488 Interface

Status Indicators

LED's: STATUS OK–Received valid setup command across bus

ARMED – Currently digitizing

TRIG'D – Trigger accepted and 6810 now digitizing post-trigger samples, if any selected

Module I.D.: Bus readable binary value "6810"

Mechanical

Packaging: R.F. shielding in conformance with IEEE-583 Standard (CAMAC)

Module	Size	Height	Width	Depth
6810	4 slots	221 mm	68 mm	292 mm
6310	1 slot	221 mm	17 mm	292 mm

Power:	MODULE	+6 V	−6 V	+24 V	−24 V
	6810	6A	3A	1.2A	1.2A
	6310	1.7A	–	–	–

Environmental

Operating Temperature: +15 to +35° C (IEEE-583 instrument mainframe maximum exhaust temperature must be less than 50° C)

Storage Temperature: −10 to +50° C storage

Operating Humidity: 10% to 90% non-condensing

Operating Altitude: 0 to 10,000 feet above sea level

APPENDIX A: GLOSSARY

A

Aperture uncertainty

The variation (rms) in A/D sampling period. Aperture uncertainty translates into measurement amplitude errors, especially on fast changing signals. Therefore, uncertainty should be small for accurate pulse risetime and falltime measurements.

B

Bandwidth

The useful input frequency range before internal filtering elements cause substantial signal attenuation. The upper limit of the frequency range equals the frequency of 29% attenuation (-3 dB). Since the 6810 bandwidth begins with DC signals, the upper limit equals the bandwidth frequency.

Bipolar signal

A dynamic signal which changes between positive and negative voltage levels.

BLOCK READ sequence

CAMAC bus commands required to initiate a transfer of digitized waveform data from the 6810 to a host computer via an external bus. The external bus is usually IEEE-488 (GPIB).

BNC connectors

Coaxial connectors used for interconnecting high frequency signals. The typical connector bandwidth is over 1 GHz.

BUILDCAT utility

Software to reconfigure WAVEFORM-CATALYST software to contain a user-selected set of CAMAC instrument drivers.

C

CAMAC

IEEE-583 Computer Automated Measurement And Control standard.

The standard defines instrument module form factor, power consumption, programming code format, a communication bus, the instrumentation mainframe (crate), and power supply levels to simplify interchangeability.

CAMAC controller

A CAMAC module which controls all the instruments within a CAMAC mainframe. The controller addresses each installed instrument via dedicated lines and transfers commands and data via a common bus in the CAMAC mainframe backplane.

CAMAC lockout

An internal condition of the 6810 which prevents CAMAC access to dual-ported memory while the microprocessor needs it. It can be tested using F(11) A(0).

CAMAC N slot number

The mainframe slot number pointed to by the 6810's front-panel arrow. During bus operation, the GPIB to CAMAC interface addresses this CAMAC slot to communicate with the 6810.

CAMAC station	See CAMAC N slot number.
Channel isolation	The ratio of signal amplitude on one channel to signal leakage into other channels, usually specified in deciBels, below the carrier.
Coupling	Filtering on the signal or trigger inputs. DC coupling means no filtering; AC coupling consists of a capacitor in series with the input to create a high pass filter effect. Other coupling types include high or low pass filter.

D

Differential inputs	An inverting and non-inverting input pair designed to remove signals common to both inputs and pass difference signals. Common mode signal examples include induced line frequency noise and bias signals.
DIP switch	A package of miniature ON/OFF toggle switches. DIP means Dual Inline Pin package for PC board mounting.
Dual clock mode	A sample clock mode for reducing waveform data storage requirements by sampling at fast rates only during pre-selected times.
Dual timebase	(see Dual clock mode)

E

Engineering Change Number (ECN)	A number assigned to any LeCroy product modification for upgrade tracking purposes.
External clock	A front-panel sample-clock input for synchronizing several 6810 modules to obtain multichannel simultaneous sampling or for synchronizing one or more 6810 modules to an external frequency source.
External signal conditioning	Any type of amplifier, attenuator, transducer bias circuit, or converter which modifies the signal to match trigger or signal input characteristics of the 6810 or enables a transducer to function. 6810 built-in conditioning eliminates the need for external conditioning in most situations.

F

Full scale voltage range	The maximum voltage which the 6810 can accurately record. Eight selectable ranges, from 400 mV to 100 V, allow the user to match the full scale voltage range with the input signal to maximize vertical resolution.

G

GPIB
A General Purpose Interface Bus, defined by the IEEE-488 Standard, for interconnecting instrumentation to a host computer for purposes of automation. Up to 15 instruments and controllers can be interconnected via one bus.

GPIB address
A selectable address from 0 to 31 for any instrument attached to the IEEE-488 Standard Interface Bus (GPIB).

GPIB controller
The computer which controls the activity of all instruments on the IEEE-488 Standard Interface Bus (GPIB). The controller instructs the instruments to be talkers (feed data onto the bus), listeners (accept data/commands from the bus), or inactive.

H

Harmonic distortion
Non-linear distortion of a sinusoidal input signal which causes harmonics (sines of frequencies equal to integer multiples of the input sine) to be added to the original signal. The numeric value equals the square root of the sum of the power in all the harmonic frequencies divided by the power in the fundamental, usually expressed in percentage or dBc.

High byte
Most significant eight bits of a two byte word. The 6810 uses a two-byte word to represent each 12-bit output waveform sample point. The most significant 4 bits exist in the lower 4 bits of the high byte. The upper 4 bits of the high byte are unused, irrelevant, and should be ignored.

Host controller
A computer with the ability to control the GPIB, store data, and execute an instrument control program.

Hysteresis
The failure of a signal to return to an initial value or via the same path. Hysteresis triggering means the signal must pass through a different level than the trigger level before the 6810 will re-arm and accept another trigger.

I

IEEE-583 backplane
The CAMAC motherboard which contains the address lines and data bus. All CAMAC modules communicate digitally via the CAMAC (IEEE-583) backplane.

Importance sampling
See Dual clock mode.

Independent feature control
The ability to set each 6810 function without modifying the settings of other functions.

Input mode
One of four configurations for optimizing the 6810 to accurately measure different signals. These configurations consist of

	inverting single-ended, non-inverting single-ended, differential, and grounded input modes.
Input impedance	The shunt resistance, capacitance, and inductance value from the input to chassis ground in single-ended mode and from (+) input to (-) input in differential mode.
Input voltage range	See full scale voltage range.
Internal trigger	Trigger initiated from either channel 1 or 2 signals passing through a selectable analog level.

L

LED	Light Emitting Diode, used for indicating instrument operating status.
Look-At-Me (LAM)	A digital service request made by the 6810 to the CAMAC controller via the CAMAC backplane. LeCroy 8901A and 6010 CAMAC controllers translate this signal into an SRQ digitial service request on the GPIB.
Low byte	Least significant eight bits of a two byte word. The 6810 uses a two-byte word to represent each 12 bit output waveform sample point.

M

Mainframe	The chassis which houses one or more digitizer modules, expansion waveform memory, other instrument type modules, and the CAMAC controller.
Mainframe Controller	Either of LeCroy's Model 8901A and Model 6010 GPIB to CAMAC crate controllers.

N

Negative slope	The falling edge of a signal.
Non-linearity	Deviation from direct proportionality.

P

Parallel port	Communication port for transferring data on several lines synchronously (bit parallel, byte serial).
Peak-to-peak voltage	The difference between the maximum voltage and the minimum voltage of a signal within a specified time window.
Positive slope	The rising edge of a signal.

Post-trigger near	In dual clock mode, a selectable number of sample points from the trigger point onward. The limit on post-trigger near is the total number of post-trigger samples.
Pulse response	The digitized waveshape compared to the original pulse input which shows the linearity of gain, phase, and offset versus frequency.

R

RAM	Random Access Memory; a data storage device which allows access to any memory location without regard to the previously accessed location.
READ sequence	The CAMAC bus commands required to retrieve and transfer status data from the 6810. See also BLOCK READ sequence.
R.F. shielding	Shielding to prevent radio frequency electric fields from generating a noise voltage in signal paths.
ROM	Read Only Memory; a permanent, non-erasable, data storage device which allows extremely rapid access to data.

S

Sampling rate	The rate at which an analog signal is measured and converted to digital 12-bit data.
Segment	A memory segment or fraction of the active memory. The number of 6810 memory segments and the segment size are user selectable. Each segment can store pre- and post-trigger data. Digitized data continuously fills a memory segment in an overwriting, circular fashion as soon as the previous segment is filled (for the first segment, as soon as the digitizer is armed). A trigger terminates the overwriting according to the pre-selected pre-/post-trigger ratio.
Serial port	A communication port for transferring data on a single line (bit serial). Other lines are often used for ground and initiating communication.
Signal-to-noise ratio (SNR)	The ratio of an rms sinusoidal input signal to the rms noise, usually expressed in deciBels.
Status byte	One byte of readable data which describes the functional status of up to eight parameters on the 6810 module at that point in time.

T

Terminator (memory)	A resistive termination on the memory access bus to prevent signal reflections. Without termination, the reflections could cause erroneous data storage or readouts.

Throughput	The effective rate of data transmission through the waveform acquisition system. The sample rate, active memory length, data transfer rate to the host computer, host computer display or storage time, digitizer re-arm time, and time until trigger all reduce the waveform throughput time.
Time base	The sample period or time between two samples. This definition differs from that for an oscilloscope (time/CRT division), since either the entire digitized waveform acquisition or just a subsection can be displayed.
Time stamp	The trigger arrival time is stored in a separate buffer for each of the waveform memory segments. The first time stamp indicates the time from "arming" the digitizer until the first trigger occurred. The second and onward time stamps represent the time between memory segment trigger arrival times.
Time stamp resolution	The time resolution of the trigger-arrival time stamp. The resolution is selectable from 1 μsec to 10 msec. It is stored in one of 1024 (maximum) 32-bit buffers.
Trigger level	The selectable voltage level which causes a trigger signal to be generated. For internal trigger, this level can be selected from negative full scale to positive full scale. For external (front panel input) trigger, this level can be selected from −5 V to +5 V. The resolution of this digitally selected trigger level is 8 bits or 256 levels. Thus it is selected numerically, with 0 representing a trigger level of negative full scale (−5 V), 128 representing 0 V, and 256 representing positive full scale (+5 V).
Trigger threshold	See Trigger level.

U

Unipolar signal	A dynamic signal which either contains only positive voltage levels or contains only negative voltage levels.

V

Vertical resolution	The total number of voltage levels (*i.e.*, 4096 for the 12-bit 6810 digitizer) or digital output code "counts". The vertical resolution is specified in terms of digital output bits for high speed "flash" type ADCs, such as used in the 6810 digitizer. For the 6810, the vertical resolution is 12 bits which represents 4096 distinct levels.
Vertical sensitivity	The vertical resolution divided by the full scale voltage on the selected range. Determines the smallest detectable level on a single-shot acquisition. Signal averaging on repetitive signals can reduce the vertical sensitivity for a given full scale voltage range.

W

Window triggering	A trigger generated by a signal passing outside of a selected voltage window. Two independent voltage levels determine the window. A negative slope triggers on the lower level and a positive slope triggers on the positive slope. Window triggering is useful for capturing noise glitches of unknown polarity.

APPENDIX B: EXAMPLE

6810 EXAMPLE PROGRAM

This example program was written for use with the LeCroy 8901A GPIB to CAMAC interface. When using the 8901A, the F,A,N commands must be converted to a sequence of decimal bytes before being sent across the GPIB to the 8901A. When using the 6010, only a single text string is sent (for example, "F9 A0 N8"). Therefore, programming for the 6010 is much easier.

Breakdown of Program Listing

Line no.

40–60	This code loads and initializes the National Instruments GPIB Driver. Note that the file "bib.m" must exist in the current directory for the program to run.
110	N% is used to store the 6810's CAMAC N slot number. This example uses slot 8 (i.e., the slot number pointed to by the "N" on the module's front panel.)
140–460	This block of code writes all of the 6810's setup parameters.
480–590	This code arms, triggers, and reads data from the 6810. The data is stored in the array ADATA% after reading.
600–610	After reading the data, F(25)A(1) is used to abort the readout. F(2)A(0) completes the abort sequence.
630–661	These lines display the acquired data in a graph form on the screen. To make this example program easier to follow, no grid lines, axis, or labels are drawn on the graph.
670–750	This code sends a CAMAC Function(F), Address (A), and Slot number (N) to the 6810 and returns its X and Q response. This would be used to issue control commands to the 6810, e.g.: arming the module or issuing a 'soft' trigger, etc.
760–870	This code sends a CAMAC Function (F), Address (A), Slot number (N), and 16 bits of data (W) to the 6810 and returns its X and Q response. This would be used to issue setup commands to the 6810, i.e. Setting its "full scale range" or "sampling period" etc.
880–970	This code sends a CAMAC Function (F), Address (A) and Slot number (N) to the 6810 and returns a 16 bit data word (W) along with the current X and Q status. This would be used to return values from the 6810, i.e. Querying the current "sampling period" or the "input offset" etc.
980–1050	These lines initialize the GPIB bus: the interface is cleared, remote enable is set, and the bus timeout is set for 3 seconds.
1060–1120	This section initializes the 8901A CAMAC crate controller. 8 bit read mode is enabled and a CAMAC Z (Initialize) is sent.
1130–1170	This code sends an F(9)A(1) to the 6810 to perform a reset.

1180–1240 This code verifies that all of the setup parameters are valid. The returned code contains one bit for each possible error in the setup. The meaning of each bit is given in the "Verify Setup" section of this manual.

1250–1320 The setup parameters are read back here and displayed on the screen.

1330–1370 This section sends an F(3)A(0) sequence and returns the 6810's module ID word. This will be "6810" if the module is at the GPIB address and CAMAC slot specified.

```
10 ' 6810 Users Manual Example Program:
20 '                                    Programming a 6810 using BASIC
25 '
30 'Load National Instruments GPIB Handler
40  CLEAR ,60000! : IBINIT1=60000! : IBINIT2=IBINIT1+3 : BLOAD
    "bib.m",IBINIT1
50  CALL IBINIT1(IBFIND,IBTRG,IBCLR,IBPCT,IBSIC,IBLOC,IBPPC,IBBNA,IBONL,
    IBRSC,IBSRE,IBRSV,IBPAD,IBSAD,IBIST,IBDMA,IBEOS,IBTMO,IBEOT,IBRDF,
    IBWRTF, IBTRAP)
60  CALL IBINIT2(IBGTS,IBCAC,IBWAIT,IBPOKE,IBWRT,IBWRTA,IBCMD,IBCMDA,IBRD,
    IBRDA,IBSTOP,IBRPP,IBRSP,IBDIAG,IBXTRC,IBRDI,IBWRTI,IBRDIA,IBWRTIA,
    IBSTA%, IBERR%,IBCNT%)
70 '
80  SCREEN 2:CLS:KEY OFF                ' Set up display
90 DIM ADATA%(1024)                     ' Data array
100 '
110 N%=8                                ' Slot no. = 8
120 GOSUB 980                           ' Initialize GPIB
130 GOSUB 1130                          ' Initialize TR6810
140 F%=16:A%=0 :W%=4   :GOSUB 760       ' Time stamp ( >16 months )
150 F%=16:A%=1 :W%=3   :GOSUB 760       ' Ch.1 Sensitivity ( 4v p-p )
160 F%=16:A%=2 :W%=0   :GOSUB 760       ' Ch.2 Sensitivity
170 F%=16:A%=3 :W%=0   :GOSUB 760       ' Ch.3 Sensitivity
180 F%=16:A%=4 :W%=0   :GOSUB 760       ' Ch.4 Sensitivity
190 F%=16:A%=5 :W%=0   :GOSUB 760       ' Block size for readout ( 1k )
200 F%=16:A%=6 :W%=0   :GOSUB 760       ' Offset for read ch.# lsb (0)
210 F%=16:A%=7 :W%=0   :GOSUB 760       ' Offset for read ch.# msb (0)
220 F%=16:A%=8 :W%=1   :GOSUB 760       ' Trig. holdoff enable ( enabled )
230 F%=16:A%=9 :W%=0   :GOSUB 760       ' Trigger slope ( +ve )
240 F%=16:A%=10:W%=0   :GOSUB 760       ' Trigger coupling ( DC )
250 F%=16:A%=11:W%=200:GOSUB 760        ' Trigger upper level
260 F%=16:A%=12:W%=0   :GOSUB 760       ' Trigger lower level
270 F%=16:A%=13:W%=3   :GOSUB 760       ' Trigger source ( CAMAC Only )
280 F%=16:A%=14:W%=54  :GOSUB 760       ' # post trig near samples lsb (300)
290 F%=16:A%=15:W%=0   :GOSUB 760       ' # post trig near samples msb
300 F%=17:A%=0 :W%=1   :GOSUB 760       ' # channels ( 1 )
310 F%=17:A%=1 :W%=128:GOSUB 760        ' Ch.1 offset ( Bipolar )
320 F%=17:A%=2 :W%=0   :GOSUB 760       ' Ch.2 offset
330 F%=17:A%=3 :W%=0   :GOSUB 760       ' Ch.3 offset
340 F%=17:A%=4 :W%=0   :GOSUB 760       ' Ch.4 offset
350 F%=17:A%=5 :W%=0   :GOSUB 760       ' Ch.1 Source & coupling ( + DC )
360 F%=17:A%=6 :W%=0   :GOSUB 760       ' Ch.2 Source & coupling
370 F%=17:A%=7 :W%=0   :GOSUB 760       ' Ch.3 Source & coupling
380 F%=17:A%=8 :W%=0   :GOSUB 760       ' Ch.4 Source & coupling
390 F%=17:A%=9 :W%=-2  :GOSUB 760       ' Trigger delay ( -2 )
400 F%=17:A%=10:W%=0   :GOSUB 760       ' No. of samples per segment ( 1k )
```

```
410 F%=17:A%=11:W%=1   :GOSUB 760      ' No. of segments lsb ( 1 )
420 F%=17:A%=12:W%=0   :GOSUB 760      ' No. of segments msb
430 F%=17:A%=13:W%=0   :GOSUB 760      ' Single clock mode
440 F%=17:A%=14:W%=16  :GOSUB 760      ' f1 sampling clock code ( 2MHz )
450 F%=17:A%=15:W%=0   :GOSUB 760      ' f2 sampling clock code
460 F%=19:A%=2 :W%=0   :GOSUB 760      ' Memory size code ( No checking )
470 '
480 ' Read back data
490     F%=26:A%=0:GOSUB 670                                    ' Enable lam
500     F%=10:A%=0:GOSUB 670                                    ' Clear lam
510     F%=9:A%=0:GOSUB 670                                     ' Arm
520     FOR R=1 TO 100:NEXT R                                   ' Delay
530     F%=25:A%=0:GOSUB 670                                    ' Manual trigger
540     FOR R=1 TO 100:NEXT R                                   ' Delay
550     F%=18:A%=1:W%=0:GOSUB 670                               ' Prepare to read seg.0
560     FOR R=1 TO 100:NEXT R                                   ' Delay
570     F%=2:A%=0:GOSUB 670                                     ' F(2),A(0) read data
580     WRT$=CHR$(106):CALL IBWRT(A8901%,WRT$)                  ' Set 16 bit read mode
590     CNT%=2048:CALL IBRDI(A8901%,ADATA%(0),CNT%)             ' Read 2k bytes
600     F%=25:A%=1:GOSUB 670                                    ' Abort read
610     F%=2:A%=0:GOSUB 670                                     ' Complete abortion
620 '
630 ' Display acquired data
640     A%=1:CNT%=1023
650     PSET (A%,(4096-(ADATA%(A%)))/20.48)
660     FOR X%=A% TO CNT% :LINE-(X%/2,(4096-ADATA%(X%))/20.48):NEXT X%
661     END
664 '
665 '              Start of subroutines
666 '
670 ' Subroutine : Send a CAMAC Command and execute a CAMAC cycle
680 '    Requires: F%,A%,N%       Returns: XQ%
690     WRT$=CHR$(97):CALL IBWRT(A8901%,WRT$)                   ' Set 8 bit read mode
700     WRT$=CHR$(65)+CHR$(95): CALL IBWRT(BD%,WRT$)            ' Execute CAMAC cycle
710     WRT$=CHR$(F%)+CHR$(A%)+CHR$(N%)                         ' Make command string
720     CALL IBWRT(A8901%,WRT$)                                 ' Write to 8901A
730     RD$=SPACE$(2):CALL IBRD(A8901%,RD$)                     ' Execute camac cycle
740     XQ%=ASC(RIGHT$(RD$,1))                                  ' Return CAMAC X and Q
750     RETURN
751 '
760 ' Subroutine : Send a CAMAC Command and write a 16 bit data word
770 '    Requires: F%,A%,N%,W%    Returns: XQ%
780     WRT$=CHR$(97):CALL IBWRT(A8901%,WRT$)                   ' Set 8 bit read mode
790     WRT$=CHR$(65)+CHR$(95): CALL IBWRT(BD%,WRT$)            ' Execute CAMAC cycle
800     IF W%<0 THEN W%=32768!+W%                               ' If data is negative
810     MSB%=W%/256:LSB%=W% MOD 256                             ' Split into 2 bytes
```

```
820       WRT$=CHR$(F%)+CHR$(A%)+CHR$(N%)+CHR$(LSB%)+CHR$(MSB%)
830       CALL IBWRT(A8901%,WRT$)                          ' Send command to 8901A
840       RD$=SPACE$(2):CALL IBRD(A8901%,RD$)              ' Execute a CAMAC cycle
850       XQ%=ASC(RIGHT$(RD$,1))                           ' Return X and Q
860       RETURN
870 '
880 ' Subroutine : Send a CAMAC Command and read a 16 bit data word
890 '     Requires: F%,A%,N%        Returns: XQ%,R%
900       WRT$=CHR$(98):CALL IBWRT(A8901%,WRT$)           ' Set 16 bit read mode
910       WRT$=CHR$(65)+CHR$(95): CALL IBWRT(BD%,WRT$)    ' Execute CAMAC cycle
920       WRT$=CHR$(F%)+CHR$(A%)+CHR$(N%)
930       CALL IBWRT(A8901%,WRT$)                          ' Send Command
940       RD$=SPACE$(3):CALL IBRD(A8901%,RD$)              ' Execute a CAMAC cycle
950       R%=ASC(LEFT$(RD$,1))+256*ASC(MID$(RD$,2,1))     ' Return data
960       XQ%=ASC(RIGHT$(RD$,1))                           ' Return X and Q
970       RETURN
971 '
980 ' Subroutine : Initialize GPIB
990 '     Open devices & return unit descriptors
1000      CNAME$="DEV1":CALL IBFIND(CNAME$,A8901%)  ' Assign unit descriptor
1010      CNAME$="GPIB0":CALL IBFIND(CNAME$,BD%)
1020      CALL IBSIC(BD%)                                  ' Send interface clear
1030      V%=1:CALL IBSRE(BD%,V%)                          ' Send remote enable
1040      V%=12:CALL IBTMO(A8901%,V%)                      ' Set timeout = 3 seconds
1050      RETURN
1055 '
1060 ' Subroutine : Initialise 8901A
1070 '
1080      WRT$=CHR$(97):CALL IBWRT(A8901%,WRT$)           ' Set 8 bit read mode
1090      WRT$=CHR$(65)+CHR$(95):CALL IBWRT(BD%,WRT$)     ' Execute CAMAC cycle
1100      WRT$=CHR$(33):CALL IBWRT(A8901%,WRT$)           ' Send a CAMAC Z
1110      WRT$=CHR$(65)+CHR$(95):CALL IBWRT(BD%,WRT$)     ' Execute CAMAC cycle
1120      RETURN
1125 '
1130 ' Subroutine : Reset TR6810
1135 '
1140 '
1150      F%=9:A%=1:GOSUB 670                              ' Reset 6810 [F(9),A(1)]
1160      FOR R=1 TO 100:NEXT R                            ' Wait for completion
1170      RETURN
1175 '
1180 ' Subroutine : Verify setup parameters
1190 '
1200      F%=18:A%=6:GOSUB 670                        ' Verify setup parameters
1210      FOR R=1 TO 100:NEXT R                       ' Wait for completion
1220      F%=2:A%=1:GOSUB 880                         ' Read result of verify
```

```
1230      PRINT " Result of verify = ";R%          ' Display result
1240      RETURN
1245 '
1250 ' Subroutine : Read back setup parameters
1260 '
1270        F%=18:A%=0:GOSUB 670                   ' Prepare to read setup
1280        FOR LP=0 TO 41
1290            F%=2:A%=1:GOSUB 880                ' Read parameter
1300            PRINT LP,R%                        ' Display parameter
1310        NEXT LP
1320        RETURN 1325 '
1330 ' Subroutine : Read module id
1340 '
1350        F%=3:A%=0:GOSUB 880                    ' Return module id
1360        PRINT "Module id = ";R%                ' Display id word
1370        RETURN
```

APPENDIX C: 6810 Driver Control

The following CAMAC commands are suggested for controlling the 6810 module.

SETUP:	F16	Ac	Wd	Channel 'c' sensitivity, choice 'd'
	F17	Ac	Wd	Channel 'c' offset, value 'd'
	F17	Ac+4	Wd	Channel 'c' source and coupling, choice 'd'
	F17	A0	Wd	Number of 'd' active channels
	F17	A10	Wd	Samples per segment, choice 'd'
	F17	A14	Wd	F1 sample clock, choice 'd'
	F16	A10	Wd	Trigger coupling, choice 'd'
	F16	A9	Wd	Trigger slope, choice 'd'
	F16	A13	Wd	Trigger Source, choice 'd'
	F16	A11	Wd	Trigger high level, value 'd'
	F16	A12	Wd	Trigger low level, value 'd'
	F17	A9	Wd	Trigger delay, value 'd'
	F16	A8	Wd	Trigger holdoff enable, choice 'd'
	F17	A13	Wd	Timebase mode, choice 'd'
	F17	A11	Wd	Low byte number of segments, value 'd'
	F17	A12	Wd	High byte number of segments, value 'd'
	F16	A0	Wd	Time Stamp resolution, choice 'd'
	F18	A6		Verify setup
	F11	A0		Wait for CAMAC lock out, Q=1 continue
	F2	A1		Read register, data = 0 setup OK
READY	F26	A0		Enable Lam
	F9	A0		ARM
TRIGGER:	F25	A0		Trigger
CLEAR:	F10	A0		Clear Lam
	F24	A0		Disable Lam
READ:	F18	A0		
	F2	A1		Read back 36 parameters
	F18	A11		
	F2	A1		Read Timestamp
	F16	A5	Wd	Block size for readout
	F16	A6	Wd	
	F16	A7	Wd	Offset in blocks for read
	F18	Ac	Wd	Prepare read channel 'c', segment 'd'
	F11	A0		Wait for CAMAC lock out, Q=1 continue
	F2	A0		Read block of data
	F25	A1		Abort, a MUST after read block!
	F2	A0		Must follow abort command

APPENDIX D: ASYST EXAMPLE

ASYST Example Using the 6920-DL to Control a 6810

Fast Disk Storage

Description: This example program should be typed into an ASCII text file (using the ASYST editor or any other available text editor) and compiled into the ASYST dictionary using the LOAD command. The example uses the Model 6920-DL drivers to acquire and read 512 ksamples from a 6810 waveform recorder. The data is transferred directly to a fixed disk after reading.

Notes: The command **CREATE.FILE** must be used to create an empty file on the disk before executing **STORE.DATA**.

This example requires that the **DATAFILE.SOV** overlay be loaded either transiently or permanently before running.

When using an 8901A crate controller and a NI PC3 GPIB Interface, the time to acquire 512K of data and transfer it to the hard disk can be as low as 9 seconds. Once the data is on the disk, use the **GRAPH.SUBFILE** command to display the data.

Hardware: LeCroy 6810 Waveform Recorder
LeCroy 8901A/6010 CAMAC controller

Listing:

```
DIM[ 4096 ] DMA.ARRAY DATA                          \ Create DMA array
: CREATE.FILE
    FILE.TEMPLATE                                   \ Define file template
    DATA []FORM.SUBFILE                             \ Subfile size = Array DATA size
    128 TIMES                                       \ 128 separate subfiles
    END                                             \ End of template
    FILE.CREATE C:6810.DTA                          \ Create data file
;
: STORE.DATA
    FILE.OPEN C:6810.DTA                            \ Open Data File
    CR ." Enter GPIB Controller type (6010/8901):"
    #INPUT                                          \ User input (Controller type)
    CASE
      6010 OF  1 6010 CAMAC.CRATE                   \ Use 6010 CAMAC controller
                      INIT.CAMAC
                      6010.ASYST.DEFAULTS
                      ENDOF
      8901  OF 1 8901 CAMAC.CRATE                   \ Use 8901A CAMAC controller
                      INIT.CAMAC
                      ENDOF
ENDCASE

8 CAMAC.SLOT                                        \ 6810 is in CAMAC slot 8
6810.DEFAULT.SETUP                                  \ Write default 6810 slot 8 6810.
DEFAULT.SETUP                                       \ Write default 6810
512 6810.SEG.SIZE                                   \ Define segment size = 512K
6810.ARM                                            \ Arm module
TRIG.WAIT                                           \ Wait for LAM
```

```
0 0 1 6810.ENABLE.READ                    \ Enable read mode on 6810
REL.TIME                                  \ Store start time
129 1 DO                                  \ Loop from 1 to 128
    DATA 6810.READ.DATA                   \ Read data into array DATA
    I SUBFILE                             \ Select subfile #I
    DATA ARRAY>FILE                       \ Transfer array to file
LOOP
 6810.DISABLE.READ                        \ Disable 6810 read mode
REL.TIME                                  \ Store finish time
FILE.CLOSE                                \ Close the data file
SWAP - . "Time taken = "                  \ Display time taken
;

: GRAPH.SUBFILE   \ [ subfile# - ]
\    This routine plots a graph of the time domain data in the given subfile
    FILE.OPEN C:6810.DTA                  \ Open data file
    SUBFILE                               \ Move to the given subfile
    UNNAMED.ARRAY                         \ Transfer the subfile data to the stack
    SUB[ 1 , 4096 , 4 ]                   \ Bin the data (only plot every 4th point)
    Y.AUTO.PLOT                           \ Plot the data
    FILE.CLOSE                            \ Close file
;
```

INDEX

INDEX

INDEX