technical information manual

CAMAC Model 8100

Dual Programmable Differential Amplifier

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy / CALIFORNIA
PALO ALTO, CALIFORNIA

TABLE OF CONTENTS

TECHNICAL DATA

LeCroy
CALIFORNIA

CAMAC Model 8100

Dual Programmable Differential Amplifier

- **Programmable input range**—from .1 volt–50 volt full scale
- **Good common mode rejection**—40 db at 100 KHz
- **Excellent frequency response**—DC to 1 MHz
- **Convenient cut-off filter**—200 KHz

The LeCroy Model 8100 Programmable Differential Amplifier is designed to provide signal conditioning and noise immunity for experiments where gain has to be optimized quickly and flexibly to extend the dynamic range of the following instrumentation. The gain of the amplifier is fully programmable by computer through international standard CAMAC interface. On the other hand, all settings can be made by hand to facilitate setup in the absence of a computer.

The single-ended outputs are designed to match the line of CAMAC transient recorders offered by LeCroy for research in fusion and other areas. The outputs can drive a high impedance to ±10 volt or a 50 ohm impedance to ±½ volt. The differential inputs are accommodated by a shielded 2 element LEMO connector and can operate in presence of a common signal of up to 100 volt. A switch selectable cut-off filter is available to limit the 1 MHz band width to 200 KHz in order to prevent aliasing when in use with the LeCroy Model 8210 or Model 2264 transient recorders (typical sampling rates of 1 MHz). The common mode rejection is 100 to 1 at 100 KHz on the 100 mV range, is better at lower frequencies and higher gain setting, and is worse at high frequencies and lower gains.

The Model 8100 is packaged in a number 1 width CAMAC module to permit front-panel, switch-selectable-gain knobs and is the first in an expanding line of signal conditioning circuits being designed for use with waveform digitizers in experiments studying transient phenomena.

Preliminary: January 1979

Instrumentation for the study of transient phenomena

LeCROY RESEARCH SYSTEMS OF CALIFORNIA • 1806 Embarcadero Rd. • Palo Alto, California 94303
TELEPHONE: (415) 856-1800 TWX: 910-373-1791

PRELIMINARY SPECIFICATION
CAMAC MODEL 8100
Dual Programmable Differential Amplifier

Input Characteristics

Type: Differential Amplifier, shielded 2 element LEMO connectors

Impedance: 1 M ohm, 30 pf

Input Ranges: 9 steps from 0.1 to 50V in a 1, 2, 5 sequence. Local settable by 2 three position switches for .1, 1, and 10 volts with a multiplier of 1, 2, and 5. Programmable by computer in the same steps. Each channel can be independently set.

Common Mode Range: ±5V on .1, .2, .5V ranges
±50V on 1, 2, 5V ranges
±100V on 10, 20, 50V ranges

Common Mode Rejection: 100: 1 at 100 KHz on .1V range. 60db at 60 Hz on 10V range

Input Protection: 200V for 10μsec on all scales

Frequency Response: DC to 500 KHz (1 db)

Anti aliasing filter: Switch selectable 2 pole butterworth filter with 200 KHz cutoff (3db point). Switch selects filters for both amplifiers at once; mpu interface can select filter on each amplifier separately.

OUTPUT CHARACTERISTICS

Maximum linear range: ±10V into high impedance (±.5V into 50Ω)

Output offset temperature coeff: 5mV/°C (1.0mV/°C optional at higher cost)

Output Impedance: 50Ω.

GENERAL

Gain: Settable for each channel in steps of .2 to 100 in a 1, 2, 5 sequence. See input range. Gains should be divided by 2 when driving 50Ω.

Input Offset Voltage: Computer settable by on-board DAC (offset binary code). Front Panel Toggle switch to set offset driving the DAC with up/down counter so that offset is readable and reproducible when switching from local to remote. DAC resolution is approx. 2.7 mV/Step referred to the output. DAC range is ±5.5V (12 binary bits).

CONTROL AND READOUT FUNCTION:

CAMAC Commands: Q: A Q=1 response is generated only in recognition of a F(1)•N or F(0)•N when a valid word is being read.
X: An X=1 (Command Accepted) response is generated when a valid F, N and A are generated.

CAMAC Code: F(0)•A(0) reads channel 1 gain.
F(16)•A(0) sets channel 1 gain at S2.
F(1)•A(0) reads channel 1 offset.
F(17)•A(0) sets channel 1 offset at S2.
F(0)•A(1) reads channel 2 gain.
F(16)•A(1) sets channel 2 gain at S2.
F(1)•A(1) reads channel 2 offset.
F(17)•A(1) sets channel 2 offset at S2.

The A1-A8 lines are used to address the desired amplifier circuit. A(0) addresses amplifier #1 (upper amplifier), A(1) addresses amplifier #2 (lower amplifier).

F(0) reads gain and status information on the addressed amplifier. Status can be read whether or not the unit is in remote mode. Gain status is read on bits 1–6; bit 7 indicates status of amplifier ground setting, bit 8 indicates status of filter switch. When amplifier 1 is addressed, bit 9 indicates status of remote/local switch.

F(16) sets gain of the addressed amplifier. Bits 1–6 set amplifier gain, bit 7 can ground inputs, bit 8 switches the filter in or out.

F(1) reads the setting of the offset DAC on the addressed amplifier. Setting is offset binary, and data appears on the R1–R12 lines, with R1 the LSB and R12 the MSB. DAC setting can be read whether or not the unit is in remote mode.

F(17) sets the offset DAC on the addressed amplifier. Offset data is accepted on lines W1–W12, with W1 the LSB and W12 the MSB. DAC Polarity: Programming all (1)'s into the offset DAC register will offset the amplifier's output by the maximum negative amount (approximately −5.5V), assuming no input signal.

Packaging: In conformance with the CAMAC standard for nuclear modules (USAEC Reports TID-25875, IEE St. #583, ESONE Report 4100e) in an RF shielded #1 CAMAC package.

Current Requirements: +6V, 420mA; −6V, 20 mA; +24V, 140mA; −24V, 130mA.

THE CAMAC MODEL 8100

Switch selects the source of the Control Commands for both Amplifiers. With the switch in "LOCAL" position, the Front panel switches control Amplifier functions; with the switch in "REMOTE" position, the Front panel controls are desabled and the CAMAC Interface provides the control.

Switched to the "IN" position, this switch causes a 200 KHZ, 2 pole Butterworth filters to be switched in line with both Amplifiers.

This switch selects Amplifier GRIMS of 1, 10, or 100 for Amplifier #1.

This switch selects a Multiplier of 1, .5, or .2, which is applied to the Gain switch setting of Amplifier 1 to determine the overall Gain of the Amplifier.

This switch allows the Dial which controls the Offset to be counted up or down. Pressing the switch in the "-" direction causes the Amplifier to become more negative.

AMPLIFIER #1
Differential Input-1 MEG OHM input impedance.

AMPLIFIER #1 OUTPUT
Impedance 50 Ohms.

AMPLIFIER #2 GAIN SWITCH
Same as Amplifier #1.

AMPLIFIER #2 MULTIPLIER SWITCH.
Same as Amplifier #1.

AMPLIFIER #2 OFFSET SWITCH. Same as Amplif. #1.

AMPLIFIER #2 DIFFERENTIAL INPUT. 1 MEG Ohm Input Impedance.

AMPLIFIER #2 OUTPUT. Impedance 50 Ohms.

OPERATIONAL DESCRIPTION

GENERAL: The LeCroy 8100 dual programmable amplifier contains 2 separate precision differential-input amplifiers with gains adjustable in a 1-2-5 sequence from .2 to 100, with a differential input from 50 volts to 100 millivolts, respectively, and a 500 khz 1-db bandwidth at all settings. Both amplifiers exhibit excellent common-mode rejection and offer a wide common-mode input range. Gain is settable either by front panel switches or via CAMAC commands.

Each amplifier contains a switchable 200 khz, 2-pole Butterworth filter. A 12-bit D/A converter on each amplifier provides offset control with a range at the output of ±5.5 volts. The filters can be switched in or out together via a front panel switch, or can be independently switched by CAMAC commands. Complete status of the amplifier can be read at any time by the CAMAC interface.

FRONT PANEL INPUTS, CONTROLS AND OUTPUTS

ANALOG INPUTS: Two differential Lemo connectors, one for each amplifier. Impedance at each input is 1 megohm to ground.

ANALOG OUTPUTS: Two single Lemo connectors, one for each amplifier. Output impedance is 50 ohms. Output range into 1 kohm: ± 10 volts; into 50 ohms: ± 2 volts max. Outputs will survive at least 5 seconds

of short circuit to ground.

REMOTE/LOCAL SWITCH: When this switch is in the Local position, the front panel switches control the amplifier characteristics; however, the CAMAC interface can still read the amplifier status.

When the switch is in the Remote position, all other front panel switches are disabled, and the amplifier charactersitics can be both set and read by CAMAC command. When the switch is changed from Local to Remote, however, all amplifier conditions that exist at the time are retained until the CAMAC interface commands a change, i.e. the amplifiers do not go into an undefined state.

When the switch is changed from Remote to Local, however, the amplifier characteristics revert to that which is indicated by the fromt panel switch positions, with the exception of the D/A setting, which remains as it was at the time of the change. If any amplifier inputs have been grounded by CAMAC command, they will be ungrounded when the switch is changed from Remote to Local.

FILTER SWITCH: When this switch is in the In position, a 200 khz (3db point) filter is switched in line with each amplifier. With the switch in the Out position, each amplifier reverts to its 500khz 1-db bandwidth.

GAIN AND MULTIPLIER SWITCHES: Each amplifier's gain is set by the combination of the Gain and Multiplier switches. The position of the Gain switch is multiplied by the setting of the Multiplier switch, e.g. if the Gain switch for amplifier 1 is set at 100, and amplifier

1's multiplier switch is set to .2, then the amplifier's overall gain is 20.

OFFSET SWITCHES: The offset switches each control a counter connected to the offset DAC in the amplifier associated with the switch. The switches are spring loaded to return to a center position. Pushing the switch momentarily to the left causes one count to be entered into the counter, such that the associated amplifer's output becomes approximately 2.7 mv more negative. A momentary push to the right causes the amplifier's output to become more positive by the same amount. If the switch is held either to the left or the right for more than 1 second, a continuous clock is switched into the negative or positive, respectively, until the switch is released. The speed of increase or decrease is such that the entire range of the DAC is traversed in approximately ____ seconds. If the lower or upper limit of the DAC is reached and passed while the switch is held in one of the active positions, the offset will simply switch to the opposite extreme and continue counting in the same direction until the switch is released.

CAMAC INTERFACE

In the following discussions, CAMAC nomenclature will be used, i.e. a "one" is defined as a TTL low level on the back connector.

TO SET AMPLIFIER OFFSET:

Amplifier #1: (Upper Amplifier) N.F(1-).A(0)(S2.W1--W12)

Amplifier #2: (Lower Amplifier) N.F(17).A(1)(S2.W1--W12)

Data is accepted on write lines W1--W12; the DAC is offset binary coded using W1 as the LSB and W12 as the MSB. Behavior of the amplifiers to different DAC settings is shown in the examples below:

	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12
1. Amplifier offset maximum negative, (amplifier output offset approximately 5.5 volts):	1	1	1	1	1	1	1	1	1	1	1	1
2. Amplifier offset maximum positive, (amplifier output offset approximately +5.5 volts:	0	0	0	0	0	0	0	0	0	0	0	0
3. Amplifier offset near midrange:	0	0	0	0	0	0	0	0	0	0	0	0

TO SET AMPLIFIER GAIN, TO GROUND INPUTS, OR TO SWITCH FILTER:

Amplifier #1 (Upper Amplifier): N.F(16).A(0).S2.(W1-W8)

Amplifier #2 (Lower Amplifier): N.F(16).A(1).S2.(W1-W8)

Write line/Switch position equivalents:

	GAIN			MULT.			GND.	FILTER
	100	10	1	1	.5	.2		
Examples:	W1	W2	W3	W4	W5	W6	W7	W8
1.) Gain = 100, no filter ungrounded....	1	0	0	1	0	0	0	0
2.) Gain = 5, no filter, ungrounded.....	0	1	0	0	1	0	0	0
3.) Gain = .2, no filter, ungrounded....	0	0	1	0	0	1	0	0
4.) Gain = 20, filtered, ungrounded.....	1	0	0	0	1	0	0	1
5.) Inputs grounded.....	0	0	0	1	0	0	1	X
	1	2	4	1	2	4		

Note that when the inputs are grounded, none of the lines in the gain group (W1-W3) are asserted. This effectively disconnects the amplifier from the input connector, so that the grounding switch is not working against any signal that may be connected there. Signals at the input connector in this situation will still see a 1 megohm inpedance to ground. It should also be noted that, when the inputs are grounded, one line of the Multiplier group should be asserted. If this is not done, the amplifier output will saturate.

Note also that in none of the examples is more than one line in the Gain group (W1-W3) or the Multiplier group (W4-W6) asserted. Doing so will not cause any damage to the amplifier, but will result in improper gain settings, changes in input impedance, or nonlinearity in response.

TO READ AMPLIFIER OFFSET

Amplifier #1 (Upper Amplifier): N.F(1).A(0).(R1-R2)

Amplifier #2 (Lower Amplifier): N.F(1).A(1).(R1-R12)

Data on the R lines has the same polarity and logic as is used to set the offset on the W lines.

TO READ AMPLIFIER GAIN, FILTER, GROUNDING, AND CAMAC ACCESS STATUS

Amplifier #1 (Upper Amplifier): N.F(0).A(0).(R1-R9)

Data on the R lines (R1-R8) has the same polarity and logic as is used

to set the gain, filter, and grounding on the W lines. R9 is used (when reading amplifier #1 status only) to indicate status of the Local/Remote switch: it is 1 if the unit is in Local mode.

Amplifier #2 (Lower Amplifier): N.F(0).A(1).(R1-R8)

Data on the R lines has the same polarity and logic as is used to set the gain, filter, and grounding on the W lines.

FUNCTIONAL DESCRIPTION

GENERAL: The amplifier used in the 8100 is made up of two separate stages in cascade, each with a gain of 10 and each preceded by a switched attenuator. The input attenuator provides division ratios of 1, 10, and 100, and is controlled by the Gain switch. It is followed by the first gain stage, which accepts differential inputs and provides a single-ended output to the second attenuator. This attenuator provides division ratios of 1, 0.5, and 0.2, and is controlled by the Multiplier switch. The output of the second attenuator drives either the second gain stage input, or the input of the 200 khz filter, if the filter is switched in. The filter is a unity-gain active type, and its output drives the input of the second gain stage if the filter is switched in. The second gain stage includes a power output stage to allow driving 50-ohm loads. This stage is also the point where the offset is injected. The offset voltage is generated by a 12-bit monolitic D/A converter using offset binary code. The 8100 contains two identical channels of the amplifier described above, plus control and CAMAC interface logic.

In the following description only the #1 amplifier will be described, plus any circuitry that is common to both. The channel #2 amplifier is identical to the channel #1 amplifier. In the above and following discussions, refer as necessary to the Amplifier Block Diagram, Fig. 1, the Amplifier Logic Block Diagram, Fig. 2, and the schematic

diagrams in the back of this manual.

INPUT ATTENUATORS: The input attenuators for the 8100 are capacitor-compensated to allow good square wave response while maintaining 1 megohm impedance. The non-inverting input attenuator is composed of resistors R77-R80 and capacitors C8, and C28-C32. R77, CR22, and CR23 form a voltage limiting network to protect the amplifier input against overvoltage. C32 compensates for the loss of the amplifier's input capacitance when the attenuator is switched into the +100 position. A relay is used in the +1 position to achieve greater common mode voltage range for the +10 and +100 postions.

The inverting input attenuator is essentially the same as the non-inverting attenuator, with the exception of R83 and R85, which are added to allow adjustment of DC common-mode rejection ratio in the +10 and +100 positions.

ICs 4I and 4H translate the TTL drive signals into appropriate voltages to drive the FET switches. Q27 provides power gain to drive the relay coils for K3 and K4.

FIRST AMPLIFIER STAGE: The first amplifier stage has a gain of 10, and is used both as an impedance converter and as a differential-to-single-ended converter. A block diagram of the type of circuit used is shown in Fig. 3. Q15 is a matched pair of junction FETs and is used as a defferential input stage, to present a very high inpedance load to the preceding 1 megohm input attenuator. Q19 is another matched pair of transistors which functions as a low drift differential -to-

single-ended converter and principal gain stage. Q17 and Q18, together with amplifier 1H, form a very low drift, high output impedance current source for the emitters of Q19. CR45 prevents output saturation in amplifier 1H. Q16 is another matched pair that acts as a current source bias for Q15 and provides a feedback path for the overall amplifier via divider R96 & R97. Gain of the stage is determined by a combination of R96, R97, R94, and R91, but can be altered easily by changing R91 alone. CR26 & CR27, in addition to CR29-32, limit voltage swings to allow quick recovery from overdrives.

INTERSTAGE ATTENUATOR: The interstage attenuator is an uncompensated resistive attenuator formed by R98-100. Switching is accomplished by 3 of the 4 MOSFETs in 3H.

200KHZ FILTER: The 200 KHZ Filter is an active 2-pole lowpass filter of the Sallen and Key single-amplifier type, with poles placed to acheive a Butterworth (maximally flat gain) response. Amplifier 1F is the active element, with R131, R132, C40, and C41 determining the rolloff point. Amplifier 2F serves as a unity-gain buffer to isolate the filter from the interstage attenuator. Filter switching is done with MOSFETs. An additional MOSFET grounds the filter when it is not in use to minimize noise pickup.

SECOND AMPLIFIER STAGE: The second amplifier stage also has a gain of 10. Q20 is a matched pair of junction FETs and is used as an input stage here to provide a high inpedance load for the interstage attenuator output. It is biased by a current source formed by Q28 and

amplifier 2E. Q23 is the primary voltage gain stage, and is biased by a current source formed by Q21, Q22, and amplifier 1E, with CR46 preventing output saturation of 1E. Q23 drives a power stage whose primary elements are Q25 and Q26. R112 allows adjustment of bias current in Q25 and Q26 by altering the voltage drop across Q24, which also helps temperature compensate that bias current. R115, R121, and R122 determine the closed-loop gain of the stage, with R122 also providing the summing point for the voltage generated by the offset D/A converter (4E). CR33-36, CR41, and CR42 limit voltage swings to improve overdrive recovery. CR37-40, R118, and R119 form a network that limits current in the power stage to protect against short circuits and overloads on the output. R138 sets the output impedance of the amplifier.

DIGITAL CONTROL AND CAMAC INTERFACE: CAMAC read and write lines are buffered near the back connector by tri-state buffers 4B, 4D, 7B, and 7D and are combined on a single 12-line read-write bus that services all the digital control circuitry for the unit. This was done partly to reduce trace crowding on the board, but the primary purpose is to keep CAMAC signals near the back of the board when the unit is not addressed in order to reduce interference in the amplifier circuits themselves. Control of the offset D/A converters is provided via two 12-bit, resettable up-down binary counters, formed by 5A, 5C, and 5E for amplifier #1, and 6A, 6C, and 6E for amplifier #2. Count switch decoding is provided by 6F-3, 6F-8 and 5F-8. One-shot 5H-2 debounces the count switches, 5H-10 outputs the single clock pulses and triggers timer 6G,

which provides the 1-second delay before the continuous clock (R1, C1, and 5F-11) is enabled. It should be noted that the clocking circuitry is common to both counters; thus only one count switch should be operated at one time, or extra counts may result.

The counters also serve as latches to hold data from the CAMAC W lines when the offset is controlled via the interface. Data from the internal bus is connected to the counters' preset data lines, and is strobed into the counters in response to commands on the $\overline{\text{Load}}$ inputs via 1C-3 (amplifier #1) and 1C-6 (amplifier #2). Data in the counters is read back onto the internal bus by tri-state buffers 5B and 5D (amplifier #1) and 6B and 6D (amplifier #2).

The state of the amplifiers' gain, filters, and grounding is determined by the data stored in latches 2A and 3C (amplifier #1) and 8C and 9A (amplifier #2), which retain data that is output by data selectors 3A-4C and 8A-7C respectively. The selectors choose either the outputs of the switches or the internal data bus as inputs, depending on the state of the Remote/Local switch, which is debounced by flip-flop 5B-5. In Local mode, the latches follow their inputs because 1C-8 and 1C-11 are held high; in Remote mode, however, S2 and the appropriate address and function codes must appear via 1A-10 or 1A-13. Data in these latches is read back onto the internal data bus via tri-state buffers 4D, 7A, and 8D.

CAMAC commands are decoded by 2B and 3B. Write lines or Read lines are enabled by 4B-6 through 8B-4 or 4B-8 through 8B-1, respectively.

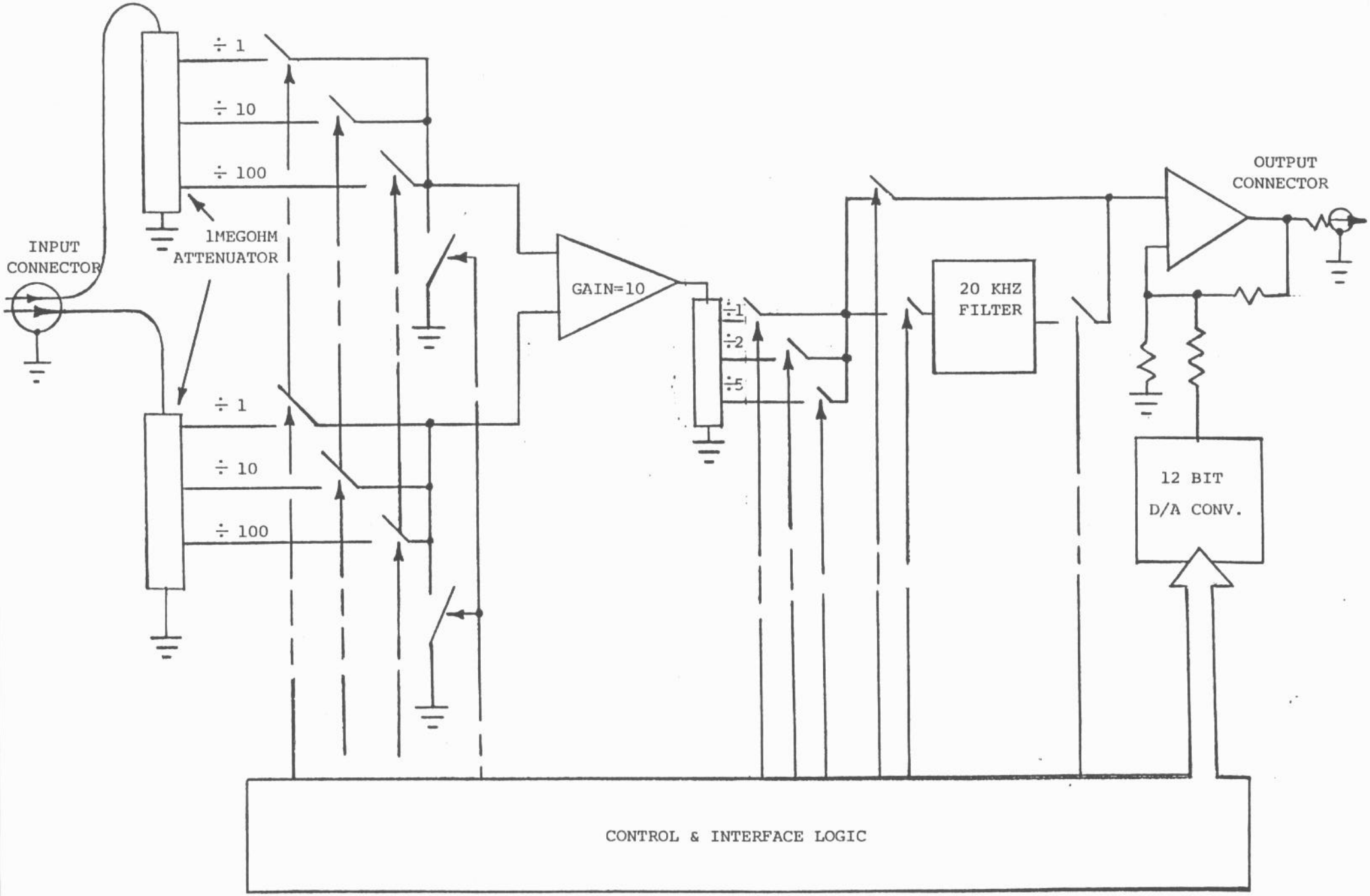


FIG. 1

AMPLIFIER BLOCK DIAGRAM (ONLY 1 CHANNEL SHOWN)

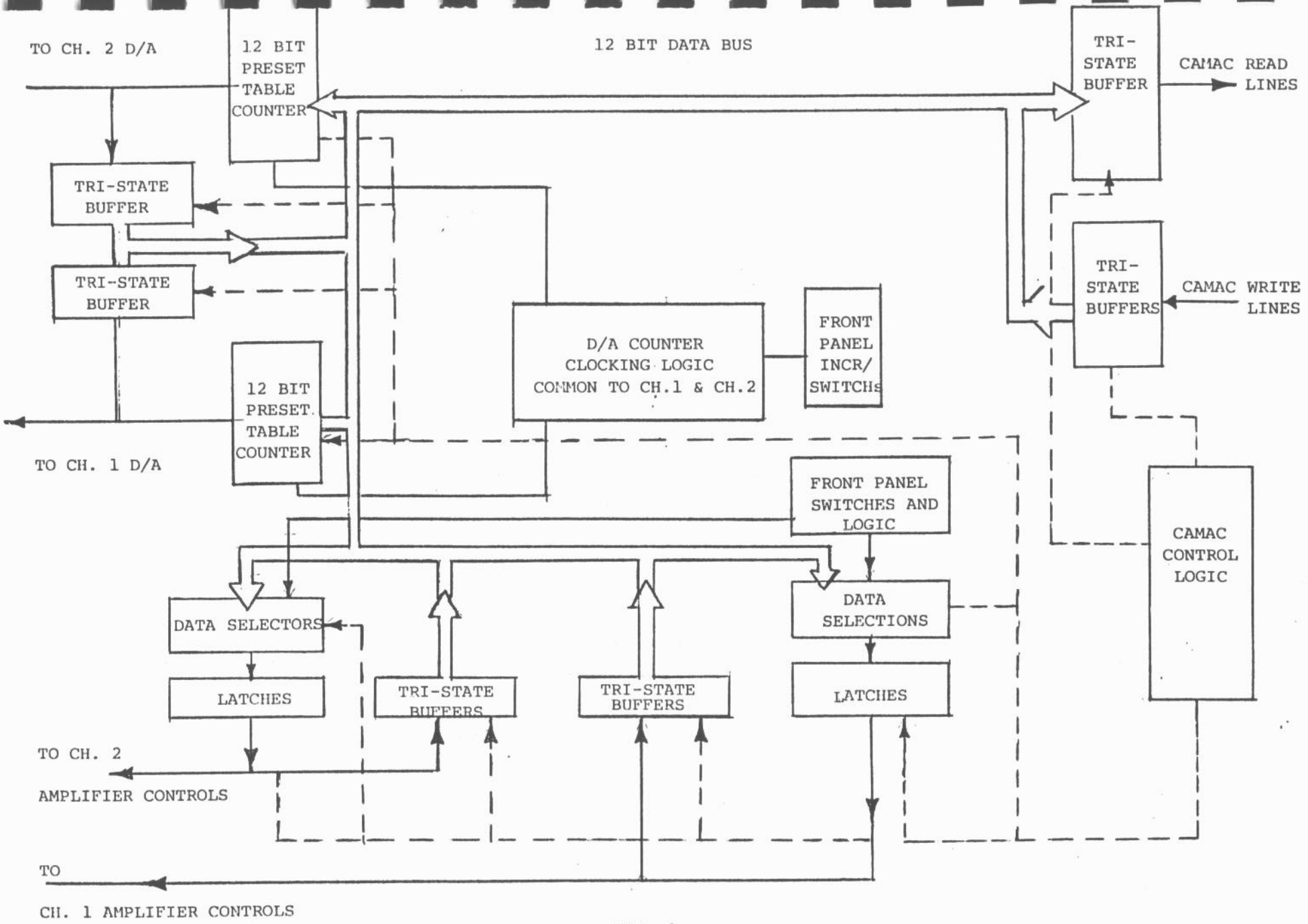


FIG. 2

8100 AMPLIFIER LOGIC BLOCK DIAGRAM

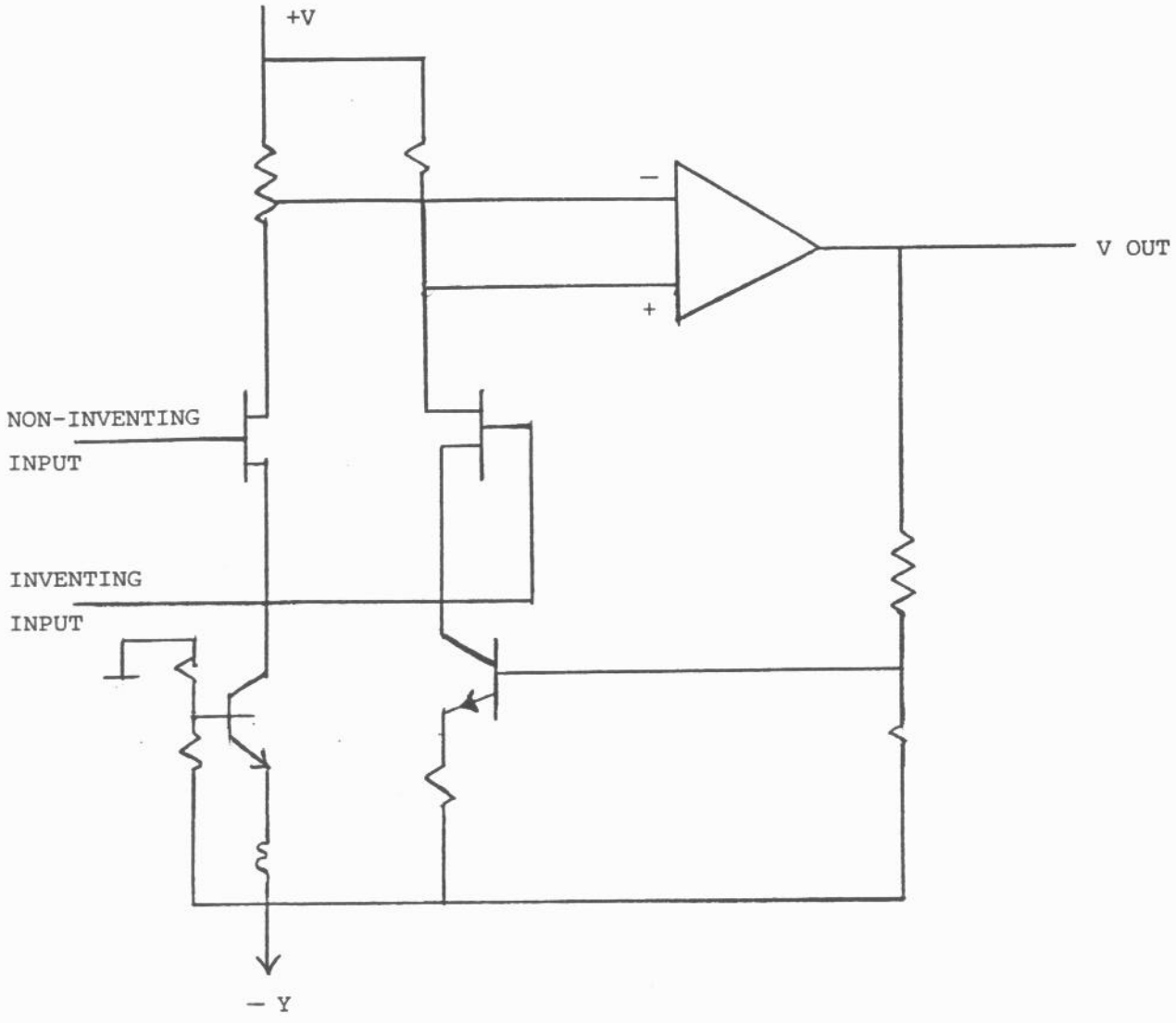


FIG. 3

FIRST AMPLIFIER STAGE BLOCK DIAGRAM

ECO NO.	DATE	PRIORITY	DESCRIPTION
1001			NOT USED
1002	6/28/79		CORRECT LAYOUT ERRORS ON "B" REV. AND PARTS LIST CHANGES
1003	9/4/79		REF. DESIGNATION CHANGES AND PARTS LIST
1004	9/18/79		PCB SILKSCREEN AND ARTWORK CHGS., ASSY DWG, PARTS LIST AND SCHEMATIC CHANGES
1005	9/27/79		RESISTOR CHANGE, ASSY DWG CHANGE TO IMPROVE AMPLIFIER GAIN AND PARTS LIST CHANGE

Remarks: On Priorities
1-Recall, field retrofit
2-Rework shippable units
3-Rework units in fabrication, assembly or test
4-Improvements for future MO's

LeCroy RESEARCH SYSTEMS

DRAWN

CHECKED

DATE

ENGINEERING CHANGE ORDERS

MODEL: 8100

DRAWING NUMBER:

technical
information

BASIC
CAMAC DATAWAY
OPERATING INFORMATION

Condensed from:

Document EUR 4100e

Published by the:

Esone Committee
of the
Joint Nuclear Research Center
Ispra Establishment -- Italy
March 1969

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.

INTRODUCTION

CAMAC is an international standard of modularized electronics as defined by the ESONE Committee of the JNRC, Ispra. Its function is to provide a scheme to allow a wide range of modular instruments to be interfaced to a standardized multi-receptacle which, in turn, may be interfaced to a computer. In this way, additions to a data transfer and control system may be made by plugging-in additional modules and making suitable software changes. Thus, CAMAC allows information to be transfered into and out of the instrument modules.

CAMAC modules may be plugged into a CAMAC Crate which has 25 Stations, numbered 1 through 25. Station 25, the rightmost station, is reserved for a Crate Controller, whereas Stations 1 - 24 are Normal Stations used for CAMAC Modules. Usually, Station 24 is also used by the controller in that most controllers are double width (#2 CAMAC). The purpose of the controller is to issue CAMAC Commands to the modules and transfer information between a computer (or other digital device) and the CAMAC modules.

Data transfer, control functions, and module powering is affected via the Dataway. This is a series of bus and individual lines across the back of the crate. The dataway lines include digital data transfer lines, strobe signal lines, and addressing lines and control lines. See Page 18C for a pin allocation chart.

In a typical dataway operation, the crate controller issues a CAMAC Command which includes specifying a station number (N), a subaddress (A), and function code (F) (see Page 17C). In response, the subaddress of the module will generate valid command accepted (X response) and act on the command. If this command requires data transfer, the read (R) or write (W) lines will be used. Note that the terms Read and Write apply to the controller, not the module. For example, under a read command, the controller reads data contained within a module.

USE OF THE DATAWAY LINES

Communication with plug-in units takes place through the Dataway. This passive multi-wire highway is incorporated in the crate and links the 86-pin sockets to all stations. The bus-lines link corresponding pins at all normal stations and, in some cases, the control station. Individual lines link one pin at a normal station to one pin at the control station. The patch pins have no specified Dataway wiring but can be connected to individual points to which patch leads may be attached.

During a Dataway operation the controller generates a command consisting of signals on individual Station Number lines to specify one or more modules, signals on the Subaddress bus-lines to specify a sub-section of the module or modules, and signals on the Function bus-lines to specify the operation to be performed. The command signals are accompanied by a signal on the Busy bus-line, which is available at all stations to indicate that a Dataway operation is in progress.

When a module recognizes a Read command, calling for a data transfer to the controller, it establishes data signals on the Read bus-lines. When a controller recognizes a Write command calling for a data transfer to a module, it establishes data signals on the Write bus lines. In addition, regardless of whether there is transfer on the R or W lines, the module may transmit one bit of status information on the Response bus-line.

Two timing signals, Strobes S1 and S2, are then generated in sequence on separate bus-lines. The strobes are used to transfer data from the Dataway into modules (on Write commands) and into the controller (on Read commands). They may also initiate other actions within the controller and modules.

Whenever there is no Dataway operation in progress (indicated by the absence of the Busy signal) any module may generate a signal on its individual Look-at-Me line to indicate that is requires attention. Three common controll signals are available at all stations, without requiring addressing by a command, in order to Initialize all units (typically after switch-on), to Clear data registers, and to Inhibit features such as data-taking.

DEFINITION OF COMMANDS

A command consists of signals on the Dataway lines which specify at least one module (by individual station number lines), a sub-section of the module or modules (by the four sub-address bus-lines), and the function to be performed (by the five function bus-lines). The command signals are maintained for the full duration of the operation on the Dataway. They are accompanied by a signal on the Busy bus-line which indicates to all units that a Dataway operation is in progress.

Station Number (N)

Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station. The stations are numbered in decimal code from the left-hand end as viewed from the front, beginning with Station 1.

Sub-Address (A8, A4, A2, A1)

Different sections of a module are addressed by signals on the four A bus-lines. These signals are decoded in the module to select one of up to sixteen sub-addresses, numbered in decimal from 0 to 15.

Function (F16, F8, F4, F2, F1)

The function to be performed at the specified sub-address in the selected module or modules is defined by the signals on the five F bus-lines. These signals are decoded in the module to select one of up to 32 functions, numbered in decimal from 0 to 31. The definitions of the 32 function codes are summarized in the Dataway Command Operations section.

Strobe Signals (S1 and S2)

Two strobe signals S1 and S2 are generated in sequence on separate bus-lines. These signals are used to transfer information between plug-in units via the Dataway or to initiate operations within units. In either case the specific action is determined by the command present on the Dataway. Both strobes are generated during each Dataway command operation, and all plug-in units which accept information from the Dataway do so in response to these strobes. The first strobe S1 is used for actions which do not change the state of signals on the Dataway lines. All units which accept data from the Dataway in a Read operation, or in a Write operation do so in response to S1. The second strobe S2 is used to initiate any actions which may change the state of Dataway signals, for example, clearing a register whose output is connected to the Dataway.

DATA

A common parallel highway is used for all transfers. All information carried by the parallel highway is conveniently described as data, although it may be information concerned with status or control features in modules. Up to 24 bits may be transferred in parallel between the controller and the selected module. Independent lines (Read and Write) are provided for the two directions of transfer.

The Write Lines (W1-W24)

The controller or other common data source generates data signals on the W bus-lines at the beginning of any 'Write' operation. The W signals reach a steady state before S1, and are maintained until the end of the operation, unless modified by S2.

The Read Lines (R1-R24)

Data signals are set up on the R bus-lines by the module as soon as a "Read" command is recognized. The R signals reach a steady state before S1, and are maintained for the full duration of the Dataway operation, unless the state of the data source is changed by S2. The controller or other common data receiver strobes the data from the R bus-lines at the time of the Strobe S1.

STATUS INFORMATION

Status information is conveyed by signals on the Look-at-Me (L), Busy (B), and Response (Q) lines.

Look-at-Me (L)

This, like the N line, is an individual connection from each station to a separate pin at the control station. When there is no Dataway operation in progress (no B present) any plug-in unit may generate a signal on its L line to indicate that it requires attention. When B is present each L signal is gated off the Dataway line by the unit which generates it.

A Look-at-Me request can be reset by Clear Look-at-Me, Initialize, or by the performance of the specific action which generated the request.

Dataway Busy (B)

The Busy signal is used to interlock various aspects of a system which can compete for the use of the Dataway. Specifically, it is generated during Dataway command or common control operations. Whenever N is present, B is present, and for the duration of B, all L signals are gated off the Dataway lines.

Response (Q)

The Q bus-line is used during a Dataway operation to transmit a signal indicating the status of a selected feature of the module.

On all Read and Write commands the signal on the Q bus-line remains static from the time the command is received until S2. For all other commands the signal on the Q bus-line may change at any time.

COMMON CONTROLS

Common control signals operate on all modules connected to them, without requiring to be addressed by a command. In order to provide protection against spurious signals the Initialize (Z) and Clear (C) signals must be accompanied by Strobe S2.

Initialize (Z)

The Initialize signal has obsolute priority over all other signals or controls. It sets all units to a basic state by resetting all resetting all registers, whether data or control, to a defined state, and by resetting all L signals and disabling them where possible. Units which generate must also cause S2 and B to be generated. Modules which accept Z gate it with S2 as a protection against spurious signals on the Z line.

Inhibit (I)

The presence of this signal inhibits any activity (for example, data taking). It must either not change when B is present or have rise and fall times not less than 200 ns.

Clear (C)

This common signal clears all registers or bistables connected to it. Units which generate C must also cause S2 and 3 to be generated. Modules which accept C gate it with S2 as a protection against spurious signals on the C line.

PRIVATE WIRING

Patch Leads (P1-P7)

Five pins (P1 to P5) on the 86-way socket at normal stations are not prewired to Dataway lines but are freely available for local connections. At the control station seven pins (P1-P7) are available. Signals on the patch pins must either remain static when B is present or have rise and fall times not less than 20 ns.

DATAWAY COMMAND OPERATIONS

A command is composed of signals on the Station Number line or lines, the Sub-Address lines and the Function lines. It is accompanied by a signal on the Busy Line. In response to a command, data may be transferred on the Read or Write lines and one bit of status information on the Q line. The two Strobes S1 and S2 must be generated in each Dataway command operation and control its timing.

The order in which the commands are described below corresponds to the function codes set out in Table 2. In this table the term 'register' is used for an addressable data source or receiver, without implying that it has a data storage property. The function codes allow the registers in a module to be divided into two distinct sets, known as Group 1 and Group 2. Thus it is possible to operate on more than the basic set of 16 registers selected by the 4 sub-address lines.

A common feature of all commands is that if the module has a Look-at-Me source which requests a specific command then the performance of that command should be reset the Look-at-Me source.

Read Commands (Function Codes 0-7)

Read commands are identified by the combination F16 = 0, F8 = 0 in the function code. They specify that information is to be transferred from a module to a controller via the R bus-lines. Data signals are set up on the R bus-lines by the module as soon as the 'Read' command is recognized, and the appropriate status signal connected to the Q bus-line. The R and Q signals reach a steady state before S1, and are maintained for the full duration of the Dataway command operation unless the state of the signal source is changed at S2. The controller or other common data receiver strobes the data from the R and Q bus lines at the time of the strobe S1.

In order to facilitate reading by sequential addressing, all registers containing data (as opposed to control information) must have cosecutive sub-addresses starting at sub-address 0. At each of these sub-addresses the module generates Q = 1 in response to the appropriate Read command. At the next sub-address in sequence (where there is not a data register) the response is Q = 0. At all remaining sub-addresses the Q signal may be used to test any feature, subject to the general requirement that the Q signal must be static from the beginning of command until at least S2.

Code 0, Read Group 1 Register

This command selects, by sub-address, one register from the first group in the module and transfers the contents of this register to the controller. The contents of the register remain unchanged.

Code 1, Read Group 2 Register

Same as Code 0, except command selects register from the second group.

Code 2, Read and Clear Group 1 Register

Same as Code 0, except the module register is cleared at time S2.

Code 3, Read Complement of Group 1 Register

Same as Code 0, except command transfers the complement of the contents of this register to the controller.

Code 4 - 7

Unassigned at this time.

CONTROL COMMANDS (Function Codes 8 - 15)

Control commands are identified generally by F8 = 1 in the function code. They are divided into two groups by the state of F16, in this case F16 = 0. They specify that information is not transferred on either the R or W bus-lines. However, information may be conveyed on the Q bus-line in any of these commands. The signal on the Q bus-line may change at any time but is strobed into the controller at time S1 and may (except in Code 8) be reset by strobe 2.

Code 8, Test Look-at-Me

This command selects a Look-at-Me source in the module and presents the state of this source on the Q bus-line.

Code 9, Clear Group 1 Register

This command selects, by sub-address, a register from the first group in the module and clears the contents of this register.

Code 10, Clear Look-at-Me

Same as Code 8, except the Look-at-Me source is cleared at time S2.

Code 11, Clear Group 2 Register

Same as Code 9, except command selects register from the second group.

Code 12-15

Unassigned at this time.

WRITE COMMANDS (Function Codes 16-23)

Write commands are identified by the combination F16 = 1, F8 = 0 in the function code. They specify that information is to be transferred from a controller to a module via the W bus-lines. The controller or other common data source generates data signals on the W bus-lines at the beginning of the "Write" operation. The module connects the appropriate status signal to the Q bus-line as soon as the command is recognized. The W and Q signals reach a steady state before S1 and are maintained for the full duration of the Dataway command operation unless the status of the signal source is changed at Strobe 2. In order to facilitate writing into registers by sequential addressing, all registers which are to contain data (as opposed to control information) have consecutive sub-addresses starting at sub-address 0. At each of these sub-addresses the module generates Q = 1 in response to the appropriate Write function. At the next sub-address in sequence (where there is not a data register) the response is Q = 0. At all remaining sub-addresses the Q signal may be used to test any feature subject to the general requirement that the Q signal must be static from the beginning of the command until at least S2.

Code 16, Overwrite Group 1 Register

This command selects, by sub-address, one register in the first group in the module and sets the contents of this register to correspond with the data generated on the W bus-lines by the controller.

Code 17, Overwrite Group 2 Register

Same as Code 16, except command selects register in the second group.

Code 18, Selective Overwrite Group 1 Register

Same as Code 16, except a separate "mask" register defines which bits in the selected register are set.

Code 19, Selective Overwrite Group 2 Register

Same as Code 18, except command selects register in the second group.

Code 20 - 23

Unassigned at this time.

CONTROL COMMANDS (Function Codes 24 - 31)

Control commands are identified generally by F8 = 1 in the function code. They are divided into two groups by the state of F16, in this case F16 = 1. They specify that information is not transferred on either the R or W bus-lines. However, information may be conveyed by the Q bus-line in any of these commands. The signal on the Q bus-line is permitted to change at any time but is strobed into the controller at time S1 and may (except in Code 27) be reset by strobe S2. Precautions must be taken to ensure that information is not lost due to Q signals appearing between S1 and S2.

Code 24, Disable

This command selects, by sub-address, and disables a feature of the module; e.g., a Look-at-Me source or a data input.

Code 25, Increment Preselected Registers

This command adds one simultaneously to the contents of each register in one of 16 groups, defined by the sub-address.

Code 26, Enable

This command enables the feature of the module selected by the sub-address, e.g., a Look-at-Me source or a data input.

Code 27, Test Status

This command selects, by sub-address, any feature of a module other than a source of a Look-at-Me request, and tests it by producing a response on the Q bus-line.

Code 28 - 31

Unassigned at this time.

DIGITAL SIGNAL STANDARDS ON THE DATAWAY

The potentials for the binary digital signals on the Dataway lines have been defined to correspond with those for compatible current sinking logic devices (e.g., the TTL and DTL series). The signal convention has, however, been inverted to be negative logic. The high state (more positive potential) corresponds to logic '0' and the low state (near ground potential) corresponds to logic '1'. Intrinsic OR outputs are thus available from the manufacturers' standard product range, and disconnected inputs go to the '0' state.

It is an essential feature of the Dataway that many units may have their signal outputs connected to the Read and Response lines. Outputs onto these lines therefore require intrinsic OR gates. The same principle is extended to other lines (Command, Write, etc.) in order to allow more than one controller-like unit in a crate. The Inhibit line may be an exception, since its signals are shaped with a slow rise and fall if they change during Dataway operations.

Voltage standards for Dataway Signals

All Dataway Signals must conform to the voltage levels as follows:

Pull-up current sources for all Dataway bus-lines are located in the crate controller (occupying the control station and at least one other station) so as to insure that there is one and only one current source per line. The minimum pull-up current when the Dataway line is at +3.5 V is defined in Table 4 as 2.5 mA but, if the controller generates Dataway signals at time intervals near the permitted minima, the pull-up current sources should preferably provide not less than 6 mA when the lines are at this potential. The pull-up for the N signals is located in the unit generating the signals and for the L signals in the unit receiving the signals so that the individual lines may be joined or grouped within these units if desired.

The N and L lines are effectively individual lines joining two units (a module and a controller) together. The Q and R lines will generally have many units generating the signals (say 20) with a few units (maximum 4) receiving the signals. The remaining lines (W, A, F, S, B, Z, I, C) will have relatively few units generating each signal (often only one) with the possibility of many units receiving the signals.

Timing of Dataway Signals

The sequence of events during a single Dataway operation is shown in Timing Diagram, Page 13C, by means of simplified signal waveforms. The shaded areas indicate the permitted variation of each signal between an ideal square signal and a signal whose transition across the appropriate signal threshold (0.8 V or 2.0 V) satisfies the conditions shown. The signal waveforms for the command and data lines apply to those lines, if any, which take up the '1' state. Other command and data lines may, of course, be in the '0' state during the operation.

The signals on the Busy line and the various signals constituting the command need not occur in exact synchroism, provided their envelope lies within the shaded areas of the diagram. Similar variation is permitted between the signals constituting the data. The broken line indicates the earlies time at which the data signals may change in response to S2.

Key points on these waveforms are indicated by t_0 - t_9, with the following significance:

Points t_0, t_3, t_6 represent the initiation of the negative-going of the Command, Strobe 1, and Strobe 2 signals, respectively. They are the times at which the signals would be received from an ideal Dataway with no capacitative loading.

Points t_9, t_5, t_8 represent similarly the initiation of the positive-going edges of the same signals.

Points t_2, t_{11} are the latest times at which the data source is permitted to initiate the negative-going and positive-going edges of the data signals.

Points t_1, t_3, t_4, t_7 represent the latest times at which the received signals are permitted to reach a maintained '1' state, and therefore refer to the last negative-going transition across the + 0.8 V threshold.

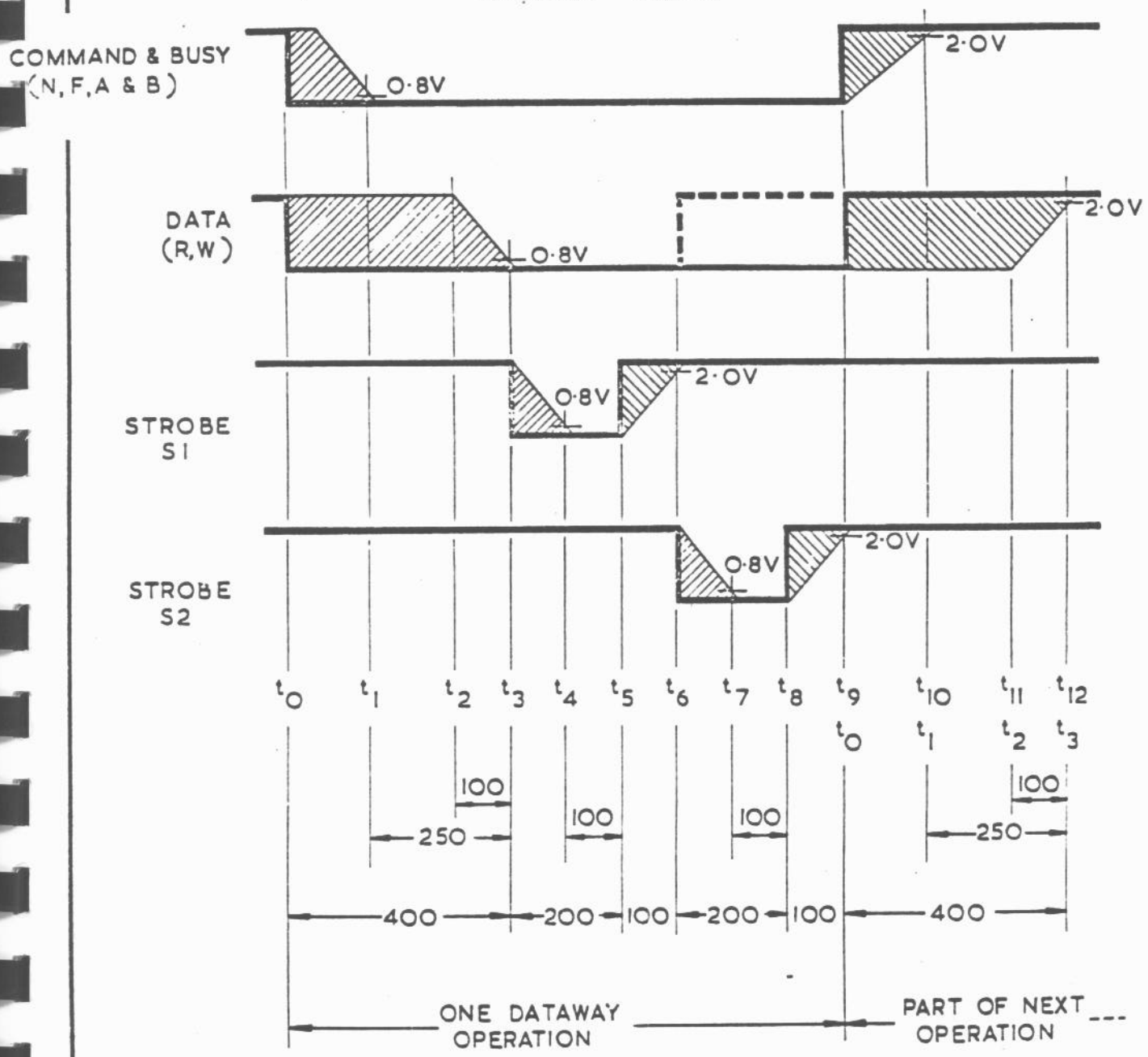
Points t_6, t_9, t_{10}, t_{12} represent the latest times at which the received signals are permitted to reach a maintained '0' state, and therefore refer to the last positive-going transition across the + 2.0 V threshold.

Controllers must initiate the negative and positive going edges of the command and strobe signals at intervals not less than those defined by t_3, t_5, t_6, t_8 and t_9. Modules respond to the command within the most adverse value of $(t_1 - t_2)$; i.e., 100 ns. The electrical characteristics of the Dataway and connections from it into units must allow signals to rise and fall within the minimum times for $(t_0 - t_1)$, $(t_2 - t_3)$ etc.

The next Dataway operation must not start before t_9.

The extreme case is shown in Timing Diagram, Page 15C, with the next operation starting at t_9, so that $t_9 - t_{12}$ of one operation coincide with $t_0 - t_3$ of the next. The command and data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive Dataway operations. Under suitable conditions any command or data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive Dataway operations. Under suitable conditions any command or data signals which have the same state during successive operations may also be maintained. In the extreme case of successive operations with the same command and data there could be a complete absence of signal transitions between t_0 and t_3.

DATAWAY TIMING



TIMES GIVEN ARE MINIMUM VALUES IN NANOSECONDS

TIMING OF A DATAWAY OPERATION.

POWER SUPPLIES

The voltage tolerances and current loadings are specified below. The specified tolerances in voltage refer to the voltage measured at the contacts of the Dataway sockets and must be maintained under the worst combination of factors such as a.c. mains voltages and frequency, the maximum current loadings, temperature and the position in the crate of the socket under observation.

Note that the maximum currents stated in the below table are subject to the over-all restrictions as follows:

1. The current carried by any contact of the Dataway socket must not exceed 3 A.
2. The total power dissipated in a crate, without forced ventilation, must not exceed 200 W.
3. The power dissipation per single width station should not, therefore, normally exceed 8 W; however, under special circumstances this rating may be increased to a maximum of 25 W provided suitable precautions are taken to comply with total power dissipation and current loadings.

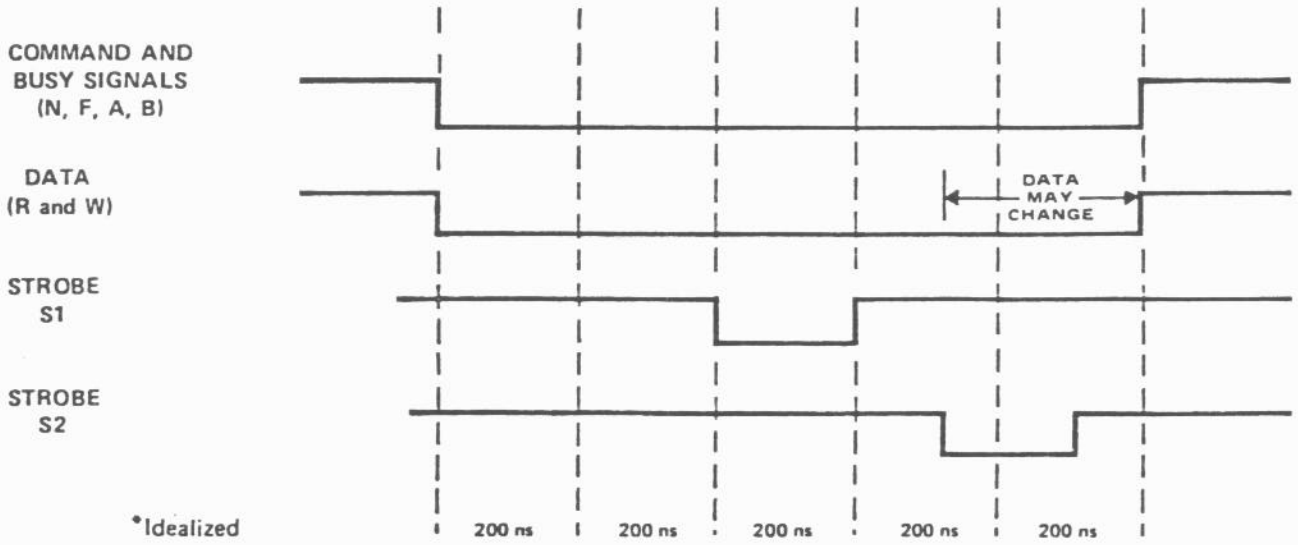
The resistance between any point on the Dataway OV power return bus-line and the point at which the power supply is joined to the crate wiring must not exceed 2 milliohms.

Supply Voltage	Voltage Tolerance	Maximum Current Loads	
		In the Plug-in (per unit width) See Notes (1) & (3) Above	In the crate See Note (2) Above
Mandatory			
+24V d.c.	± 0.5%	1A	6A
+ 6V d.c.	±2.5%	2A	25A
- 6V d.c	±2.5%	2A	25A
-24V d.c	±0.5%	1A	6A
OV			
Additional (as required)			
+200V d.c.	+60V, -20V		0.1A
+ 12V d.c.	± 0.5%		
- 12V d.c.	± 0.5%		
117V a.c.	+10%, -12%		0.5A

CAMAC FUNCTION CODES

CODE F( )	FUNCTION	FUNCTION SIGNALS					CODE F( )
		F16	F8	F4	F2	F1	
0	Read Group 1 Register	0	0	0	0	0	0
1	Read Group 2 Register	0	0	0	0	1	1
2	Read and Clear Group 1 Register	0	0	0	1	0	2
3	Read Complement of Group 1 Register	0	0	0	1	1	3
4	Non-standard	0	0	1	0	0	4
5	Reserved	0	0	1	0	1	5
6	Non-standard	0	0	1	1	0	6
7	Reserved	0	0	1	1	1	7
8	Test Look-at-Me	0	1	0	0	0	8
9	Clear Group 1 Register	0	1	0	0	1	9
10	Clear Look-at-Me	0	1	0	1	0	10
11	Clear Group 2 Register	0	1	0	1	1	11
12	Non-standard	0	1	1	0	0	12
13	Reserved	0	1	1	0	1	13
14	Non-standard	0	1	1	1	0	14
15	Reserved	0	1	1	1	1	15
16	Overwrite Group 1 Register	1	0	0	0	0	16
17	Overwrite Group 2 Register	1	0	0	0	1	17
18	Selective Set Group 1 Register	1	0	0	1	0	18
19	Selective Set Group 2 Register	1	0	0	1	1	19
20	Non-standard	1	0	1	0	0	20
21	Selective Clear Group 1 Register	1	0	1	0	1	21
22	Non-standard	1	0	1	1	0	22
23	Selective Clear Group 2 Register	1	0	1	1	1	23
24	Disable	1	1	0	0	0	24
25	Execute	1	1	0	0	1	25
26	Enable	1	1	0	1	0	26
27	Test Status	1	1	0	1	1	27
28	Non-standard	1	1	1	0	0	28
29	Reserved	1	1	1	0	1	29
30	Non-standard	1	1	1	1	0	30
31	Reserved	1	1	1	1	1	31

DATAWAY TIMING *



*Idealized

PIN ALLOCATION AT NORMAL STATION

(Stations 1-24)

Bus-line	Free Bus-line	P1	B	Busy	Bus-line
Bus-line	Free Bus-line	P2	F16	Function	Bus-line
Individual patch contact		P3	F8	Function	Bus-line
Individual patch contact		P4	F4	Function	Bus-line
Individual patch contact		P5	F2	Function	Bus-line
Bus-line	Command Accepted	X	F1	Function	Bus-line
Bus-line	Inhibit	I	A8	Sub-address	Bus-line
Bus-line	Clear	C	A4	Sub-address	Bus-line
Individual line	Station Number	N	A2	Sub-address	Bus-line
Individual line	Look-at-Me	L	A1	Sub-address	Bus-line
Bus-line	Strobe 1	S1	Z	Initialize	Bus-line
Bus-line	Strobe 2	S2	Q	Response	Bus-line
		W24	W23		
		W22	W21		
		W20	W19		
		W18	W17		
		W16	W15		
		W14	W13		
		W12	W11		
		W10	W9		
		W8	W7		
		W6	W5		
		W4	W3		
		W2	W1		
		R24	R23		
		R22	R21		
		R20	R19		
		R18	R17		
		R16	R15		
		R14	R13		
		R12	R11		
		R10	R9		
		R8	R7		
		R6	R5		
		R4	R3		
		R2	R1		
Power Bus-lines	−12V d.c.	−12	−24	−24V d.c.	Power Bus-lines
	+200V d.c.	+200	−6	−6V d.c.	
	117V a.c. Live	ACL	ACN	117V a.c. Neutral	
	Reserved	Y1	E	Clean Earth	
	+12V d.c.	+12	+24	+24V d.c.	
	Reserved	Y2	+6	+6V d.c.	
	OV (Power Return)	0	0	OV (Power Return)	

24 Write Bus Lines

W1 = least significant bit
W24 = most significant bit

24 Read Bus Lines

R1 = least significant bit
R24 = most significant bit

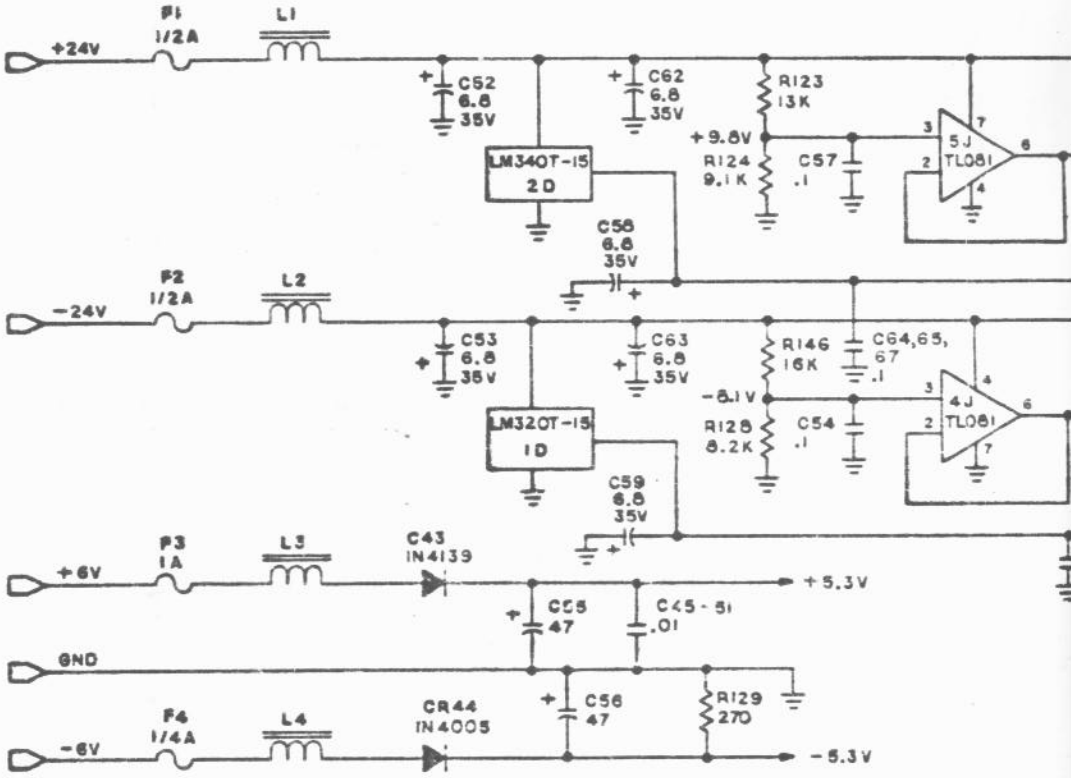
PIN ALLOCATION AT CONTROL STATION

(Station 25)

Individual patch contact		P1	B	Busy	Bus-line
Individual patch contact		P2	F16	Function	Bus-line
Individual patch contact		P3	F8	Function	Bus-line
Individual patch contact		P4	F4	Function	Bus-line
Individual patch contact		P5	F2	Function	Bus-line
Bus-line	Command Accepted	X	F1	Function	Bus-line
Bus-line	Inhibit	I	A8	Sub-address	Bus-line
Bus-line	Clear	C	A4	Sub-address	Bus-line
Individual patch contact		P6	A2	Sub-address	Bus-line
Individual patch contact		P7	A1	Sub-address	Bus-line
Bus-line	Strobe 1	S1	Z	Initialize	Bus-line
Bus-line	Strobe 2	S2	Q	Response	Bus-line
		L24	N24		
		L23	N23		
		L22	N22		
		L21	N21		
		L20	N20		
		L19	N19		
		L18	N18		
		L17	N17		
		L16	N16		
		L15	N15		
		L14	N14		
24 Individual Look-at-Me Lines		L13	N13	24 Individual Station Number Lines	
L1 from Station 1, etc.		L12	N12	N1 to Station 1, etc.	
		L11	N11		
		L10	N10		
		L9	N9		
		L8	N8		
		L7	N7		
		L6	N6		
		L5	N5		
		L4	N4		
		L3	N3		
		L2	N2		
		L1	N1		
	−12V dc.	−12	−24	−24V d.c.	
	+200V d.c.	+200	−6	−6V d.c.	
Power	117V a.c. Live	ACL	ACN	117V a.c. Neutral	Power
Bus-lines	Reserved	Y1	E	Clean Earth	Bus-lines
	+12V d.c.	+12	+24	+24V d.c.	
	Reserved	Y2	+6	+6V d.c.	
	OV (Power Return)	0	0	OV (Power Return)	

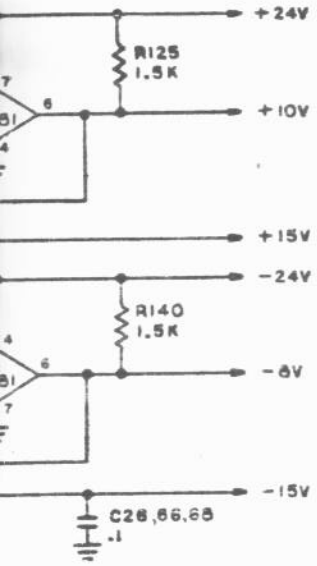
STANDARD DATAWAY USAGE

TITLE	DESIGNATION	CON-TACTS	USE AT A MODULE
Command			
Station Number	N	1	Selects the module (Individual line from control station).
Sub-Address	A1, 2, 4, 8	4	Selects a section of the module.
Function	F1, 2, 4, 8, 16	5	Defines the function to be performed in the module.
Timing			
Strobe 1	S1	1	Controls first phase of operation (Dataway signals must not change).
Strobe 2	S2	1	Controls second phase (Dataway signals may change).
Data			
Write	W1 – W24	24	Bring information to the module.
Read	R1 – R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service (Individual line to control station).
Busy	B	1	Indicates that a Dataway operation is in progress.
Response	Q	1	Indicates status of feature selected by command.
Command Accepted	X	1	Indicates that module is able to perform action required by the command.
Common Controls			*Operate on all stations connected to them, no command required.*
Initialize	Z	1	Sets module to a defined state. (Accompanied by S2 and B).
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears registers. (Accompanied by S2 and B).
Non-Standard Connections			
Free bus-lines	P1, P2	2	For unspecified uses.
Patch contacts	P3 – P5	3	For unspecified interconnections. No Dataway Lines.
Mandatory Power Lines			*The crate is wired for mandatory and additional lines.*
+24V d.c.	+24	1	
+6V d.c.	+6	1	
−6V d.c.	−6	1	
−24V d.c.	−24	1	
OV	0	2	Power return
Additional Power Lines			*Lines are reserved for the following power supplies.*
+200V d.c.	+200	1	Low current for indicators etc.
+12V d.c.	+12	1	
−12V d.c.	−12	1	
117V a.c. (Live)	ACL	1	
117V a.c. (Neutral)	ACN	1	
Clean Earth	E	1	Reference for circiuts requiring clean earth
Reserved	Y1, Y2	2	Reserved for future allocation.
TOTAL		86	



NOTE, UNLESS OTHERWISE SPECIFIED:

1. ALL CAPACITORS ARE IN MICROFARDS.
2. ALL DIODES ARE IN4448.
3. ALL RESISTORS ARE IN OHMS, 1/4W, ± 5%.
4. VOLTAGE READING VALID WITH NO INPUT SIGNAL AND GAIN SWITCHES SET TO 1 POSITION. (REMOTE / LOCAL SWITCH IN LOCAL POSITION)



TO PIN 4 ON DS8800 IC'S:
3F,7F,2G,3G,7G,8G,4H,
6H,4I,6I

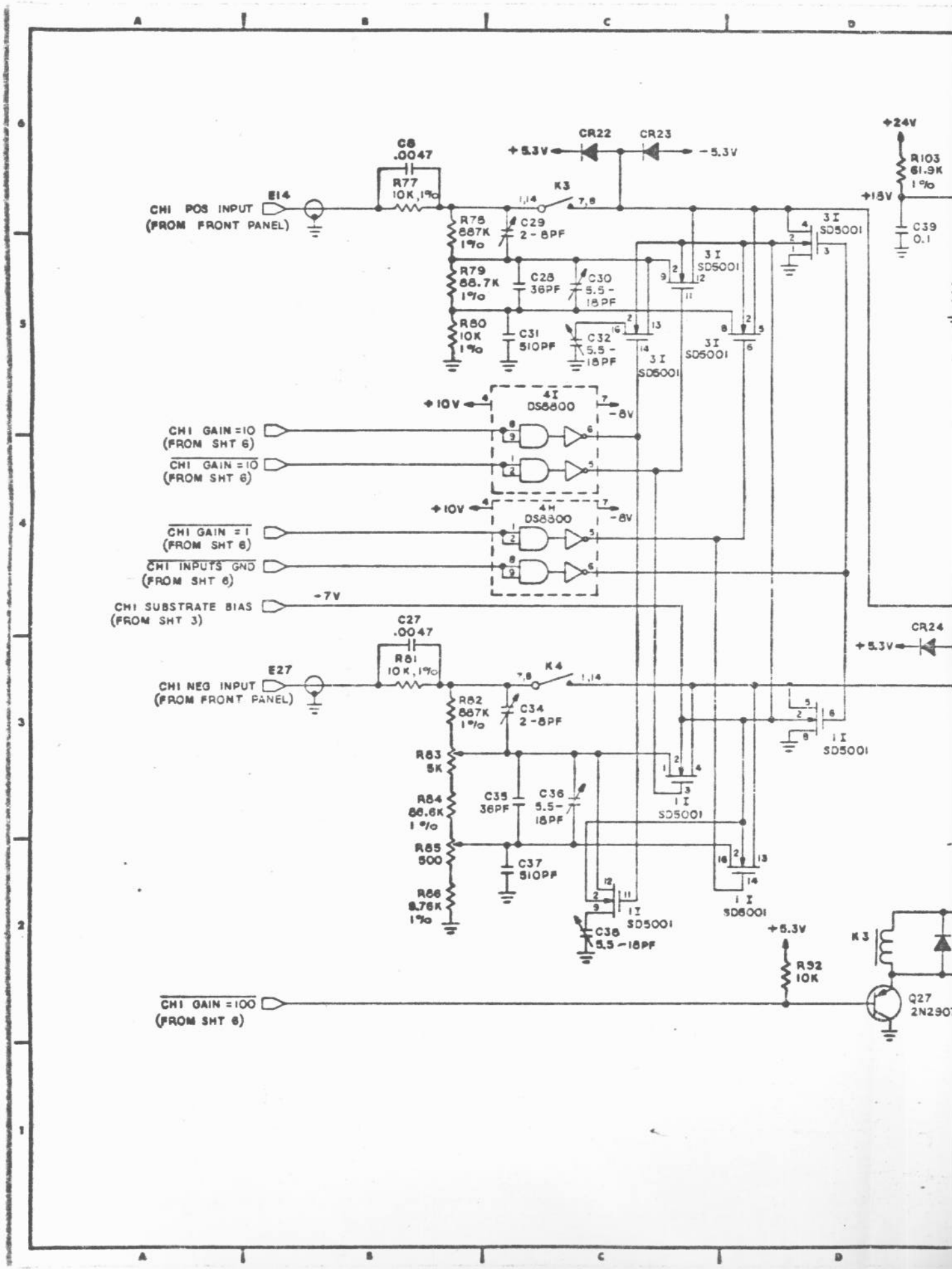
TO PIN 7 ON DS8800 IC'S:
3F,7F,2G,3G,7G,8G,4H,
6H,4I,6I

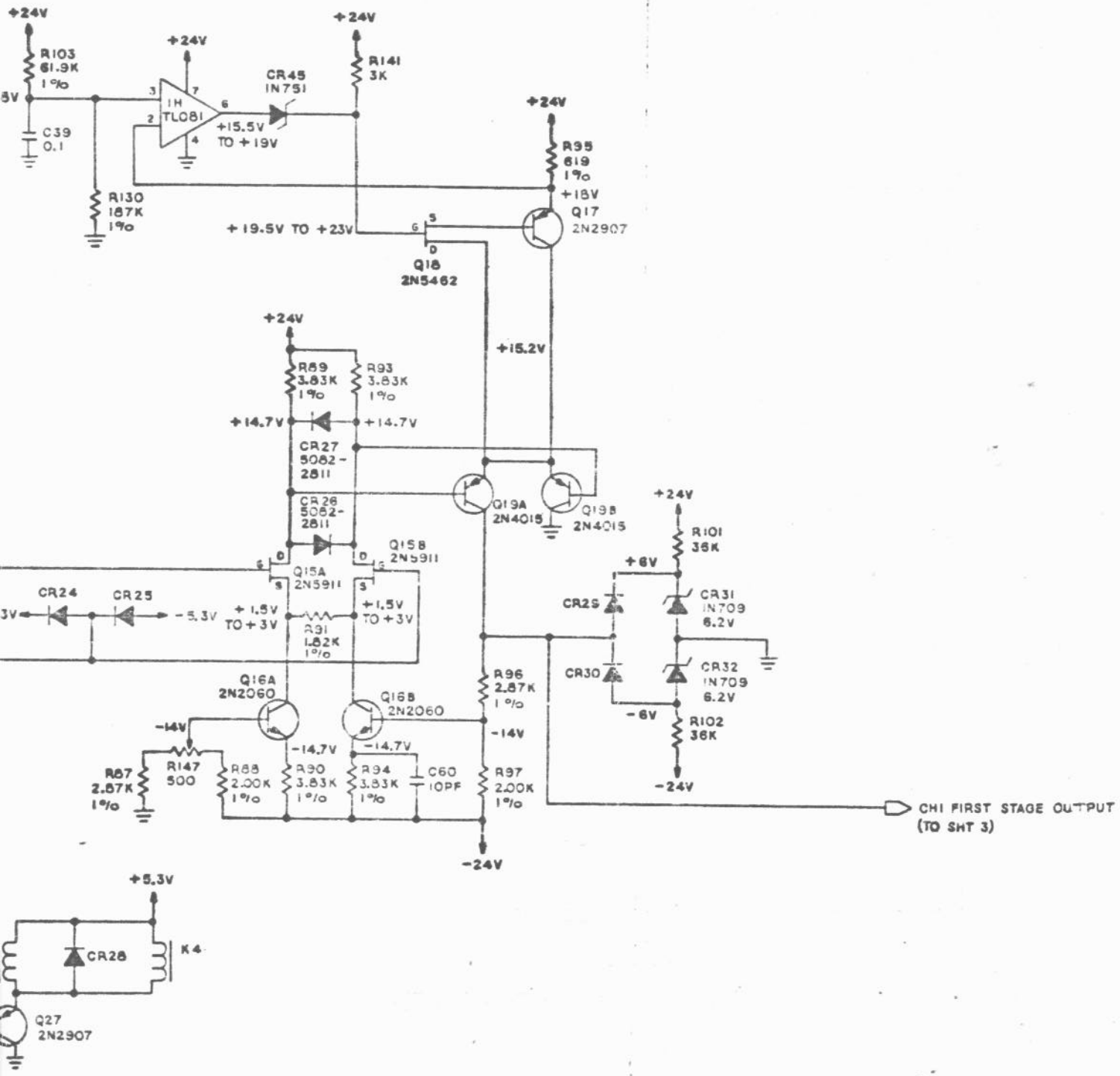
TYPE	POSITION	UNUSED ELEMENTS	+5V PIN	GND PIN	+15V PIN	-15V PIN
74LS00	9C		14	7		
74LS01	8B		14	7		
74LS02	1A		14	7		
74LS08	6F		14	7		
74LS20	4B		14	7		
74LS30	1B,2B		14	7		
74LS32	1C		14	7		
74LS112	5G		16	8		
74LS132	5F		14	7		
74LS138	3B		16	8		
74LS157	3A,8A,4C,7C		16	8		
74LS191	5A,6A,5C,6C,5E,6E		16	8		
74LS367	7A,5B,6B,7B,9B,4D, 5D,6D,7D,8D,9D		16	8		
74LS375	2A,9A,3C,8C		16	8		
DS8800	3F,7F,2G,3G,7G,8G, 4H,6H,4I,6I		10	3		
74LS221	5H		16	8		
DAI200	4E,7E		20	24	22	23
LM320	1D					
LM340	2D					
NE555	6G		8	1		
SD500-	2I,3H,7H,9I,1I, 5I,7I,9I					
TL081CP	1C,2E,9E,1F,2F,9F, 1H,10H,9G,10G					

REF DESIGNATION LAST USED	REF DESIGNATION NOT USED
C72	
CR48	
F4	
K4	
L4	
R148	
Q29	Q12

LeCroy RESEARCH SYSTEMS

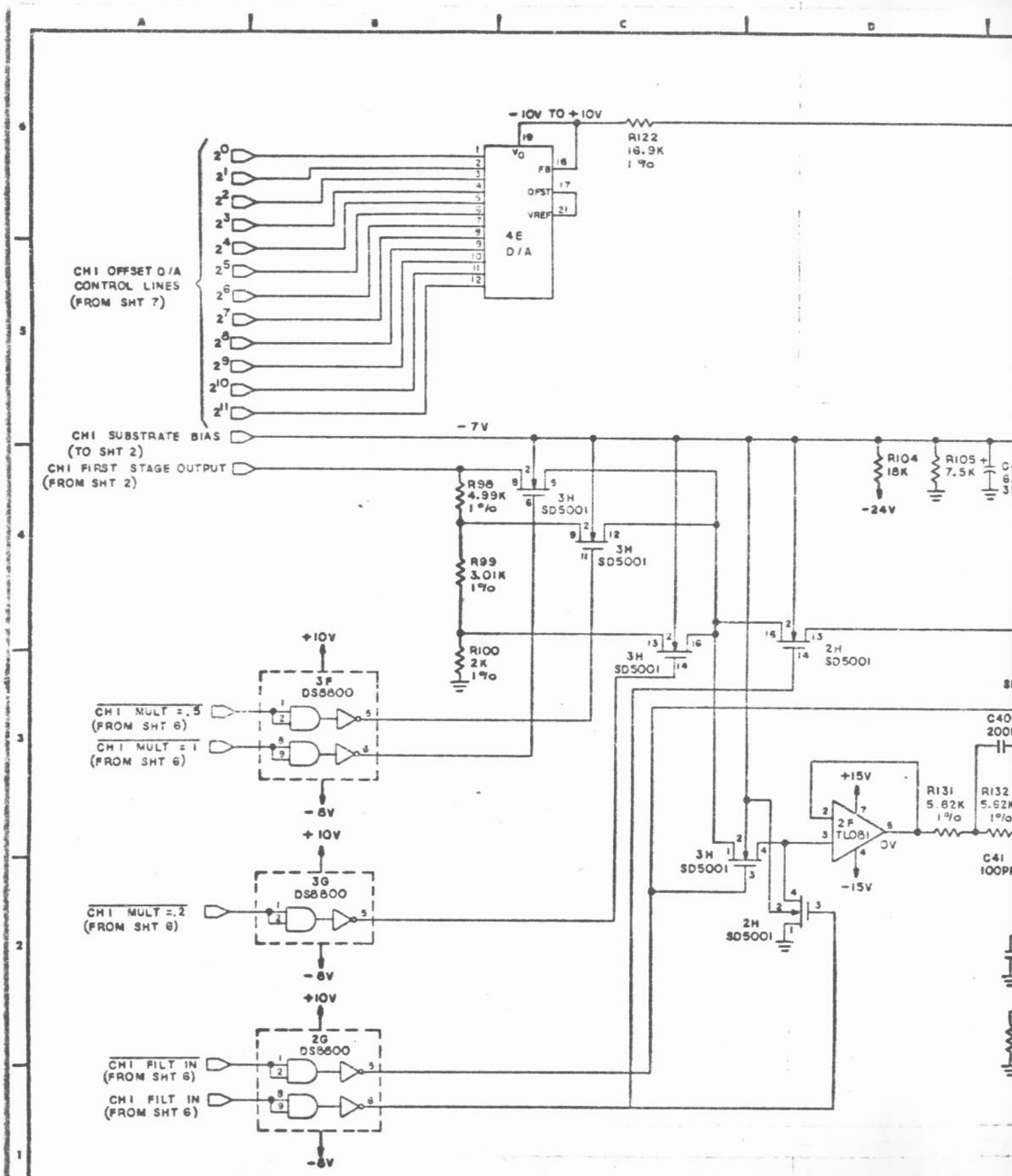
DRAWN RTC	8100 AMPLIFIER
CHECKED RTC 5/4/79	
DATE 5/79	
DRAWING NUMBER: 8100	SHEET 1 OF 8
ECO NO. 1004 DATE 5/79	

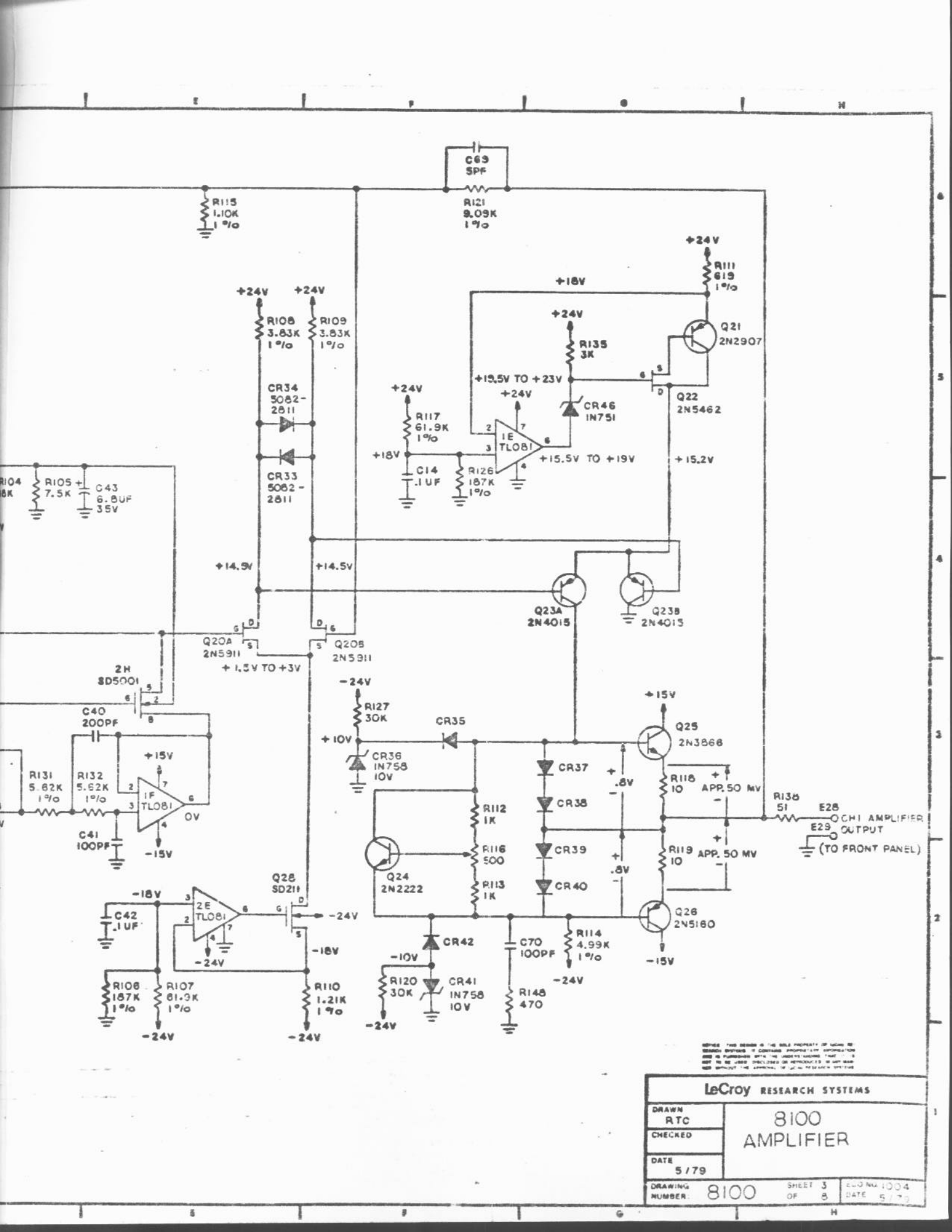

C8
.0047
R77
10K, 1%
CHI POS INPUT
(FROM FRONT PANEL)
E14
CR22
CR23
+5.3V
-5.3V
K3
1,14
7,8
R78
887K
1%
C29
2-8PF
R79
88.7K
1%
C28
36PF
C30
5.5-
18PF
R80
10K
1%
C31
510PF
C32
5.5-
18PF
3 I
SD5001
+24V
R103
61.9K
1%
+15V
C39
0.1
+10V
4 I
DS8600
-8V
CHI GAIN=10
(FROM SHT 6)
CHI GAIN=10
(FROM SHT 6)
4 H
DS8600
CHI GAIN = 1
(FROM SHT 6)
CHI INPUTS GND
(FROM SHT 6)
-7V
CHI SUBSTRATE BIAS
(FROM SHT 3)
C27
.0047
R81
10K, 1%
CHI NEG INPUT
(FROM FRONT PANEL)
E27
K4
R82
887K
1%
C34
2-8PF
R83
5K
R84
88.6K
1%
C35
36PF
C36
5.5-
18PF
R85
500
C37
510PF
R86
8.76K
1%
C38
5.5-18PF
1 I
SD5001
CR24
+5.3V
R92
10K
K3
Q27
2N2907
CHI GAIN=100
(FROM SHT 6)



LeCroy RESEARCH SYSTEMS

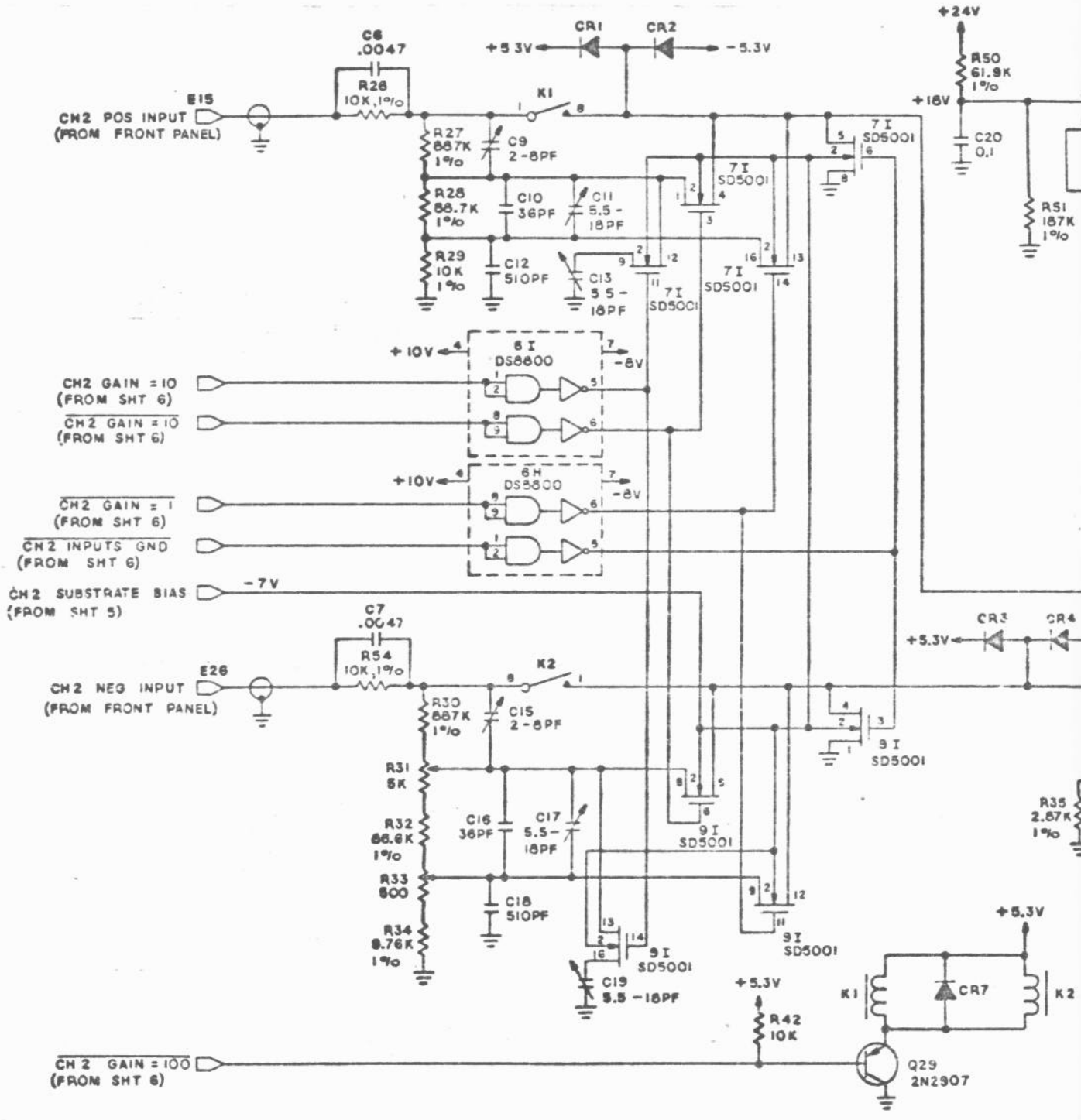
DRAWN RTC	8100 AMPLIFIER
CHECKED	
DATE 5/79	
DRAWING NUMBER: 8100	SHEET 2 OF 8 | ECO NO. 1004 DATE 5/79

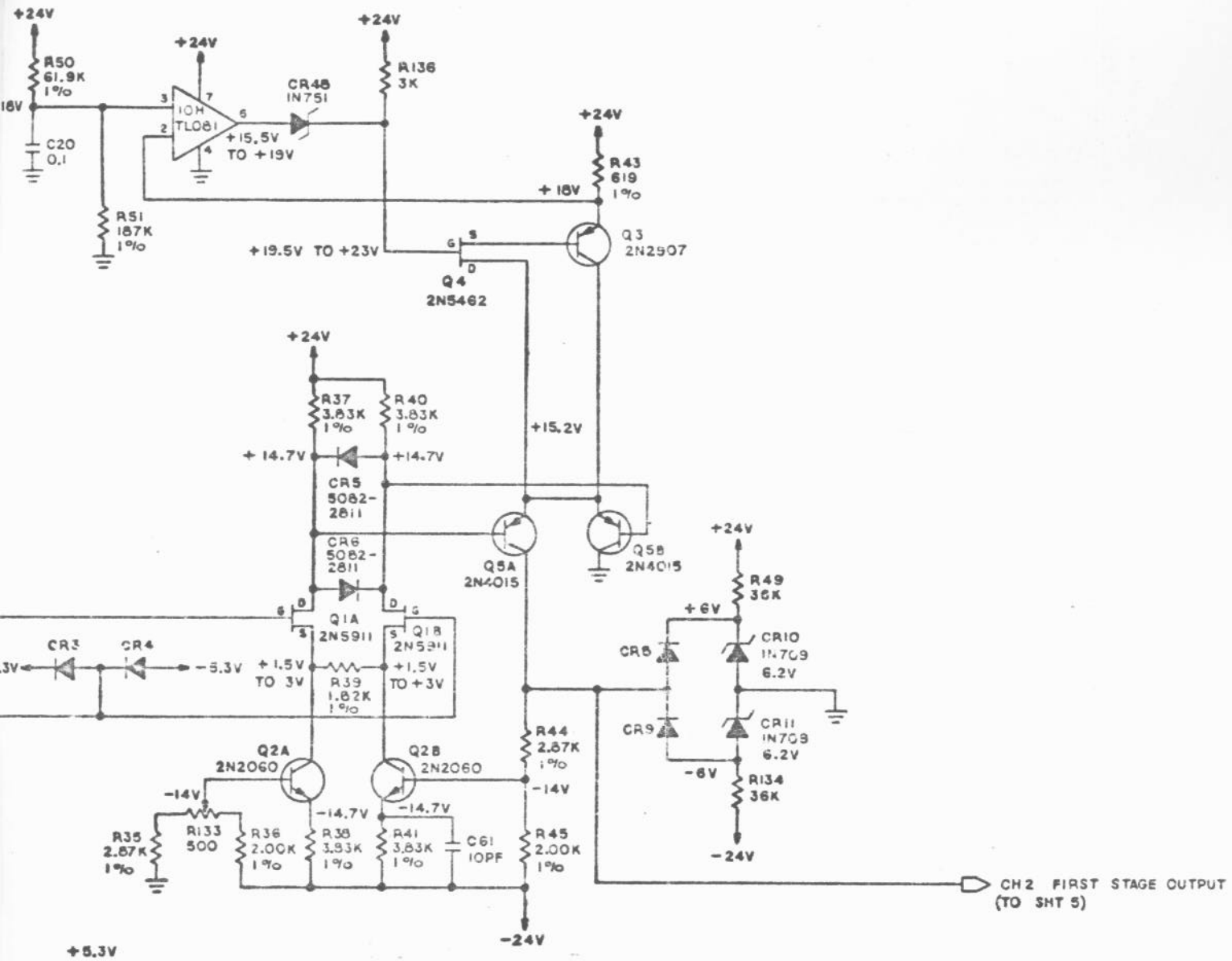

-10V TO +10V
R122
16.9K
1%
CH1 OFFSET D/A
CONTROL LINES
(FROM SHT 7)
4E
D/A
CH1 SUBSTRATE BIAS
(TO SHT 2)
-7V
CH1 FIRST STAGE OUTPUT
(FROM SHT 2)
R98
4.99K
1%
R99
3.01K
1%
R100
2K
1%
3H
SD5001
R104
18K
R105
7.5K
-24V
+10V
3F
DS8600
CH1 MULT =.5
(FROM SHT 6)
CH1 MULT = 1
(FROM SHT 6)
-8V
3G
DS8600
CH1 MULT =.2
(FROM SHT 6)
2G
DS8600
CH1 FILT IN
(FROM SHT 6)
2H
SD5001
+15V
2F
TL081
0V
-15V
R131
5.62K
1%
R132
5.62K
1%
C40
200
C41
100PF



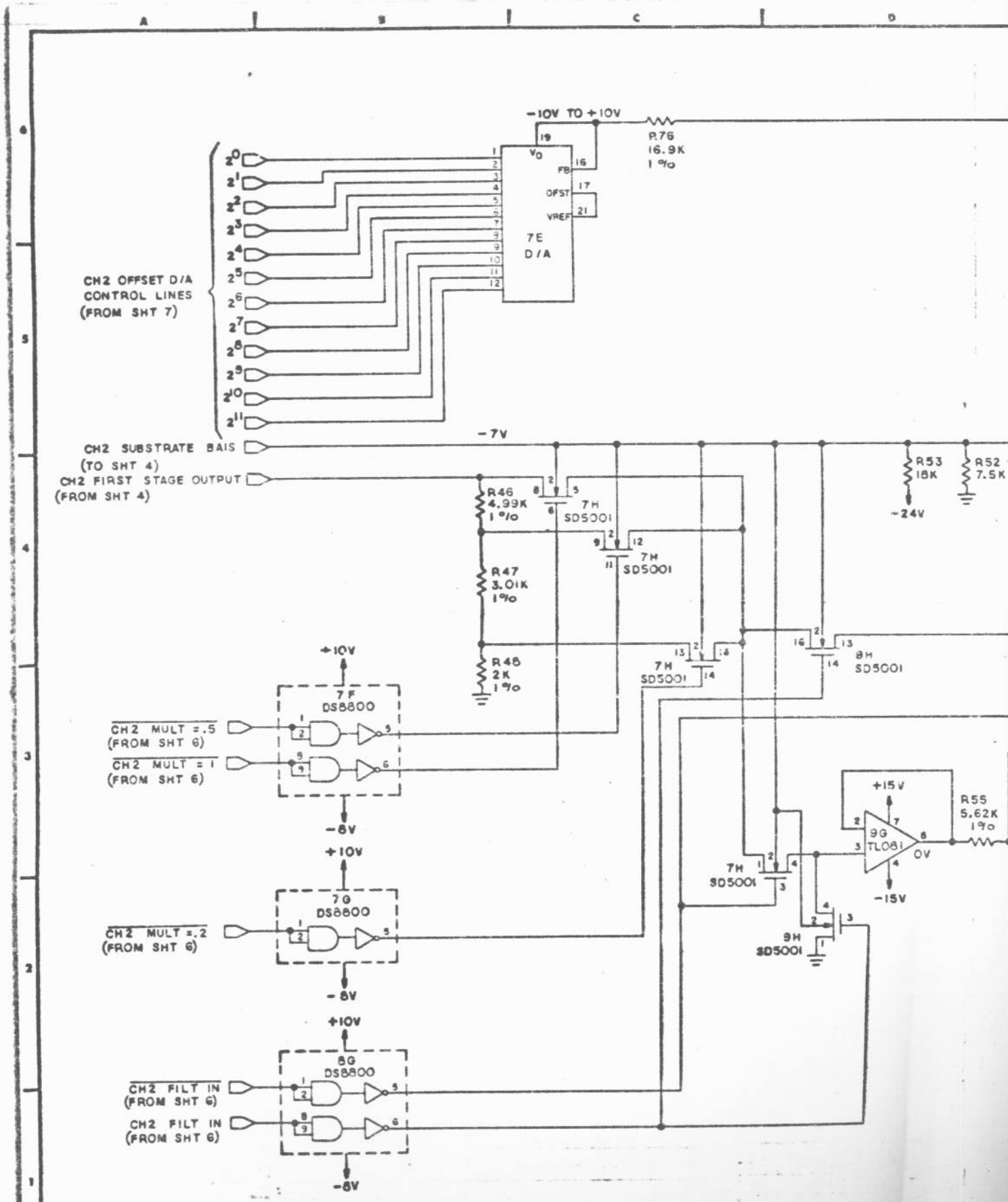
LeCroy RESEARCH SYSTEMS

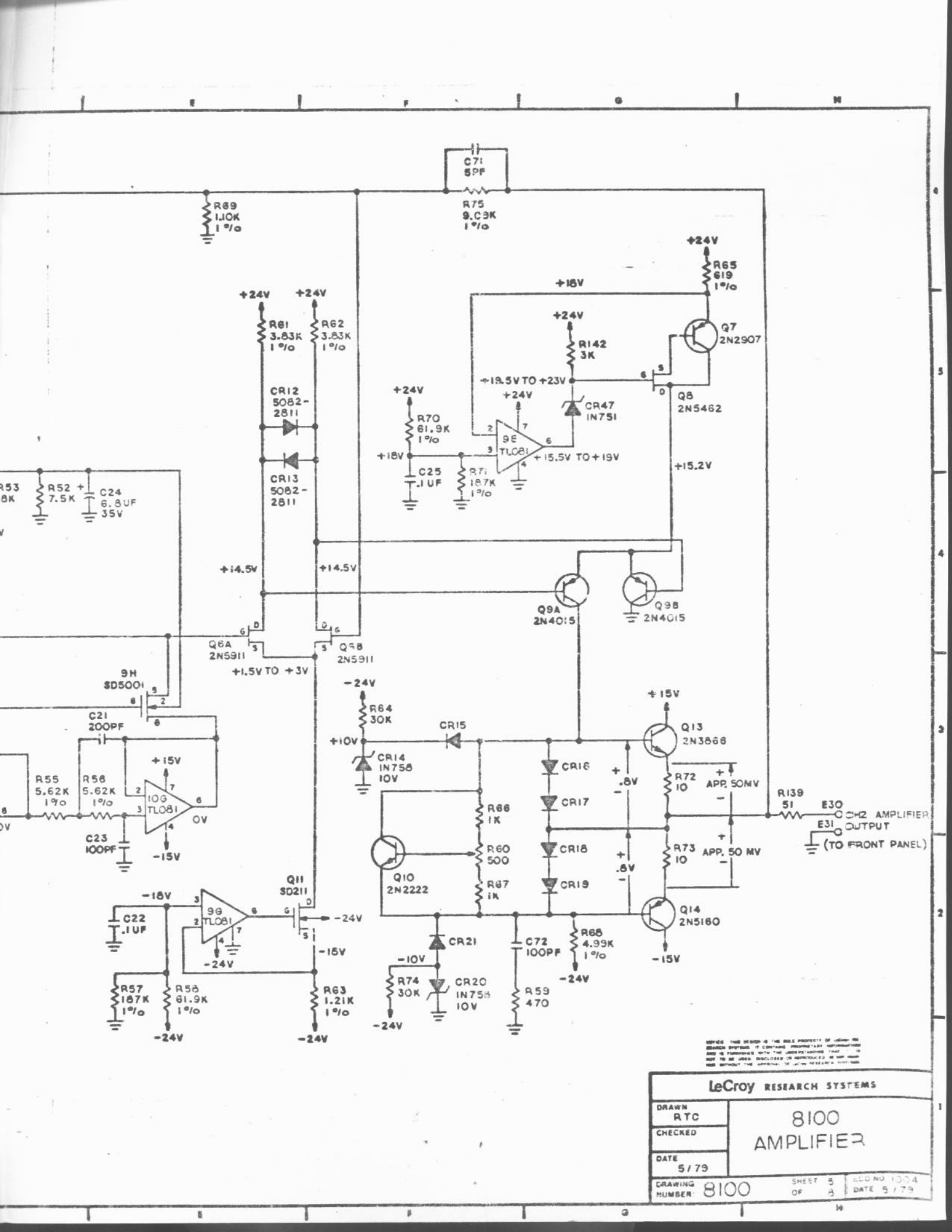
DRAWN RTC	8100 AMPLIFIER
CHECKED	
DATE 5/79	
DRAWING NUMBER 8100	SHEET 3 OF 8


C6
.0047
R26
10K,1%
E15
CH2 POS INPUT
(FROM FRONT PANEL)
CR1
CR2
+5.3V
-5.3V
K1
+24V
R50
61.9K
1%
+16V
C20
0.1
R51
187K
1%
R27
887K
1%
C9
2-8PF
R28
88.7K
1%
C10
36PF
C11
5.5-
18PF
R29
10K
1%
C12
510PF
C13
5.5-
18PF
7I
SD5001
+10V
6I
DS8600
-8V
CH2 GAIN = 10
(FROM SHT 6)
CH2 GAIN = 10
(FROM SHT 6)
6H
DS8600
CH2 GAIN = 1
(FROM SHT 6)
CH2 INPUTS GND
(FROM SHT 6)
CH2 SUBSTRATE BIAS
(FROM SHT 5)
-7V
C7
.0047
R54
10K,1%
E26
CH2 NEG INPUT
(FROM FRONT PANEL)
K2
CR3
CR4
+5.3V
R30
887K
1%
C15
2-8PF
9I
SD5001
R31
5K
R32
88.8K
1%
C16
36PF
C17
5.5-
18PF
R33
500
R34
8.76K
1%
C18
510PF
C19
5.5-18PF
R35
2.67K
1%
+5.3V
R42
10K
K1
CR7
K2
Q29
2N2907
CH2 GAIN = 100
(FROM SHT 6)

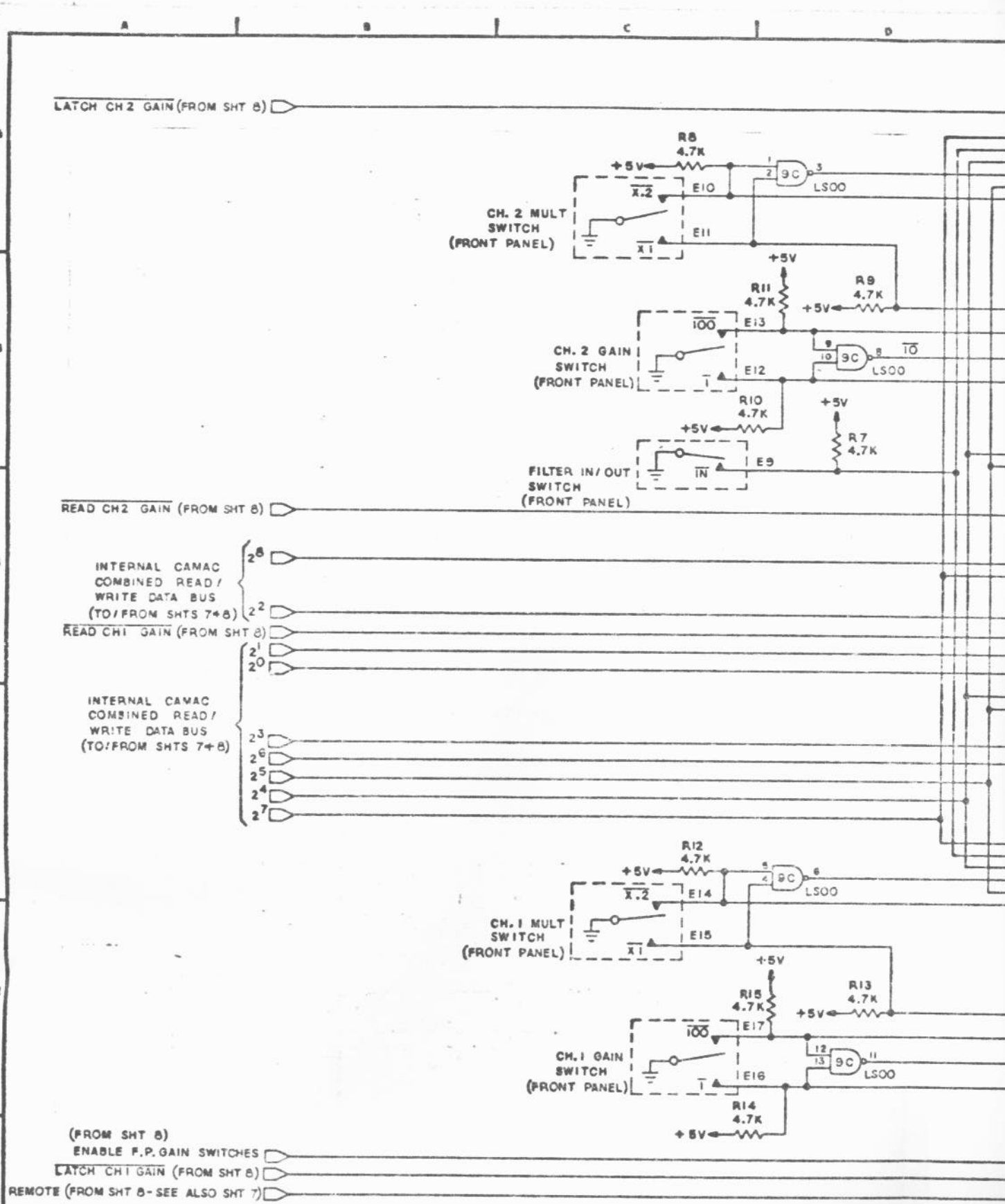


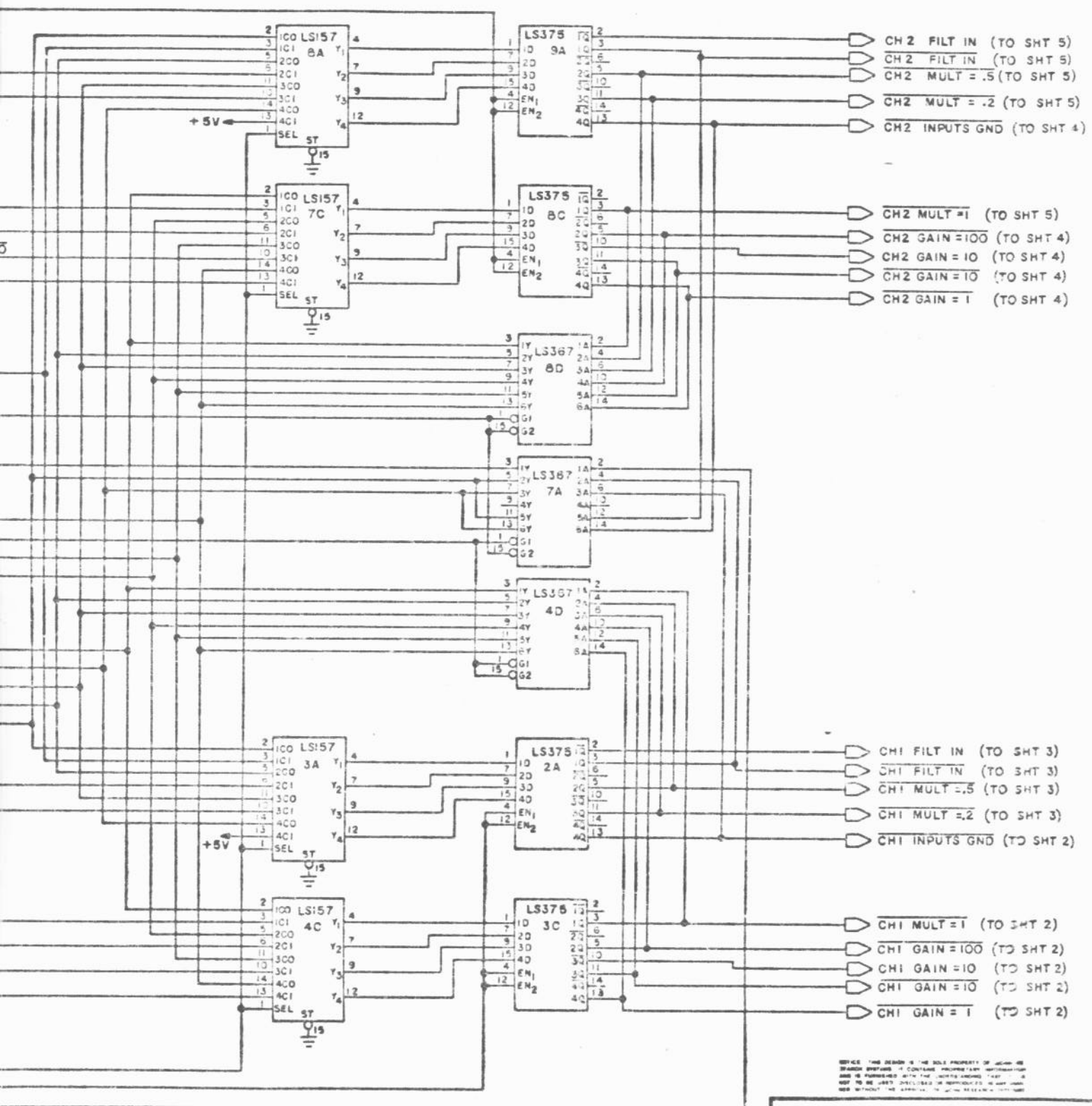
LeCroy RESEARCH SYSTEMS	
DRAWN RTC	8100 AMPLIFIER
CHECKED MK 5/6/79	
DATE 5/79	
DRAWING NUMBER 8100	SHEET 4 OF 8
ECO NO. 1004 DATE 5/79	


-10V TO +10V
R76
16.9K
1%
7E
D/A
CH2 OFFSET D/A
CONTROL LINES
(FROM SHT 7)
CH2 SUBSTRATE BAIS
(TO SHT 4)
CH2 FIRST STAGE OUTPUT
(FROM SHT 4)
-7V
R46
4.99K
1%
R47
3.01K
1%
R48
2K
1%
7H
SD5001
R53
18K
-24V
R52
7.5K
8H
SD5001
+10V
7F
DS8800
CH2 MULT =.5
(FROM SHT 6)
CH2 MULT = 1
(FROM SHT 6)
-8V
7G
DS8800
CH2 MULT =.2
(FROM SHT 6)
8G
DS8800
CH2 FILT IN
(FROM SHT 6)
+15V
9G
TL081
0V
-15V
R55
5.62K
1%
9H
SD5001



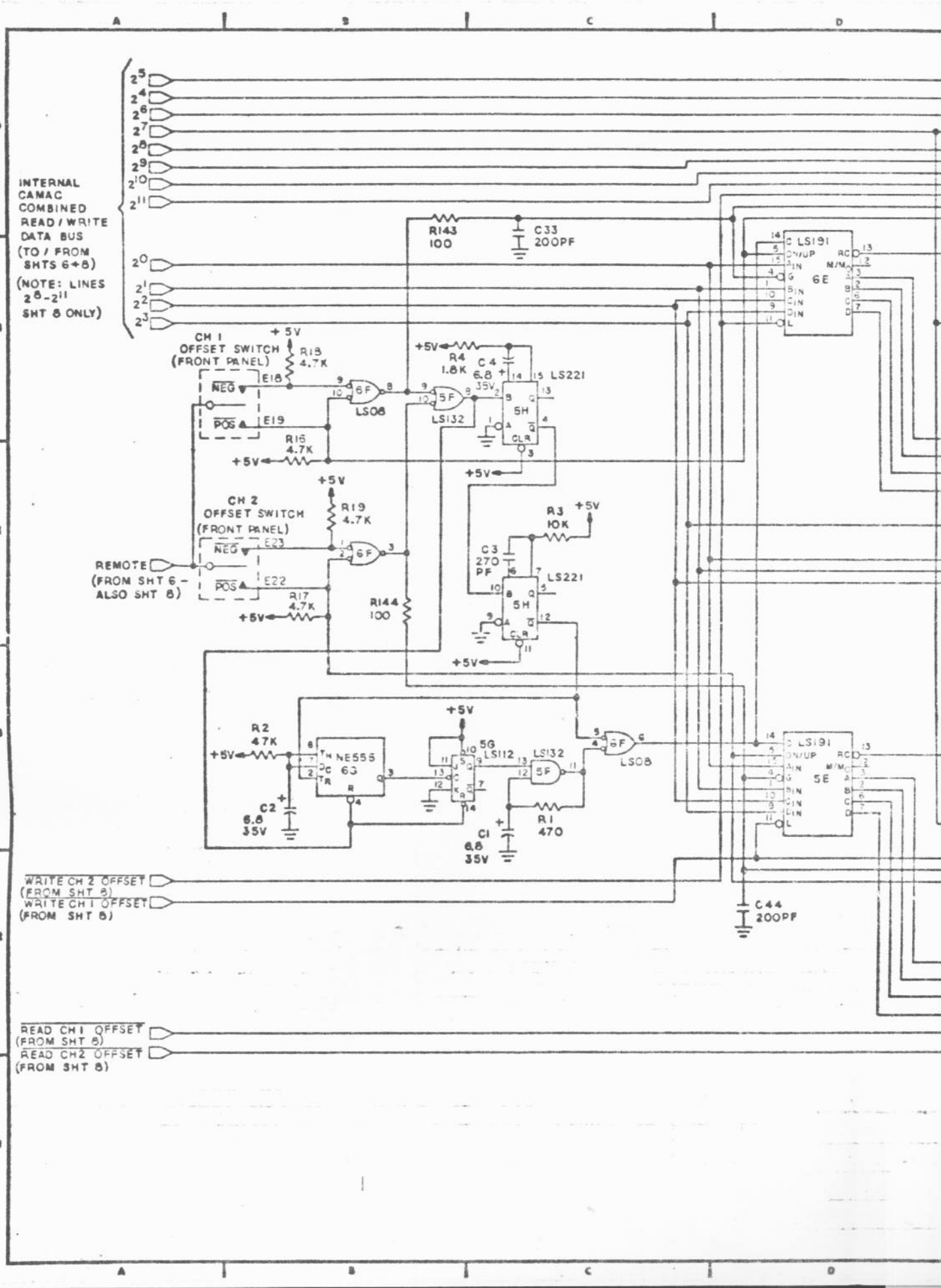
LeCroy RESEARCH SYSTEMS	
DRAWN RTC	8100 AMPLIFIER
CHECKED	
DATE 5/79	
DRAWING NUMBER: 8100	SHEET 5 OF 8 — ECO NO 1004 DATE 5/79

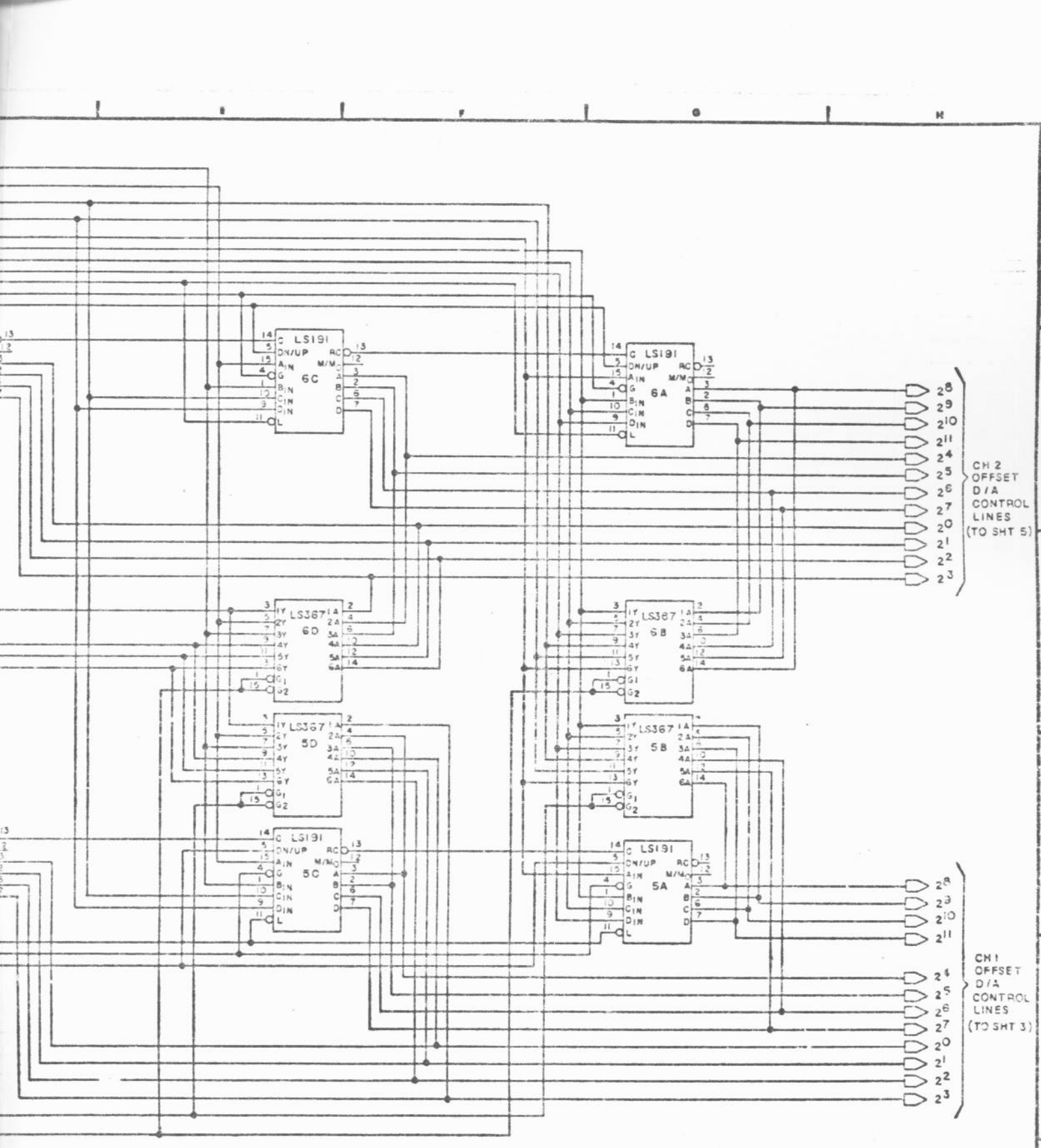

LATCH CH2 GAIN (FROM SHT 8)
R8
4.7K
+5V
9C
LS00
X.2
E10
CH. 2 MULT SWITCH (FRONT PANEL)
X1
E11
+5V
R11
4.7K
R9
4.7K
+5V
100
E13
CH. 2 GAIN SWITCH (FRONT PANEL)
1
E12
10
9C
8
LS00
R10
4.7K
+5V
+5V
R7
4.7K
FILTER IN/OUT SWITCH (FRONT PANEL)
IN
E9
READ CH2 GAIN (FROM SHT 8)
INTERNAL CAMAC COMBINED READ/WRITE DATA BUS (TO/FROM SHTS 7+8)
READ CH1 GAIN (FROM SHT 8)
INTERNAL CAMAC COMBINED READ/WRITE DATA BUS (TO/FROM SHTS 7+8)
R12
4.7K
+5V
9C
LS00
X.2
E14
CH. 1 MULT SWITCH (FRONT PANEL)
X1
E15
+5V
R15
4.7K
R13
4.7K
+5V
100
E17
CH. 1 GAIN SWITCH (FRONT PANEL)
1
E16
12
13
9C
11
LS00
R14
4.7K
+5V
(FROM SHT 8) ENABLE F.P. GAIN SWITCHES
LATCH CH1 GAIN (FROM SHT 8)
REMOTE (FROM SHT 8 - SEE ALSO SHT 7)



LeCroy RESEARCH SYSTEMS

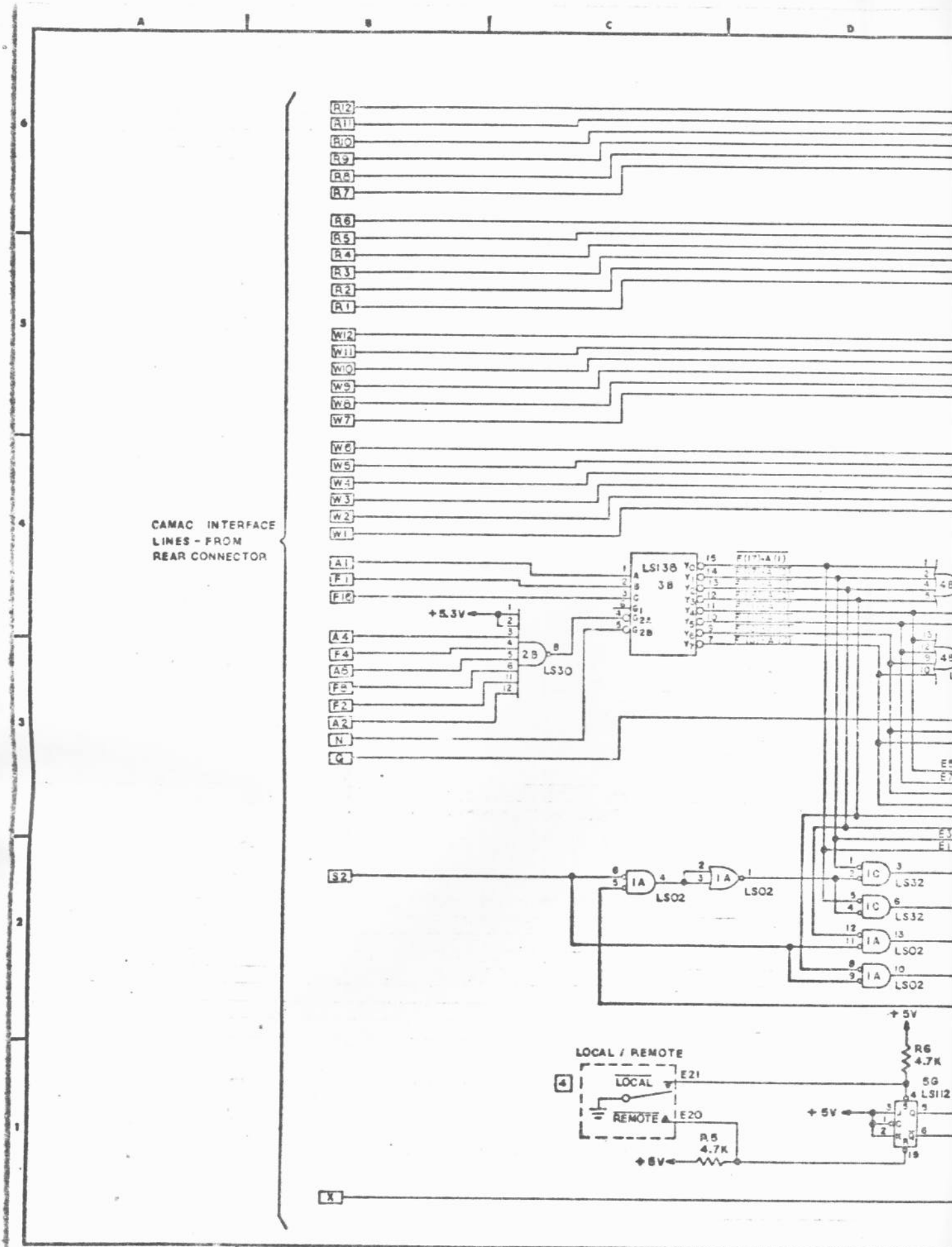
DRAWN RTC	8100 AMPLIFIER
CHECKED PAK 6/6/79	
DATE 5/79	
DRAWING NUMBER 8100	SHEET 6 OF 8
ECO NO 1004 DATE 5/79	

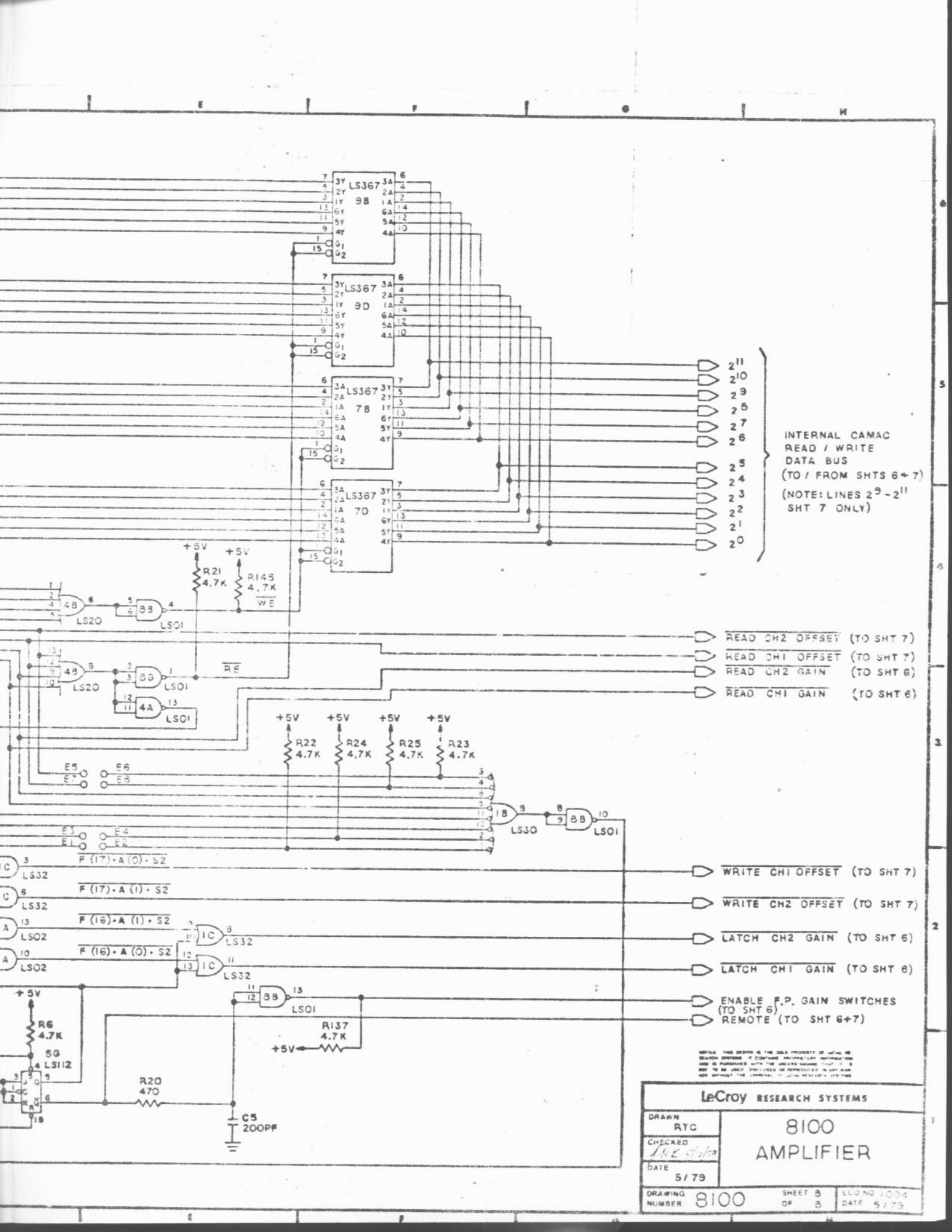

INTERNAL CAMAC COMBINED READ / WRITE DATA BUS (TO / FROM SHTS 6+8)
(NOTE: LINES 2^8-2^11 SHT 8 ONLY)
2^0
2^1
2^2
2^3
2^4
2^5
2^6
2^7
2^8
2^9
2^10
2^11
R143 100
C33 200PF
CH 1 OFFSET SWITCH (FRONT PANEL)
+5V
R18 4.7K
NEG
POS
E18
E19
R16 4.7K
6F
LS08
5F
LS132
R4 1.8K
C4 6.8 35V
LS221
5H
CLR
CH 2 OFFSET SWITCH (FRONT PANEL)
R19 4.7K
E23
E22
R17 4.7K
REMOTE (FROM SHT 6 - ALSO SHT 8)
R144 100
R3 10K
C3 270 PF
R2 47K
NE555
C2 6.8 35V
5G
LS112
C1 6.8 35V
R1 470
LS191
6E
5E
C44 200PF
WRITE CH 2 OFFSET (FROM SHT 8)
WRITE CH 1 OFFSET (FROM SHT 8)
READ CH 1 OFFSET (FROM SHT 8)
READ CH2 OFFSET (FROM SHT 8)

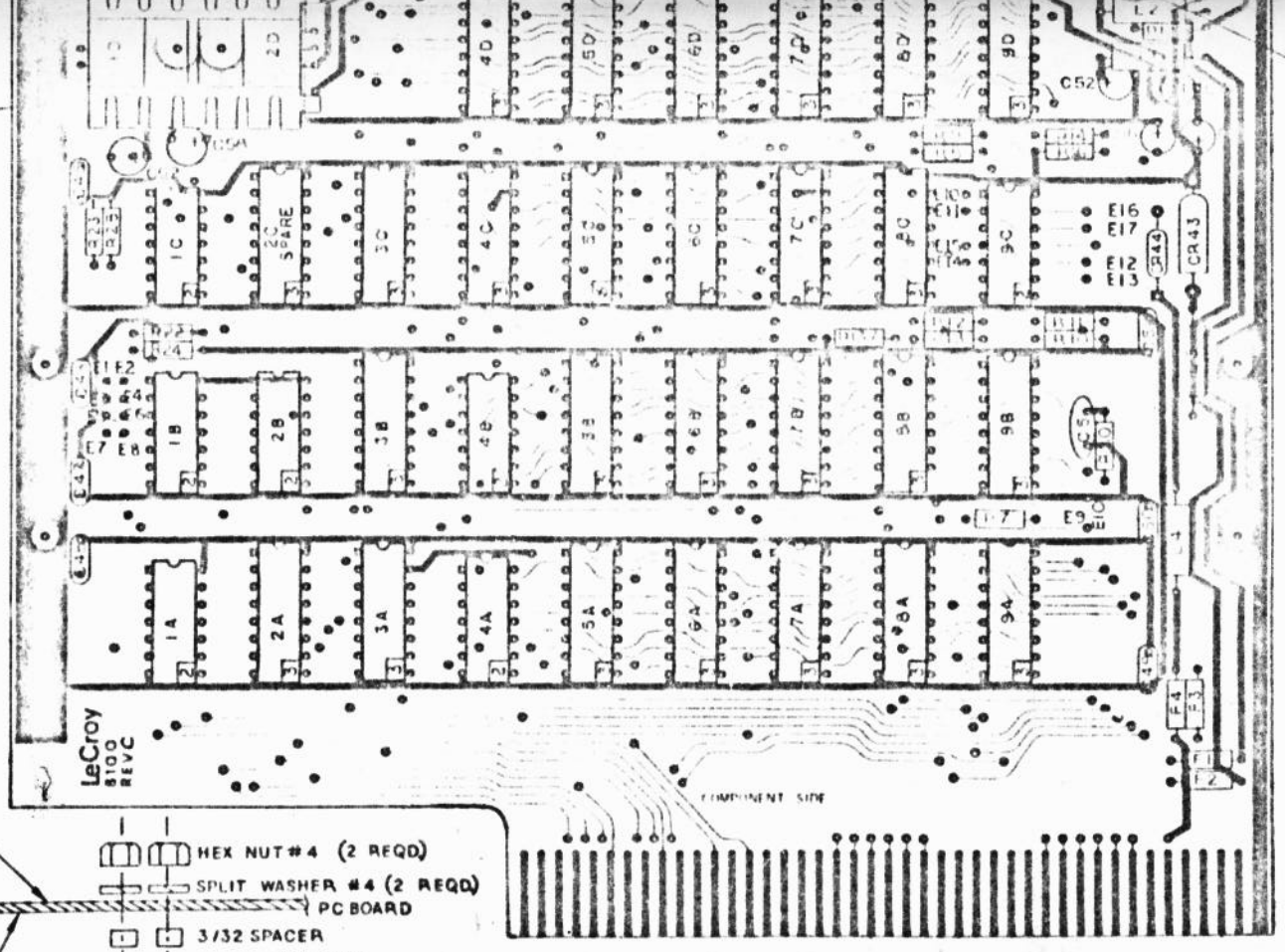


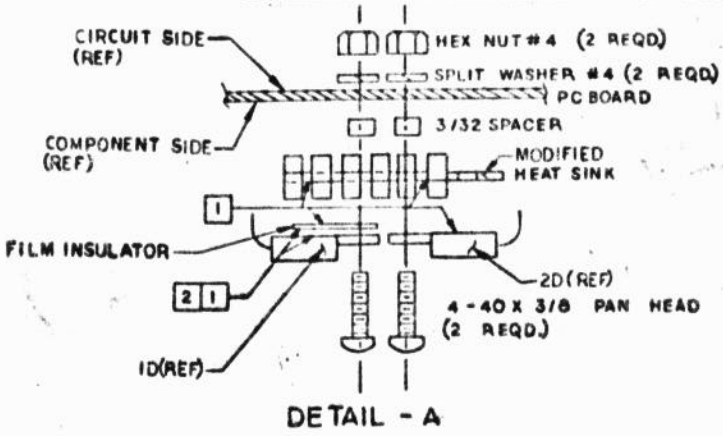
LeCroy RESEARCH SYSTEMS

DRAWN RTC	8100 AMPLIFIER
CHECKED RE 5/31/79	
DATE 5/79	
DRAWING NUMBER: 8100	SHEET 7 OF 8
ECO NO 1004 DATE 5/79	


CAMAC INTERFACE LINES - FROM REAR CONNECTOR
R12
R11
R10
R9
R8
R7
R6
R5
R4
R3
R2
R1
W12
W11
W10
W9
W8
W7
W6
W5
W4
W3
W2
W1
LA1
F1
F16
+5.3V
A4
F4
A5
F8
F2
A2
N
G
LS138
3B
2B
LS30
S2
1A
LS02
1C
LS32
+5V
R6
4.7K
LOCAL / REMOTE
LOCAL
E21
REMOTE
E20
R5
4.7K
+5V
5G
LS112
X


LS367 9B
LS367 9D
LS367 7B
LS367 7D
INTERNAL CAMAC READ / WRITE DATA BUS (TO / FROM SHTS 6 & 7)
(NOTE: LINES 2^9 - 2^11 SHT 7 ONLY)
R21 4.7K
R145 4.7K
WE
RE
READ CH2 OFFSET (TO SHT 7)
READ CH1 OFFSET (TO SHT 7)
READ CH2 GAIN (TO SHT 6)
READ CH1 GAIN (TO SHT 6)
R22 4.7K
R24 4.7K
R25 4.7K
R23 4.7K
LS30
WRITE CH1 OFFSET (TO SHT 7)
WRITE CH2 OFFSET (TO SHT 7)
LATCH CH2 GAIN (TO SHT 6)
LATCH CH1 GAIN (TO SHT 6)
ENABLE F.P. GAIN SWITCHES (TO SHT 6)
REMOTE (TO SHT 6+7)
R137 4.7K
R6 4.7K
R20 470
C5 200PF
LS112
LeCroy RESEARCH SYSTEMS
DRAWN RTC
CHECKED
DATE 5/79
8100 AMPLIFIER
DRAWING NUMBER 8100
SHEET 8 OF 8
ECO NO. 1004 DATE 5/79





DETAIL - A

NOTES: UNLESS OTHERWISE SPECIFIED

1. APPLY THERMAL COMPOUND EVENLY OVER THESE SURFACES.
2. BE SURE INSULATOR CLEARS POSITIVE REGULATOR OR POS REGULATOR WILL NOT MAKE PROPER CONTACT WITH HEAT SINK.

3. 1 DENOTES 8 PIN IC SOCKET
   2 DENOTES 14 PIN IC SOCKET
   3 DENOTES 16 PIN IC SOCKET
   4 DENOTES 24 PIN IC SOCKET

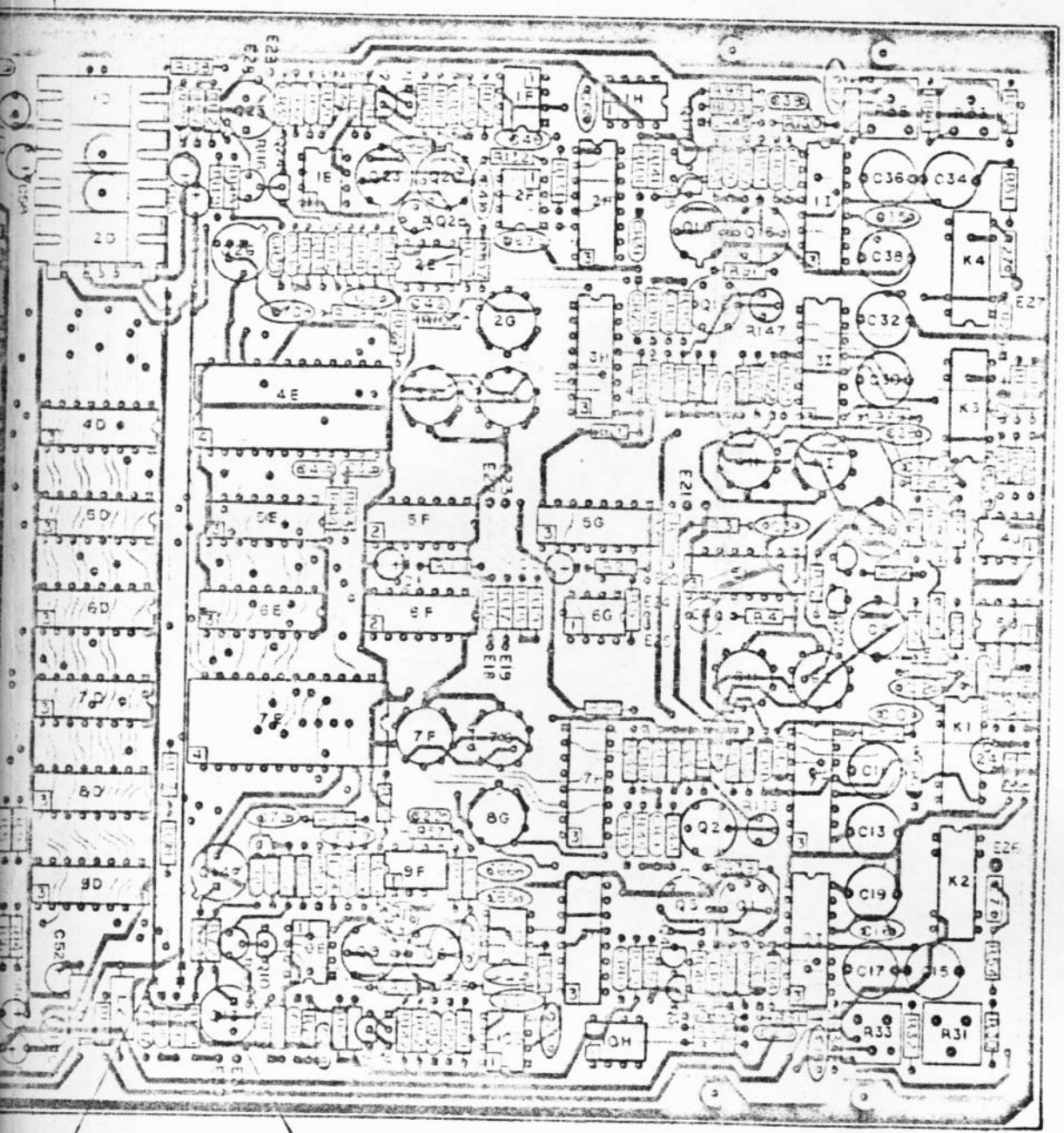
LeCroy	
MODEL: 8100	SCREEN / SIDE: COMPONENT
SCALE: 2:1	ECO: 1002
DONE BY: LTR	DATE: 1-3-79

LeCroy RESEARCH SYSTEMS

AMPLIFIER
PCB ASSY
8100

818-100-011 1002

SEE DETAIL - A



MODIFIED BUSS BAR
(2 PLCS)

TRANSIPAD (4 PLCS)
XQ13, XQ14, XQ25, XQ26