CICADA ENGINEERING SPECIFICATION	DOCUMENT NO. TFTR-10B3-H304A	
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	DATE- 9/7/78	
SUBJECT: Digital Output (Optoisolators)	PREPARED BY: J. Bosco / J. Bosco	

APPROVED BY

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REVISIONS

DATE	DESCRIPTION
9/7/78	Rev. A as noted on pages 4, 7 and 15.

1.0 Abstract

The purpose of this specification is to define the characteristics of a single width CAMAC module with optoisolator outputs.

2.0 Reference Documents

2.1 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC) IEEE Std. 583-1975.

2.2 CAMAC - A Modular Instrumentation System for Data Handling AEC. TID-25875.

2.3 Printed Circuit Board Fabrication and Assembly Specification, Document TFTR-10A2-H54B.

2.4 Electronic Schematic Specification, Document TFTR-10A2-H55.

2.5 Reliability, Quality Control and Temperature Cycling, Document TFTR-10A2-H58.

3.0 Introduction

The module defined by this specification will serve as a CAMAC interface between elements of the TFTR and the CICADA computer system. This module will be housed in a CAMAC crate and will be controlled by the CAMAC Dataway. Data received from the Dataway will be used to control 16 output optoisolators. The optoisolator outputs will be used to control a variety of devices, for example, power supplies, valves and amplifiers.

4.0 Basic Features

4.1 This CAMAC module will contain 16 optically isolated open collector transistor outputs. The 16 outputs will be available on a standard 36 pin card edge connector at the rear of the CAMAC card and there will be two outputs from each transistor with no common connection. The output rating shall be a minimum of 28 volts DC at a current of 16 milliamperes. Transistor protection must be provided by the external circuitry.

4.2 The electrical components of this module are to be mounted on a high quality printed circuit board (see specification 2.3). Component placement shall be such as to minimize undesired electrical coupling.

4.3 The transistor outputs will be controlled by Dataway commands. The mode of operation will be determined by the position of two manual switches. The switches are to be located on the module but must not be accessible from the front panel. One switch will either select a momentary or latched mode for the outputs. The momentary time interval will be 300 milliseconds and the latched state is maintained until a new command or reset is received. The second switch will select one of the following three conditions: (1) all 16 transistors normally open, (2) all 16 transistors normally conducting, or (3) 8 transistors normally open and 8 normally conducting. The normally open or normally conducting condition is defined as the state of the transistor with power applied after a Dataway clear or initialize command. With power off, all 16 transistors must be in the normally open state. During module power-up, all 16 transistors must be automatically initialized to the normal state, taking into account the setting of the second switch described above.

4.4 The module must respond in the same way to Dataway commands whether it is in the momentary or latched state except that Selective Clear (Command #2 below) will have no effect on the transistors in the momentary mode.

4.5 The states of the transistors will be controlled by Dataway lines W1-W16 and the appropriate command. When the condition of 8 normally open, 8 normally closed transistors operating mode is selected, the 8 normally open transistors will be controlled by lines W1-W8 and the 8 normally closed transistors by lines W9-W16 and the appropriate command.

4.6 The commands which the module must respond to are listed below:

Command #	Code	Action
1	F(18)·A(0)	Selective set transistors 1 to 16
2	F(21)·A(0)	Selective clear transistors 1 to 16
3	C + Z	Set all transistors to normal condition
4	F(0)·A(0)	Outputs transistor states to Dataway lines R1-R16; outputs encoded switch settings on lines R22-R24
5	F(6)·A(0)	Outputs module identifying number on lines R1-R12; outputs encoded switch settings on lines R22-R24
6	F(16)·A(0)	Overwrite transistors 1 to 16 Command #6 is deleted. RA

5.0 Mechanical Characteristics

5.1 This module must conform to the mechanical requirements outlined in reference specifications 2.1 and 2.2.

5.2 The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA type FR-4 or equivalent. See reference specification 2.3.

5.3 This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate. See reference specifications 2.1 and 2.2.

5.4 All components are to be identified with a standard manufacturer's part number or standard method of marking (e.g., resistor color coding).

5.5 All electrical components are to be mounted on only one side of the board.

5.6 The condition of this module is to be monitored by LED's which can be viewed from the module front panel. See Figure 10.1 for the suggested front panel layout. The front panel must be of aluminum and both sides are to have an iridite (conducting) finish. The color of the letters shall be chosen to contrast with the iridite finish and may be engraved or silk screened.

5.7 The 36 pin card edge connector must mate with a Viking 3V18 connector (or equivalent). The card edge connector must be marked with pin 1 on top and pin 18 on the bottom on each side of the card. It is not necessary to mark each pin.

5.8 All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part number on the electrical schematic associated with this module. See reference specification 2.4.

6.0 Electrical Characteristics

6.1 This module must conform to the electrical requirements outlined in reference specifications 2.1 and 2.2.

6.2 Whenever possible, low power circuitry (such as the 74LS series) shall be used to minimize power dissipation.

6.3 The module must derive its input from the standard $\pm$24 volt and $\pm$6 volt CAMAC supply voltages.

6.4 The +6 and -6 volt supply voltages must be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages must be bypassed with electrolytic capacitors of at least 6.8 microfarads. In addition, at least half the integrated circuits must contain a ceramic bypass capacitor of at least .01 microfarads on their supply voltage lines. The .01 microfarad capacitors should be located as close as possible to the integrated circuits.

6.5 All inputs to this module which come through the Dataway shall follow the input characteristics defined in references 2.1 and 2.2.

6.6 The output transistors shall be capable of switching 28 volts DC at 16 milliamperes. When open, the leakage current through the transistors must be less than 30 microamperes at rated voltage over the full temperature range. When closed carrying 16 milliamperes, the transistor output voltage must be less than 0.5 volt over the full temperature range.

6.6.1 Any transistor output shall be capable of withstanding a minimum of 300 volts to any other transistor output, to the isolator input or to ground. The isolator input to output resistance shall be a minimum of 10^{10} ohms. The isolator input to output capacitance shall be a maximum of 5 picofarads.

6.6.2 Circuitry external to the module shall limit the output voltage to a maximum of 30 volts.

6.7 The condition of the transistor outputs is under the control of data transferred into the module from the Dataway. The transistor outputs must be valid i.e., fully open or closed within a maximum of 20 microseconds after being commanded from the Dataway. A typical optoisolator circuit to satisfy the requirements of paragraphs 6.6 and 6.7 is shown in Figure 10.2.

6.8 The CAMAC commands listed in section 4.6 are described in detail below.

6.8.1 Command #1 (Selective Set) F(18)·A(0)

This command must activate the affected transistors to the state opposite from their normal position, i.e., a normally open transistor is closed and a normally conducting transistor is opened. The transistors that are affected are those for which the corresponding write (W) line is a logical "1".

If the module has been selected to be in the latched mode, the transistor conditions established by the Selective Set command must be maintained until an Overwrite, Selective Clear, Clear or Initialize command is received. If the module has been selected to be in the momentary mode, the affected transistors must momentarily activate the desired state once and only once for each Overwrite or Selective Set command. The momentary activation time is defined as having a value of 300 milliseconds with a tolerance of $^{-0}_{+20\%}$. It shall be possible to activate individual transistors independent of the state of other transistors. The transistors will be activated through Dataway commands which can occur at a maximum rate of one command every twenty (20) microseconds. In the momentary mode the activation time of three hundred (300) milliseconds for an individual transistor shall not be affected by the state of other transistors.

6.8.2 Command #2 (Selective Clear) F(21)·A(0)

This command must return affected transistors to their normal state. The affected transistors are those for which the corresponding write (W) line is a logical "1". This command will have no effect on the transistors in the momentary mode.

6.8.3 Command #3 (Clear or Initialize) C+Z

These commands must set all transistors to their normal state as defined by the position of the mode switch. This command will be automatically generated when the module is powered on.

6.8.4 Command #4 (Read Register) F(0)·A(0)

This command gates the transistor state on read lines R1-R16 in a one to one correspondence. The point to be read is the isolator input and not the transistor output. A read line which returns a logical "1" in response to this command is defined as presently having the corresponding transistor in the activated state, i.e., a normally open transistor is conducting and a normally conducting transistor is open. If the module is in the momentary state, all read lines will return logical "0"'s to this command. See the description under 6.8.5 below for the assignment of lines R22 to R24.

6.8.5 Command #5 (Read Module Number & State) F(6)·A(0)

This command gates the module identification number (decimal 304, binary 000100110000) on the read lines R1-R12 with the LSB on R1. The selected module operating mode is to be encoded and gated onto read lines R22 to R24 as defined by the table below.

Condition	R22	R23	R24
Latched	1	X	X
Momentary	0	X	X
All 16 transistors normally open	X	0	0
All 16 transistors normally closed	X	0	1
8 transistors normally open; 8 normally closed	X	1	0

6.8.6 Command #6 (Overwrite Outputs) F(16)·A(0)

This command forces the transistor outputs to follow the data on the write lines, i.e., a logical "1" on a write line will force the corresponding transistor to go into a conducting state and a logical "0" on a write line will force the corresponding transistor to go into an open state. In the latched mode the transistors will maintain the state set by the overwrite command until another command is received. In the momentary mode the outputs will be activated only once for each overwrite command. Command #6 is deleted. RA

6.9 Q and X shall be returned as a logical "1" for all commands which the module is equipped to perform.

6.10 The module shall not generate or respond to CAMAC signals B, L or I.

6.11 The condition of the optoisolator inputs is to be monitored by 16 LED's mounted on the module front panel. The corresponding LED's will light for the duration of time that a transistor is energized. Five additional front panel LED's are to monitor the selected module condition as defined below:

LED #1: Lit in Latched condition; off otherwise

LED #2: Lit in Momentary condition; off otherwise

LED #3: Lit when 16 N.O. condition is selected; off otherwise

LED #4: Lit when 16 N.C. condition is selected; off otherwise

LED #5: Lit when 8 N.O. and N.C. condition is selected; off otherwise

One other LED will light whenever the module is addressed and be held on for a duration of approximately 200 milliseconds. All 32 LED's described are to have front panel labels with abbreviations acceptable.

6.12 All components on this module must have a MTBF rating as specified in reference 2.5.

7.0 Environmental Data

7.1 The module must operate over an ambient temperature range of 0 to +50°C.

7.2 The module must operate over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must operate, as defined, in the presence of an external magnetic field changing at a maximum rate of 100 gauss per second with a peak magnitude of 50 gauss in any direction.

7.4 The module must operate in a radiation environment of 1 rad/second (peak) with a total integrated lifetime dose of 1000 rad.

8.0 Safety

8.1 All components of this module must be of flame retardant material.

8.2 The desired failure mode is for the transistor outputs to be open.

9.0 Testing

9.1 The module shall undergo all tests normally performed by the Seller. A description of the tests performed on this module and the results obtained shall be furnished by the Seller. Successful performance of the tests in sections 9.1 and 9.2 does not relieve the Seller of the responsibility of certifying that all requirements specified herein are met.

9.2 In addition to the tests performed in section 9.1, the specific tests outlined in Table 10.1 shall be performed by the Seller. The table specifies the test conditions; the Seller is to provide the data in the test measurement column and the name of the person performing the test. The test measurements shall be made with instruments which have an accuracy of ±10% or better. The tests specified in Table 10.1 are to be performed after the module has undergone the temperature cycling test specified in reference 2.5. The module is to be mounted in a CAMAC crate and powered from the standard ±6 volt and ±24 volt CAMAC supply. The module function codes are to be tested on the CAMAC dataway through the use of a computer or manual test device which can supply appropriate data and timing. The dataway timing is to meet the conditions specified in reference 2.1. If the tests specified in Table 10.1 have already been performed as part of the Seller's normal tests, the results can be recorded in Table 10.1, i.e., the tests do not have to be repeated. All the tests must be successfully executed before the module will be accepted.

10.0 Quality Control

10.1 This equipment shall meet all applicable requirements specified in reference 2.5.

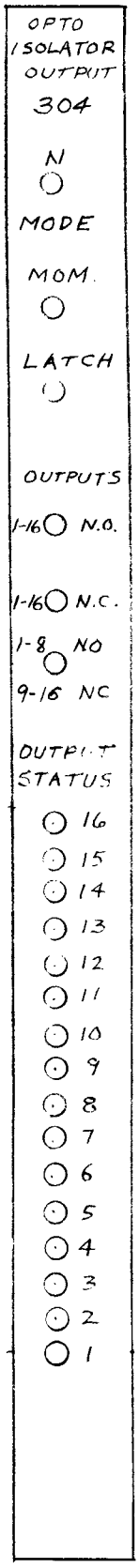

Fig. 10.1 Front Panel Layout

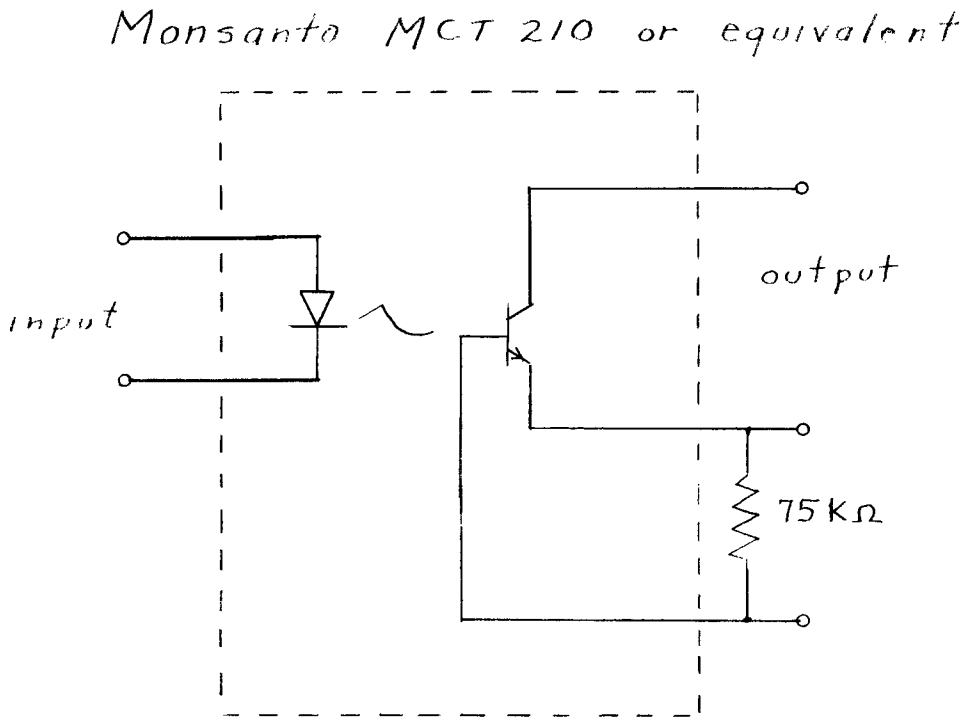

Fig. 10.2 Typical Opto Isolator

Test #	Reference Section	Test Condition	Test Measurement	Test Performed by
1	6.6	Transistors conducting and carrying 16mA DC. Each transistor is to be tested but only the highest output voltage is to be recorded.	Output voltage in volts	
2	6.6	Transistors open with 28 volts DC across them. Each transistor is to be tested but only the highest leakage current is to be recorded.	Leakage current in microamps	
3	6.6	Supply 30 volt, 10 microsecond pulses to open transistors. Each transistor to be tested but only highest current to be recorded.	Pulse current in milliamps	
4	6.6.1	Supply $\pm$300 volts DC from ground to a conducting transistor. Each transistor to be tested but only highest current to ground to be measured.	Current to ground in microamps	
5	6.6.1	Supply $\pm$300 volts DC from one conducting transistor sequentially to all other transistors and measure the current. Only the highest current need be recorded.	Transistor to transistor current in microamps	
6	6.7	Perform Selective Set command that causes a normally open transistor to conduct. Use latched mode. Measure the time from command initiation to full conduction. Each transistor to be tested but only longest time to be recorded.	Time in micro-seconds	
7	6.8.1	Perform Selective Set commands in latched mode. Each transistor to be tested.	Do transistors function as specified? Yes--- No----	

Table 10.1 Tests

Test #	Reference Section	Test Condition	Test Measurement	Test Performed By
8	6.8.1	Perform Selective Set commands in momentary mode. Each transistor to be tested.	Does the command function as specified including activation times? Yes--- No----	
9	6.7 6.8.2	Perform Selective Clear command to each transistor.	Does the command function as specified? Yes--- No----	
10	6.8.3	Perform clear and Initialize functions for each of the three mode switch settings.	Does the command function as specified? Yes--- No----	
11	6.8.4	Perform Read Register command in Latch and Momentary modes.	Does the command function as specified? Yes--- No----	

Test #	Reference Section	Test Condition	Test Measurement	Test Performed By
12	6.8.5	Perform Read Module Number and State in Latched and Momentary Modes.	Does command function as specified? Yes--- No----	
13	6.8.6	Perform overwrite command in latched and momentary modes. This test is deleted.	Does command function as specified? Yes--- No----	RA

OUTPUT CONNECTOR

Outputs are at a rear card edge connector located above the dataway connector. Mate is Viking 3V18 or equivalent. "R" designation denotes RIGHT side of the board when viewing the front of the module; pin 1 at the upper left, 1R is the upper right. The outputs and corresponding pin numbers are as listed.

Output		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
P2 Pin	Col(L)	3	11	4	12	5	13	6	14	7	15	8	16	9	17	10	18
Number	Emit(R)	3	11	4	12	5	13	6	14	7	15	8	16	9	17	10	18

Opto Isolator Rear Panel output orientation
Note: Collector must be + with respect to Emitter.
"L" is designated by a "B" on the Viking Connector
"R" is designated by a "A" on the Viking Connector

Princeton University: PPPL Computer Division

To: W. Rauch

Date: July 14, 1987

From: J. Wertenbaker

Subject: 304 Power-up Problem

The power-up reset feature of the 304A module from Bi-Ra has been found to be inadequate. The problem is a momentary activation of one or more outputs for about 750 milliseconds upon power-up. Out of the 30 modules that were tested for this problem, 11 showed it on a test bench. Their serial numbers are 1, 330, 333, 382, 383, 385, 386, 388, 389, 394, and 395.

The state of each output on the 304A is determined by 16 J-K flip-flops, U46-U53. Because when powered up they will come up in an indeterminate state, they must be cleared before their output can reach the opto-isolators. R1 and C1 are set up to trigger U3 750 milliseconds after power-up. U3 then outputs a pulse that clears all the flip-flops. The problem is that this is much too long for the outputs to be activated when they shouldn't be.

The crate controller also has something to do with it. A C or a Z will clear the outputs. The 3952 crate controller will output a Z within a second after power-up. However, it was found that the batches of 3952's previous to the serial number 2500, upon power-up, will output a glitch on the Z line that is just enough to clear the outputs on the 304A. About 1 second after power-up, it will output the Z properly. The batches after the serial number 2500 do not output this glitch, and therefore wait for about 1 second before the Z cycle happens. We currently have about 75 newer 3952's and 405 older ones. This means that most 304A's will not show the problem, because the majority of the 3952's are of the older generations. This is why the problem hasn't been noticed until now.

Jane Montague and I worked out a fix for the problem. Replace C1 with a 5K ohm resistor. Remove R1 and run a 1K ohm resistor from U3 pin 10 to the collector of Q2. The 5K ohm resistor will fit perfectly in C1's place, while the 1K resistor will have to be placed on the solder side of the board, between the pad below U3 where R1 was and the feed-through below S1. The leads of the 1K ohm resistor run over traces and must be insulated.

This circuit will work in conjunction with the power-down circuit already existing in the 304A. As the input voltage slowly rises, all the TTL chips will receive power before the output opto-isolators. Q1 and Q2 will remain off until the input voltage reaches about 5 volts. By that time, all the TTL chips are working. Above 5 volts, Q1 will turn on Q2, which will make power available to the opto-isolators, U4-U18. But, when the collector of Q2 rises above 1.7 volts, U3 triggers, clearing the outputs. While in theory there seems to be a race condition between the opto-isolators activating and the clear signal de-activating the opto-isolators, it is the best solution that can be found without re-designing the board. One module was modified and tested, and a glitch on the output was seen, but it was less than 50 microseconds in length and it was not clear as to whether or not it was induced through the power line.