

**CICADA
ENGINEERING
SPECIFICATION**

DOCUMENT NO.
TFTR-10B3-H321

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DATE - 10/7/80

SUBJECT
8 Channel D/A

PREPARED BY

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APPROVED BY

CICADA MANAGER

PPL QUALITY CONTROL

TOKAMAK OPERATIONS MANAGER

DATA ACQUISITION MANAGER

TFTR DEPUTY PROJECT MANAGER

REVISIONS

DATE	DESCRIPTION
10/5/80	Unipolar conversion procedure added to page 2 New reference documents as per 2.6 and 2.7 New illustrations - Figure 4, 5, 6, and 7

1.0 Abstract

This specification sets forth the functional requirements of an 8 channel D/A module.

2.0 Reference Documents

2.1 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Standard 583-1975.

2.2 Printed Circuit Board Fabrication and Assembly Specification, Document No. TFTR-10A2-H54B.

2.3 Reliability, Quality Control and Temperature Cycling, Document No. TFTR-10A2-H58.

2.4 Electronic Schematic Specification, Document No. TFTR-10A2-H55.

2.5 Printed Circuit Artwork Specification, Document No. TFTR-10A2-H53.

2.6 "H321 D/A Modules", Memo PE-M-6064, dated 24 September 1980, J. Pollock.

2.7 Jorway Corporation, Drawing #1803-D-350, "Octal D/A Component Layout".

3.0 Introduction

The CAMAC module specified will be used as an interface between elements of the Tokamak Fusion Test Reactor (TFTR) and the Central Instrumentation, Control and Data Acquisition (CICADA) computer system. The module will be controlled by the CAMAC Dataway (reference document 2.1).

4.0 Basic Features

The module shall have a balanced differential analog voltage output corresponding in magnitude to the 12 bit digital input presented to that particular channel. The module will have eight (8) input channels and eight (8) corresponding output channels. The digital inputs for a given output channel will come from the Dataway. Selection of the output channel will be determined by the subaddress codes A0 through A7. The resolution of each D/A output will be 12 bits with a full scale differential output range of 10.24 volts line to line. (See Figure 2). The input to the module will be two's compliment code. The analog outputs will be presented at the auxiliary rear edge connector. The module shall have the added feature of unipolar operation by implementing specified modifications to the module as specified in Figures 4, 5 and 6. This defined procedure converts each D/A output channel into a dual unipolar output analog channel. One output yields positive voltages only, the other output yields negative voltages only. The full scale swing for each output shall be 10.2375 volts (.0025 volts/bit). The relationship of these outputs with respect to the hex data loaded into the output storage register is shown in Figure 4.

It must be pointed out that such modified modules shall be identified by placing a sticker on the module side panel of the module which states the following:

H321 D/A Module
Unipolar Outputs
Modified by _____ Date
Calibrated by _____ Date

The front panel of the modified module must bear a durable sticker with the initials "UNI" stamped or engraved on it. A "gravoply" type engraved label is acceptable.

It must be noted that it is not possible to mix bi-polar and unipolar outputs on the same module.

4.1 The module shall respond to the following commands:

1. F(0).A(*) Read D/A input register
2. F(6).A(0) Read the module identifying number on the dataway
3. F(16).A(*) Overwrite the D/A input register
4. Z + C Clears the D/A input registers

* = Subaddress 0 to 7

4.2 Outputs must be capable of supplying 10mA over the entire output voltage range. The output amplifiers must be capable of driving at least one hundred (100) feet of twisted pair cable.

4.3 The module will generate a Q and X = 1 signal for commands the module is equipped to process.

4.4 The front panel will include a "N" indicator lamp that will flash on for 200ms when the module is addressed.

5.0 Mechanical Characteristics

5.1 The module will be single width (1x) and will be housed in a CAMAC module frame for insertion into a CAMAC crate.

5.2 The module shall conform to the mechanical specifications as specified in document 2.1.

5.3 The components are to be mounted on only one side of the board and are to be identified with a manufacturer's standard part number or other RETMA markings.

5.4 The 36 pin card edge connector (auxiliary connector) must mate with a Viking 3V18 connector or equivalent. The card edge connector on the module must be marked with pin 1 on the top row and pin 18 on the bottom row.

5.5 All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part number on the electrical schematic associated with this module. See reference document 2.4.

6.0 Electrical Characteristics

6.1 The input power shall be derived from the standard +6 volt and +24 volt CAMAC supply voltages. Whenever possible, low power logic circuitry (such as 74LS series) shall be used to minimize power consumption and dissipation.

6.2 It is recommended that the +5 and ground lines for the TTL logic shall be carried on sandwich type busses which are located underneath the dual-in-line packages.

6.5 CAMAC Commands

6.5.1 Command #1 Read Output Register [F(0).A(*)]

This command transfers the status of the output register designated by a (*) onto R1 through R12 of the read lines of the Dataway. The range of (*) is 0 to 7. R1 is the least significant bit, R12 is the most significant bit of the output register.

6.5.2 Command #2 Read Module Identifying Number [F(6).A(0)]

This command gates the identifying number (decimal 321, binary 101000001) onto the read lines of the dataway R1 through R9.

6.5.3 Command #3 Overwrite the Output Register [F(16).A(*)]

This command transfers the data on the write lines of the Dataway to the output register designated by the subaddress A(*). The data transfer takes place on strobe signal S1. The write lines used for data transfer for this command are W1 through W12. (LSB is on W1). There are eight (8) output registers; one for each D/A converter on the module.

6.5.4 Z+C Clear Input Registers

This dataway signal resets the D/A input registers and causes the outputs to assume a zero volt level.

6.6 Module Parameters

6.6.1 Linearity: ± 1 least significant bit (LSB) maximum deviation.

6.6.2 Error due to temperature variation over the 0° to 50°C range: $\pm 2\%$ range.

6.6.3 Settling time shall be less than 4 microseconds to within $\pm 1\text{LSB}$ of final value.

6.6.4 Temperature coefficient: $+50\text{ppm}/^{\circ}\text{C}$ maximum.

6.6.5 Output deviation due to power supply output. Variation shall be less than $\pm 0.01\%$ full scale per 1% power supply variation.

6.6.6 Long term stability of any channel shall be $\pm 0.1\%$ over one year at 25°C .

6.7 Output Range

The module will have a bi-polar output range of -10.24 volts to $+10.235$ volts, ± 2.5 millivolts each at 25°C for each channel.

6.7.1 The analog output shall be within ± 2.5 millivolts of zero (0.0) volts for a binary input of 0000 0000 0000 at 25°C .

6.7.2 The analog output shall be 10.235 volts, ± 2.5 millivolts for a binary input of 0111 1111 1111 at 25°C .

6.7.3 The analog output shall be -10.240 volts, ± 2.5 millivolts for a binary input of 1000 0000 0000 at 25°C .

6.7.4 The output vs binary input function for all of the D/A channels is illustrated in Figure 2.

7.0 Environmental Data

The module must be capable of operating, as defined, under the following conditions:

7.1 Temperature range 0 to +50°C.

7.2 Humidity range 10% to 90% (relative).

7.3 Magnetic field $\frac{d\phi}{dt} \leq 100$ gauss/sec

$$-50 \text{ gauss} < \phi < +50 \text{ gauss}$$

7.4 Radiation Intensity: ≤ 1 rad/sec peak

Cumulative Dose: 1000 rad maximum

8.0 Safety

8.1 All components of this module must be of flame retardant material.

8.2 Upon power turn on, the analog outputs must assume a zero volt level within 1 LSB of zero volts (+2.5mv) at 25°C.

9.0 Testing

9.1 The module shall undergo all tests normally performed by the seller.

A description of the tests to be performed shall be furnished by the seller.

The tests should include those listed in Table 11.1.

9.2 The tests shall be performed with digital test equipment with an accuracy of +0.01% full scale. The module under test must be tested in a CAMAC crate equipped with +6 volts and +24 volts supplied via a standard CAMAC power supply.

The module command codes are to be tested functionally with commands from the Dataway in conjunction with a terminal or other device capable of supplying appropriate data and timing. The tests in Section 10.1 are to be performed after the module has undergone tests outlined in reference 2.3.

The Dataway signals and timing must meet the conditions specified in reference 2.1.

If the tests in 11.1 have been performed as normal procedure by the seller, they do not have to be repeated, but results must be recorded. Tests will be performed after temperature cycling.

10.0 Quality Control

10.1 The module specified herein must meet the requirements in reference 2.3.

Test Number	Reference Section	Test Condition	Test Measurement	Test Performed By
1	8.2	<p>With the module operating in a CAMAC crate at an ambient temperature of 25°C, the following tests must be performed, in addition to those normally performed by the vendor. Measurements should be made with a Digital Voltmeter (DVM) with a resolution of 100 microvolts maximum. Error of the DVM must be <u>±</u>.005% maximum.</p>	Differential output in volts DC	
2	6.7	<p>Apply power to the module. Measure and record the analog output for all 8 channels. All outputs must be within <u>±</u>2.5 millivolts of zero volts for acceptance.</p>	Differential output in volts DC	
3	6.7	<p>Measure and record the analog output for all 8 channels. With a data input of 0111 1111 1111 (07FF₁₆) to each channel. Each output must be within <u>±</u>2.5 millivolts of <u>±</u>10.235 volts for acceptance.</p>	Differential output in volts DC	
4	6.6.3	<p>Measure and record the analog output for all 8 channels with a data input of 1000 0000 0000 (0800₁₆) to each channel. Each output must be within <u>±</u>2.5 millivolts of -10.240 volts for acceptance.</p> <p>Settling time test. Measure and record the time required to change the analog output of each channel from zero to full scale voltage at each polarity. Record the elapsed time required for each output to settle to within <u>±</u>1LSB (least significant bit) of full scale for both polarities (<u>±</u>).</p> <p>Elapsed time shall be less than 4 microseconds at each channel for acceptance.</p>	Time in microseconds	

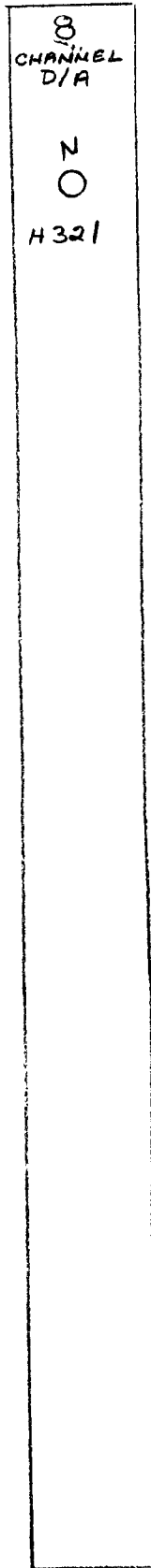
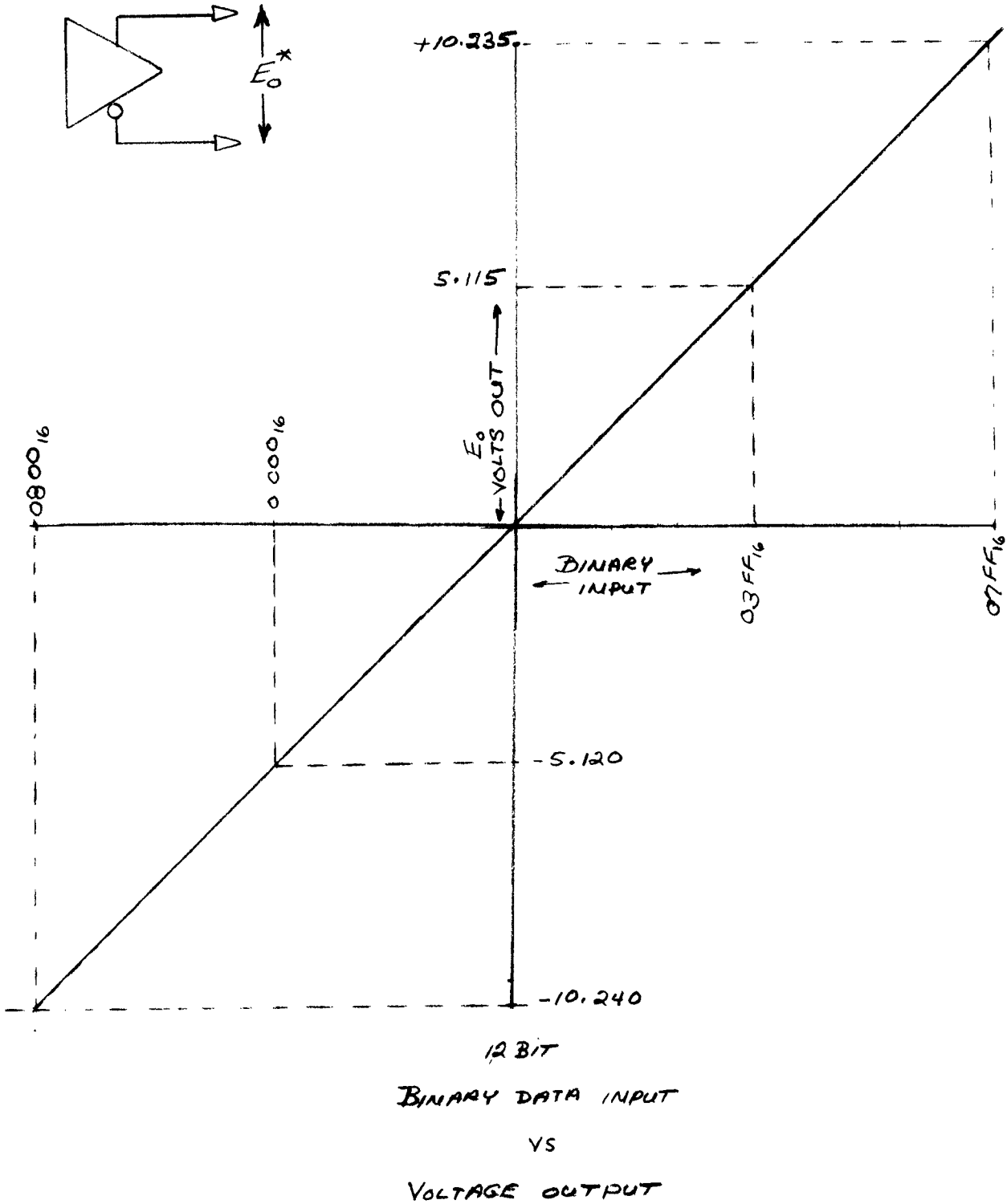


Figure 1

FRONT PANEL LAYOUT, 8 CHANNEL D/A MODULE



* MEASURE WITH RESPECT TO THE
INVERTED OUTPUT.

Figure 2

Auxiliary Rear Connector

Pin Allocations

(front view of crate)

	<u>+/- 10 Volts Pinout</u>		<u>0 - 10 Volts Pinout</u>	
	<u>Non-Inverted Output</u>	<u>Inverted Output</u>	<u>Non-Inverted Output</u>	<u>CAMAC Ground</u>
Channel 1	1B	1A	1B	9B
Channel 2	2B	2A	2B	10B
Channel 3	3B	3A	3B	11B
Channel 4	4B	4A	4B	12B
Channel 5	5B	5A	5B	13B
Channel 6	6B	6A	6B	14B
Channel 7	7B	7A	7B	15B
Channel 8	8B	8A	8B	16B

Analog Outputs

Figure 3



SUBJECT

H321 D/A MODULE
OUTPUT VS HEX DATA - UNIPOLAR

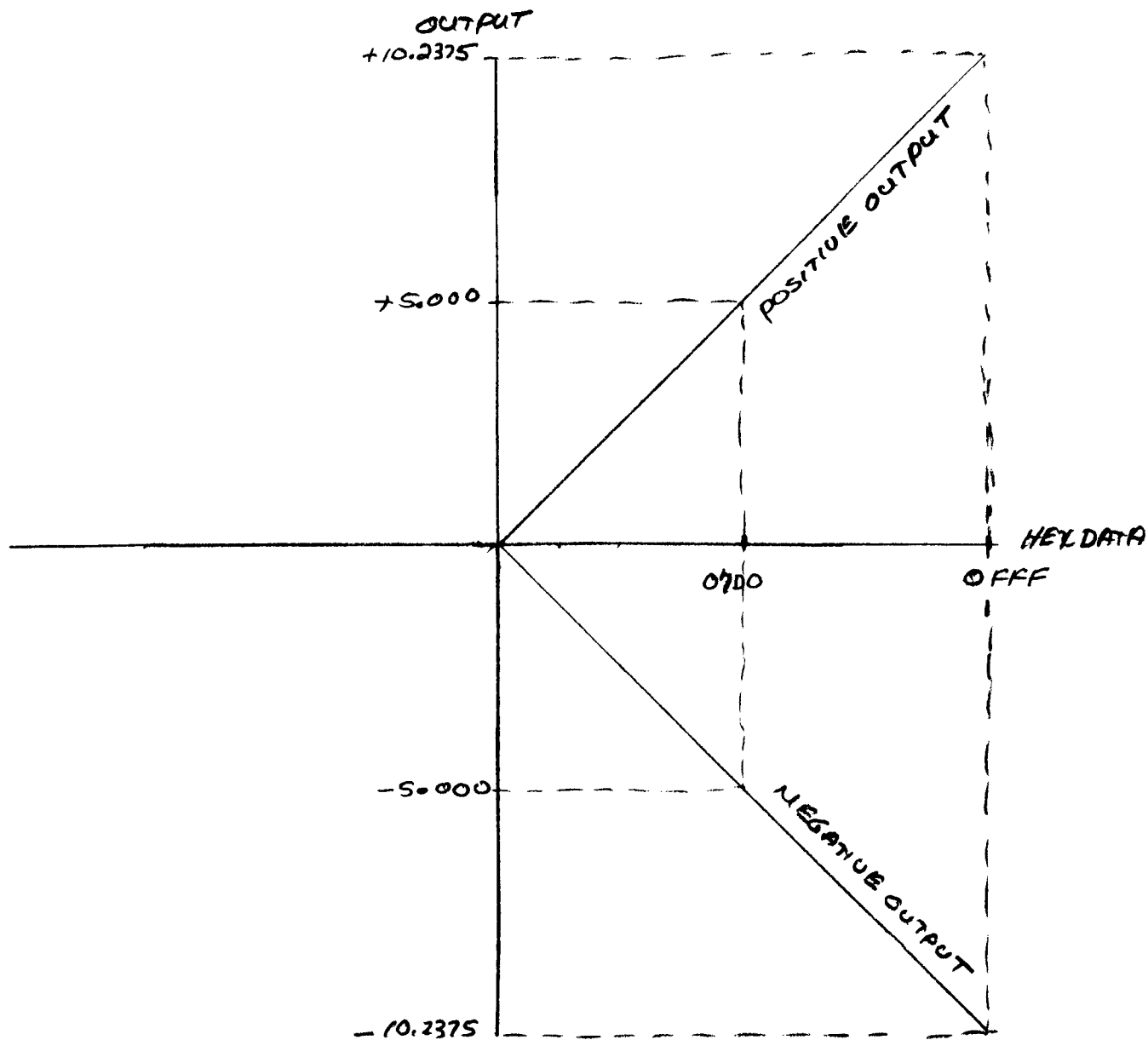
NAME

J. BLOCK

DATE

10-3-80

REVISION DATE



POSITIVE ONLY OUTPUTS ARE ON "B" AUX. CONNECTOR PINS
NEGATIVE ONLY OUTPUTS ARE ON "A" AUX. CONNECTOR PINS.

FIGURE 4



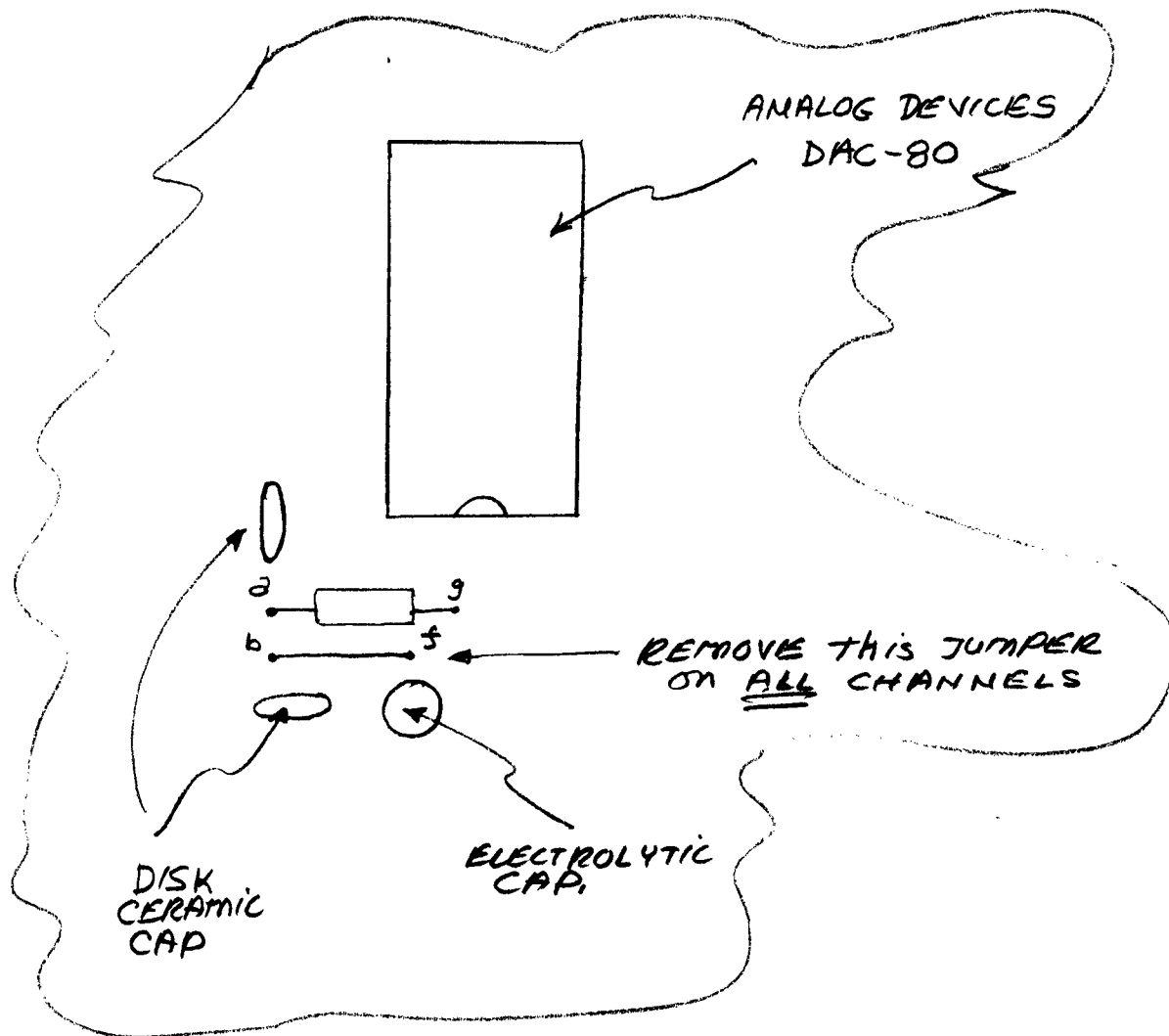
SUBJECT H321 D/A MODULE
BI POLAR TO UNIPOLAR CONVERSION

NAME J. POLLOCK

DATE 10-3-80

REVISION DATE

ITEM 4 IN FIGURE 7



NOTE:

NOT DRAWN
TO SCALE

LAYOUT SHOWN APPLIES TO ALL ANALOG OUTPUT CHANNELS.

FIGURE 5



SUBJECT

M321 D/A MODULE
BI-POLAR TO UNIPOLAR CONVERSION

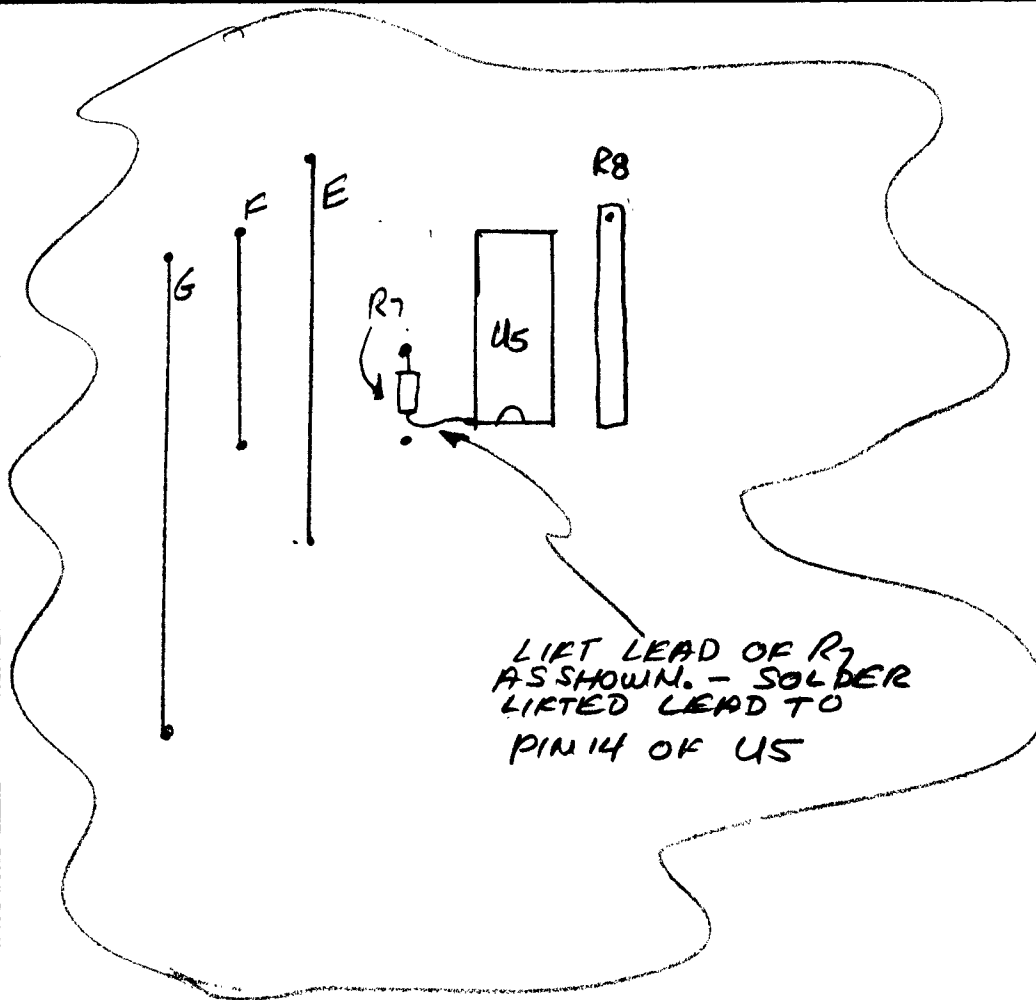
NAME

J. Pollock

DATE

10-3-80

REVISION DATE



SEE ITEM 3 IN FIGURE 7

FIGURE 6

BIPOLAR TO UNIPOLAR CONVERSION

1. Nand gate U2 has two (2) sections that must be bypassed. Remove pins 8 and 11 from U2 with precision cutters to avoid damage to the other IC pins. Remove the cut pins from the printed circuit board.
2. Prepare two (2) bare #22 jumper wires. Use one (1) jumper to short the pads for pins 12 and 11 together. Use the other jumper to short the pads for pins 8 and 9 together.
3. Lift the -6 volt end of R7 as per Figure 6 and solder it to pin 14 of U5.
4. Remove the "b" to "f" jumpers adjacent to each D/A (Analog Device DAC-80) as per Figure 5.
5. Ground pins 9B, 10B, 11B, 12B, 13B, 14B, 15B, and 16B to provide a separate ground pin for each channel.
6. Rezero and recalibrate each D/A channel using the F(16).A(*) command (see 6.5.3) to establish the otuput vs. HEX input relationship as per Figure 4.
7. Mark front panel with a "UN1" to indicate the module is strapped for unipolar operation.
8. See Figure 7 for suggested connection to the auxiliary connector.

Figure 7

