CICADA ENGINEERING SPECIFICATION

DOCUMENT NO. TFTR-10B3-H322

DATE- 9/24/79

SUBJECT: Digital Input Module, Voltage/Relay Contacts, Type 322

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TAC HEAD

REVISIONS

DATE	DESCRIPTION

1.0 Abstract

This specification, in conjunction with referenced documents, sets forth all characteristics of the subject module. The intended use of this document is to provide a minimum design goal for the module, as well as a working document for subsequent users.

2.0 Reference Documents

2.1 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Std. 583-1975.

2.2 CAMAC - A Modular Instrumentation System for Data Handling. AEC TID-25875.

2.3 Printed Circuit Board Fabrication and Assembly Specification, Document No. TFTR-10A2-H54B.

2.4 Electronic Schematic Specification, Document No. TFTR-10A2-H55.

2.5 Reliability, Quality Control and Temperature Cycling, Document No. TFTR-10A2-H58.

3.0 Introduction

The CAMAC module specified will be used as an interface between elements of the Tokamak Fusion Test Reactor (TFTR) and the Central Instrumentation Control and Data Acquisition (CICADA) computer system. The module will be housed in a CAMAC crate and will be controlled by the CAMAC Dataway (reference document 2.1). The module will monitor the status of discrete inputs (on/off devices) for conversion to computer compatible level and format.

4.0 Basic Features

The module shall be a single width CAMAC module and will interface to sixteen discrete input devices. Selective loading of components on the printed circuit board shall allow the module to accommodate either contact closure or input voltage sources. When loaded to serve as a voltage sensing input module, the module shall provide optical isolators between the input signal and the module circuitry. In response to CAMAC commands, the module shall be capable of operating as a digital input module and/or as a "maskable" change of state module. In addition, the module shall provide the circuitry to support a self test CAMAC command for the purpose of exercising the internal circuitry of the module.

4.1 Digital Input Feature

The module shall be capable of transferring the current status of its sixteen input ports to the CAMAC dataway during all modes of operation.

4.2 Change of State Feature

The module shall operate as a maskable change of state device with the capability of generating CAMAC LAM's. Two sixteen bit mask registers (M1 and M2), a LAM enable flag, a system arm flag and a sixteen bit "New Status Register" (NSR) shall be provided. Upon receipt of CAMAC command "System Arm" or "Clear LAM", the module shall transfer the data pattern of its sixteen input ports to the "New Status Register". The module will then perform the function, $F = (M1)(LS)(\overline{NSR}) + (M2)(\overline{LS})(NSR)$ as depicted in figure 11.1 on each bit of the system. Effectively mask M1 allows the function for positive transitions of Line Status (LS) and M2 allows the function for negative transitions of LS. When armed, the assertion of the function (F) shall cause a load of the data of the Line Status into NSR, and a clear of the "System Arm" bit. The NSR may be read from the dataway to provide the user with the Line Status following a non-masked input

transition. The module will be rearmed upon receipt of a "Read New Status" command to record subsequent changes. Upon being armed by the "Read New Status" the module may immediately reload the NSR if an additional non-masked state change(s) is present. The LAM flag, if enabled, will be set upon the occurrence of a non-masked state change and be cleared by "Clear LAM", "System Arm" or "Read New Status". A logic depiction of the LAM, NSR and Arm bit are shown in Figure 11.2. It should be noted that the New Status Register will be loaded with the Line Status Data in response to a "Clear LAM", "System Arm" or the occurrence of function (F) (when armed).

4.3 Self Test Feature

The module shall provide th e capability of simulating input signal conditions through the use of a dataway command. In response to the CAMAC self test command the module shall functionally switch the change of state logic circuits from the line status to drivers slaved to the CAMAC write lines. The trigger function "F" (summation of non-masked change of state sensors) shall be inhibited for sufficient time to allow all sixteen input drivers to stabilize prior to triggering down stream load signals. In all other respects the module will respond to the self test input pattern in the same way as to line status input.

5.0 Mechanical Characteristics

5.1 The module shall conform to mechanical specifications as indicated in reference 2.1 and 2.2.

5.2 The module shall be a single (1x) width CAMAC module.

5.3 The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA type FR-4 or equivalent.

5.4 This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate. See reference specification 2.1.

5.5 All components are to be identified with a standard manufacturer's part number or standard method of marking (e.g., resistor color coding).

5.6 All electrical components are to be mounted on only one side of the board.

5.7 The condition of this module is to be monitored by LED's located on the module front panel. See Figure 11.5 for the suggested front panel layout. All lettering on the front panel shall be either engraved or silkscreened. The front panel material shall be aluminum with an iridite finish with contrasting colored lettering.

5.8 The 36 pin card edge connector (auxiliary connector) must mate with a Viking 3V18 connector (or equivalent). The card edge connector must be marked with pin 1 on top and pin 18 on the botton on each side of the card.

5.9 All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part number on the electrical schematic associated with this module. See reference specification 2.4.

5.10 Auxiliary connector pin assignments shall conform to Figure 11.6.

5.11 The module printed circuit layout shall provide for selective loading of components to allow for operating characteristics as delineated in paragraphs 6.5.1-6.5.2. Components that are to be selectively loaded shall be mounted on printed circuit type sockets. The use of header type component mountings, for plug insertion into the sockets, is acceptable for non-standard component pinouts.

6.0 Electrical Characteristics

6.1 This module must conform to the electrical requirements outlined in reference specifications 2.1 and 2.2.

6.2 Input Power shall be derived from the standard $\pm$6 volt and $\pm$24 volt CAMAC supply voltages. Whenever possible, low power circuitry (such as the 74LS series) shall be used to minimize power dissipation.

6.3 The +6 and -6 volt supply voltages, if used, must be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages, if used, must be bypassed with electrolytic capacitors of at least 6.8 microfarads. In addition, at least half the integrated circuits must contain a ceramic bypass capacitor of at least .01 microfarads on their supply voltage lines. The .01 microfarad capacitors should be distributed on the board and be located as close as possible to the integrated circuits.

6.4 The use of insulated sandwich type busses for carrying the +5 volt and ground lines for TTL logic is strongly encouraged to provide noise suppression and to simplify printed circuit layout design.

6.5 The module input circuit shall be designed to allow the circuit board to be loaded to sense either contact closures or the presence of an external voltage source. (See Figure 11.3 for suggested input circuit).

6.5.1 When loaded for contact closure sensing the module design shall accommodate the use of contacts rated as follows:

maximum open circuit voltage	25 VDC
maximum closed circuit current	10 MA
maximum closed circuit resistance	50 Ohms

6.5.2 When loaded for source voltage sensing the module shall provide isolation between the external voltage source and the module circuitry. The input circuit shall provide a series current limiting resistor to allow selective loading for compatability with either 5 volt logic or for 24 volt logic. Optic coupler parameters shall conform, as a minimum, to the following characteristics:

Propagation delay, turn on and turn off	10μs maximum
Isolation voltage	1000 volts minimum

The module input circuit layout shall be designed to allow the circuit board to be selectively loaded for compatability with either 5 volt logic or 24 volt logic with the following characteristics.

	Input 24		Input 5	
	Max	Min	Max	Min
High Input	30 volts	20 volts	5 volts	2 volts
Low Input	4 volts	0 volts	0.5 volts	0 volts

The module input impedance shall be designed to sink a maximum of 10 milliamperes at nominal input voltage.

6.5.3 Self Test Circuitry

The self test feature of the module shall be implemented in a fashion as schematically delineated in Figure 11.4. System timing shall allow for data skew on CAMAC write lines by disabling the function (F) during all addressed CAMAC operations with the exception of time S1 of a self test cycle. It should be noted that the self test drives must be located downstream of the debounce circuit for speed compatability with the CAMAC dataway.

6.6 CAMAC Command Description

6.6.1 Command #1 Initialize or Clear [Z+C]

These commands shall reset the module to the following state:

LAM:	Clear and Disabled
ARM:	Disarmed
Mask M1:	Clear
Mask M2:	Clear
New Status Register:	Clear

6.6.2 Command #2 Read Module Number [F(6).A(0)]

This command gates the module identification number (decimal 322, hexidecimal 142) onto the dataway read lines R1-R12 with the LSB on R1.

6.6.3 Command #3 Read Line Status [F(0).A(0)]

This command gates the current status of the module 16 input channels onto the dataway read lines R1-R16. The logic convention shall be such that a contact closure (for contact sensing) or presence of voltage (for voltage sensing) shall be interpreted as a logic "1".

6.6.4 Command #4 Read New Status Register [F(1).A(0)]

This command gates the contents of the New Status Register onto the dataway read lines R1-R16. In addition, the command will clear the LAM bit (if set) and rearm the module.

6.6.5 Command #5 Read Mask M1 [F(1).A(1)]

This command gates the contents of mask register M1 onto the dataway read lines R1-R16.

6.6.6 Command #6 Read Mask M2 [F(1).A(2)]

This command gates the contents of mask register M2 onto the dataway read lines R1-R16.

6.6.7 Command #7 Clear LAM [F(10).A(0)]

This command clears the LAM (if set) and loads the Line Status into the New Status Register.

6.6.8 Command #8 Overwrite M1 [F(17).A(1)]

This command gates the data on write lines W1-W16 into mask register M1. The M1 register controls the internal function (F) and generation of LAM for line status changes going from logic "0" to logic "1". Channels are masked (ignored) by setting the appropriate bit to logic "0".

6.6.9 Command #9 Overwrite M2 [F(17).A(2)]

This command operates in the same way as command #8 for the M2 register for control of LAM on a logic "1" to logic "0" transition of line status.

6.6.10 Command #10 Selective Set M1 [F(19).A(1)]

This command selectively sets to logic "1" (enable function) bits of mask register M1. Bits affected are those for which the corresponding write line is a logical "1".

6.6.11 Command #11 Selective Set M2 [F(19).A(2)]

This command operates in the same fashion as command #10 for mask register M2.

6.6.12 Command #12 Selective Clear M1 [F(23).A(1)]

This command selectively sets to logic "0" (disable function) bits of mask register M1. Bits affected are those for which the corresponding write line is a logical "1".

6.6.13 Command #13 Selective Clear M2 [F(23).A(2)]

This command operates in the same fashion as command #12 for mask register M2.

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6.6.14 Command #14 Disable Arm [F(24).A(0)]

This command clears the module Armed Flag (if set). The contents of the New Status Register and the status of the LAM are not affected by this command.

6.6.15 Command #15 Disable LAM [F(24).A(1)]

This command inhibits the module LAM flag from being transmitted to the dataway.

6.6.16 Command #16 Enable Arm [F(26).A(0)]

This command sets the module armed flag, clears the LAM and loads the Line Status into the New Status Register.

6.6.17 Command #17 Enable LAM [F(26).A(1)]

This command allows the module LAM flag to be transmitted to the dataway.

6.6.18 Command #18 Self Test [F(20).A(0)]

This command functionally switches the module input buffers from the Line Status to buffered data from the dataway write lines W1-W16. The module will function as if a short duration bit pattern corresponding to the CAMAC "write" data had been sensed at the input. The module will perform all other functions (mask, LAM generation, etc.) in the same fashion as it normally operates while sensing Input Status. The effective utilization of this command requires that module be in the following state prior to the self test command.

NSR = Line Status

System "Armed"

LAM Clear

LAM Enabled (optional)

6.7 The module shall provide three (3) LED indicators mounted on the front panel. All indicators must illuminate for a minimum time of approximately 200 milliseconds. The indicators shall function as defined below:

LED #1	Lit when N is received
LED #2	Lit when LAM is enabled
LED #3	Lit when LAM is set

6.8 All components on this module must have a MTBF rating as specified in reference 2.5.

7.0 Environmental Data

7.1 The module must operate, as defined, over an ambient temperature range of 0 to +50°C.

7.2 The module must operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must not be affected by an external magnetic field changing at a maximum rate of 100 gauss per second with a peak magnitude of 50 gauss in any direction.

7.4 The module must operate, as defined, in a radiation environment of 1 rad/second (peak) with a total integrated lifetime dose of 1000 rad.

8.0 Safety

All components of this module must be of flame retardant material.

9.0 Testing

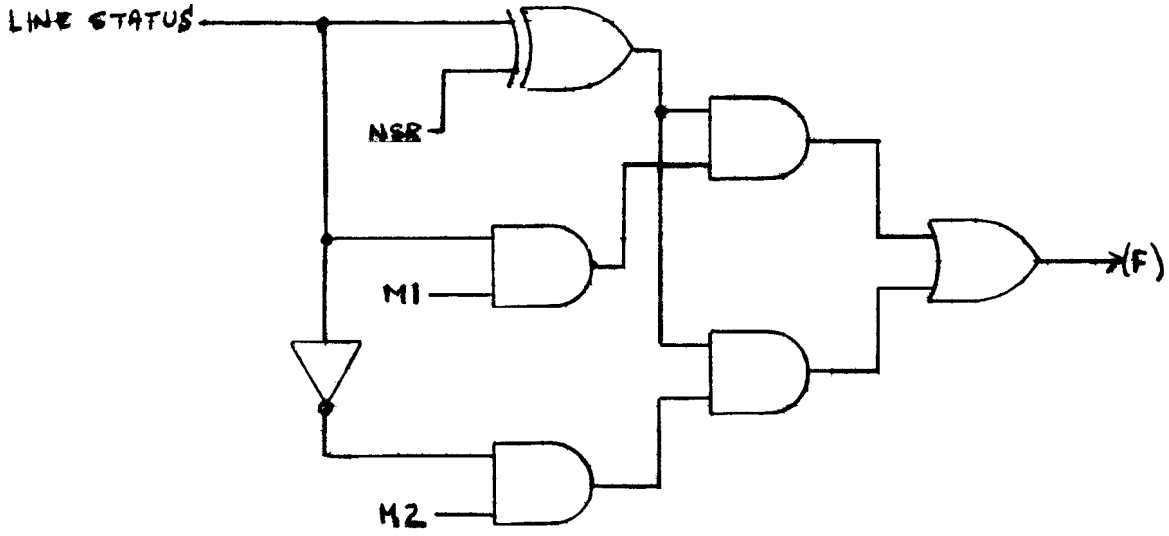
9.1 The module shall undergo all tests normally performed by the seller. A description of the test performed on this module and the results obtained shall be furnished by the seller. Successful performance of the tests in sections 9.1 and 9.2 does not relieve the seller of the responsibility of certifying that all requirements specified herein are met.

9.2 In addition to the test performed in section 9.1, the specific tests outlined in Table 11.7 shall be performed by the seller. The table specifies the test conditions; the seller is to provide the data in the test measurement column and the name of the person performing the test. Analog measurements required to perform the test shall be made with instruments which have an absolute accuracy of $\pm$1.0% or better.

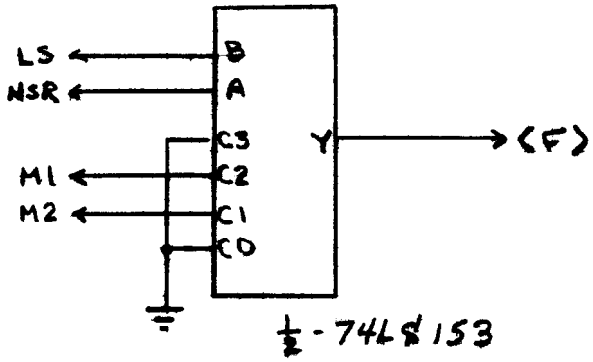
The procedure for testing of the module is given by Table 11.7. The module is to be mounted in a standard CAMAC crate. Commands to the module may be initiated through use of a computer or manual test device. "Line Status" input shall be compatable with the module input circuit (contact closure or suitable voltage).

10.0 Quality Control

10.1 This equipment shall meet all applicable requirements specified in reference 2.5.



LOGIC EQUIV. FUNCTION <F>

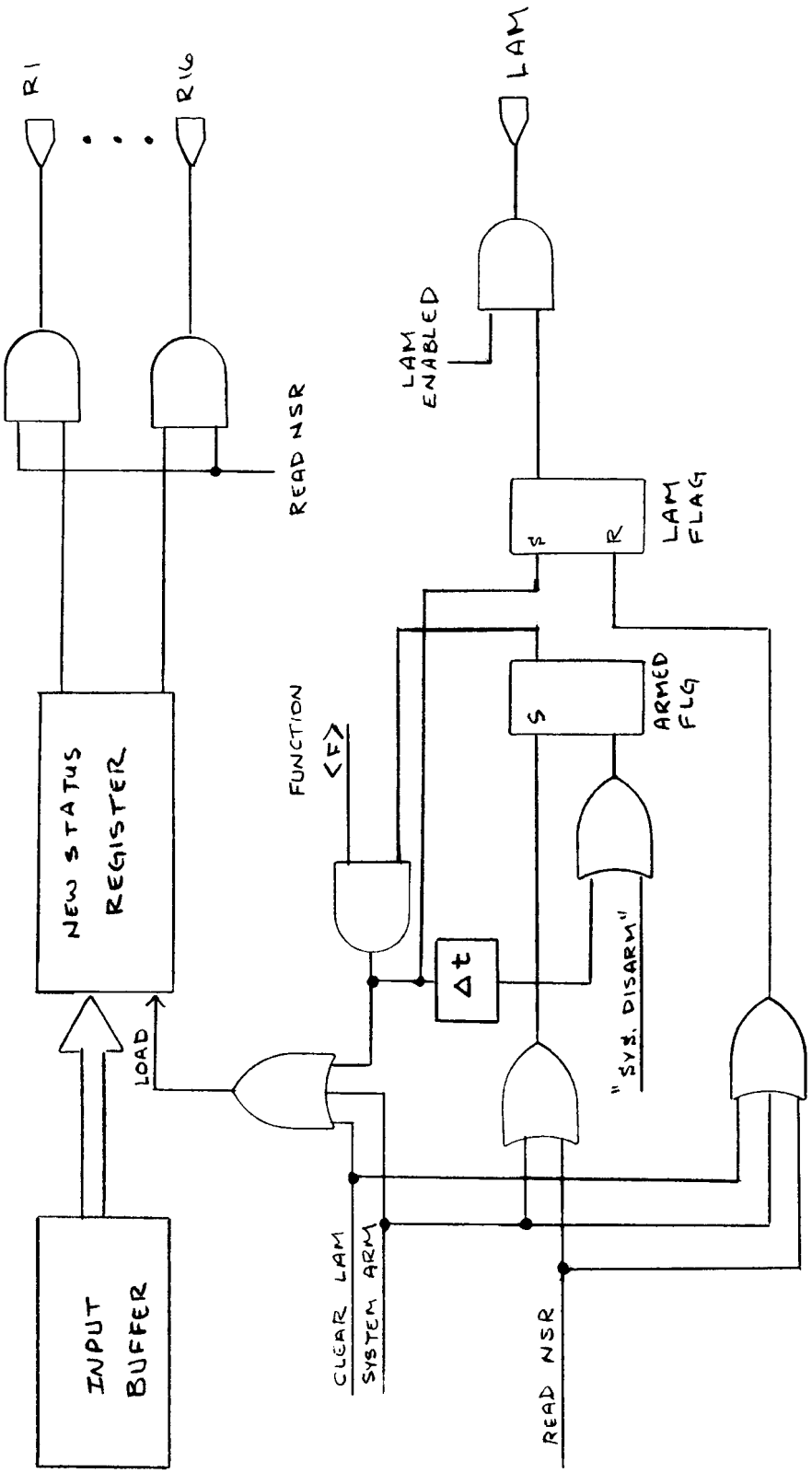


½ - 74LS153

SUGGESTED HARDWARE (F)

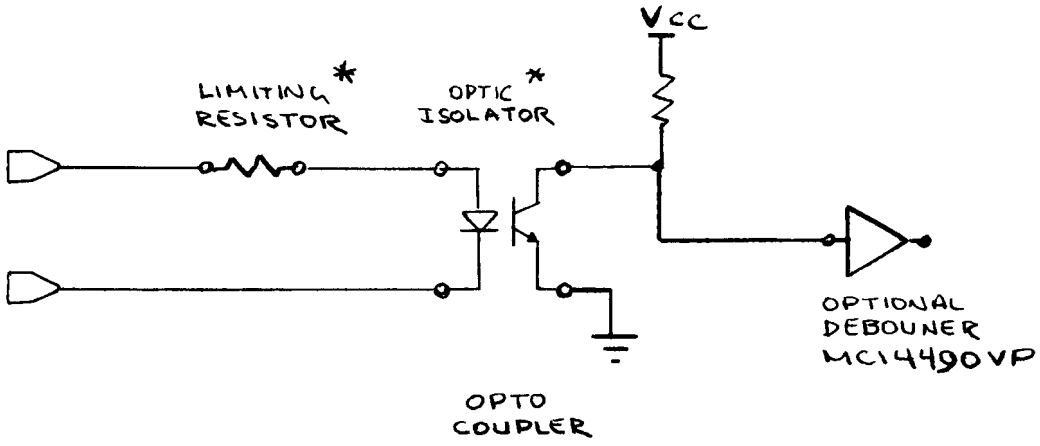
FUNCTION <F>

FIGURE 11.1

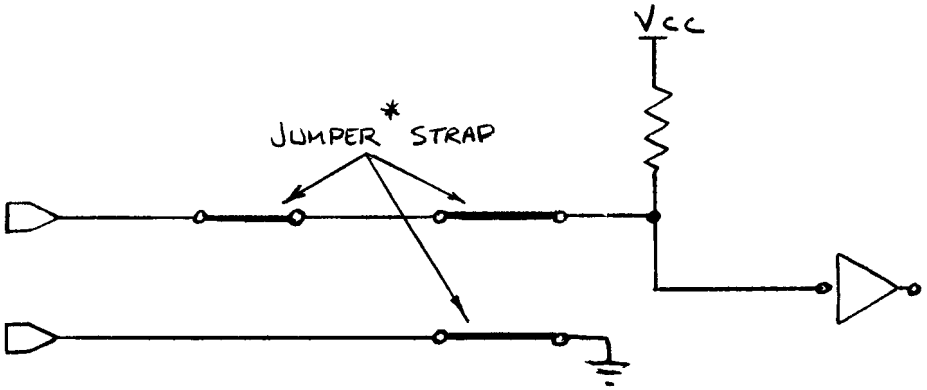


LOGIC DEPICTION
NEW STATUS REG, LOADING

FIGURE 11.2



VOLTAGE TYPE INPUT CIRCUIT

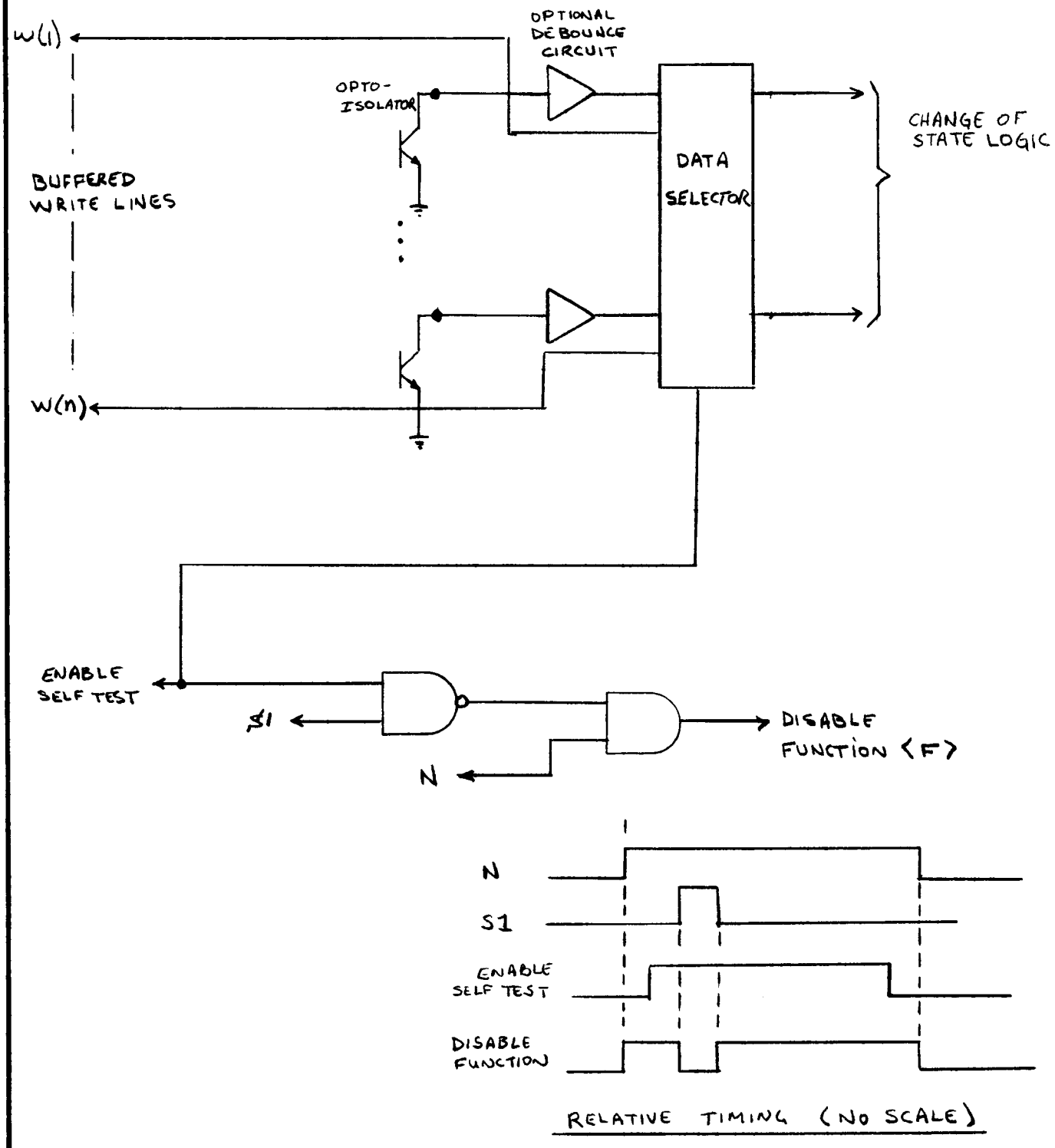


CONTACT TYPE INPUT CIRCUIT

* COMPONENTS SELECTIVELY LOADED - STRAPS OR LIMIT RESISTOR & ISOLATOR

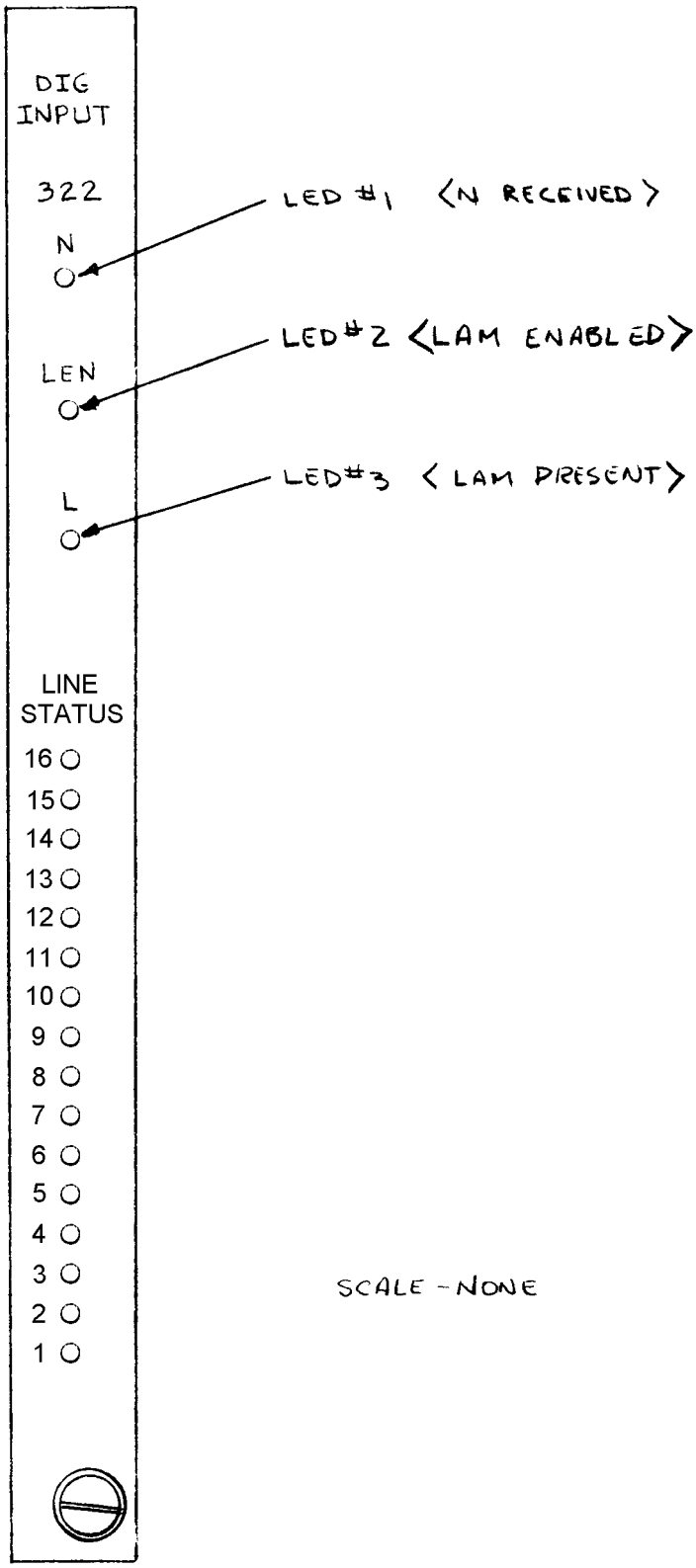
SUGGESTED INPUT CIRCUIT

FIGURE 11.3



LOGIC DEPICTION, SELF TEST FEATURE

FIGURE 11.4



SCALE - NONE

FRONT PANEL LAYOUT

FIGURE 11.5

AUXILIARY CONNECTOR

(Viewed from rear of crate)

RETURN	PIN	PIN	SIGNAL HIGH
Channel 1	1A	1B	Channel 1
Channel 2	2A	2B	Channel 2
Channel 3	3A	3B	Channel 3
Channel 4	4A	4B	Channel 4
Channel 5	5A	5B	Channel 5
Channel 6	6A	6B	Channel 6
Channel 7	7A	7B	Channel 7
Channel 8	8A	8B	Channel 8
Channel 9	9A	9B	Channel 9
Channel 10	10A	10B	Channel 10
Channel 11	11A	11B	Channel 11
Channel 12	12A	12B	Channel 12
Channel 13	13A	13B	Channel 13
Channel 14	14A	14B	Channel 14
Channel 15	15A	15B	Channel 15
Channel 16	16A	16B	Channel 16

Figure 11.6

Input Connector Pin Assignment

Lamps are lited when a logical "1" is applied at the input ports.

6.0 Input Connections

Inputs to respective channels are accessible at the rear auxiliary connector. Connector mate is a Viking 3VH18 or equivalent. Corresponding channel number input pin connections and associated optical-isolator U numbers are listed in Table 6.

Channel No.			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN	A	Signal Low	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	B	Signal High	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
U#			25	21	10	24	20	9	18	7	17	6	15	4	13	2	12	1

7.0 Strap Selects

Strap points are 1 through 8 for each of 16 inputs. User may add wire-wrap posts or solder jumper between the points.

Strap points 1,2,3,4 are located near the upper left corner of the corresponding U numbered IC listed in paragraph 6.0; 5,6 are directly below, and 7,8 are near the lower right corner. U numbers and strap points are silk screened on all PC boards with serial numbers which exceed 012. For unmarked boards refer to the Model 322 Silk Screen layout.

Strapping is shown in the table. All other points are open.

Type of Input	Strap	Strap
Voltage 5V	3 to 4	7 to 8
Voltage 24V	2 to 4	7 to 8
Contact	1 to 8	5 to 6

ISOLATED CONTACT