CICADA SYSTEM
SPECIFICATION

DOCUMENT NO.
TFTR-10B3-H356

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DATE- ~~07/27/83~~ 8/17/83

SUBJECT

HISTOGRAMMER

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REVISIONS

DATE	DESCRIPTION

Histogrammer

1. Abstract.

This specification, in conjuction with referenced documents, sets forth all characteristics of the subject module. The intended use of this document is to provide a minimum design goal for the module as well as a working document for subsequent users. This specification will take precedence if areas of overlap with referenced documents should occur.

2. Reference Documents.

2.1. IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Std. 583-1975.

2.2. Printed Circuit Board Fabrication and Assembly Specification, CICADA Handbook Volume I, TFTR-10A2-H54B.

2.3. Electronic Schematic Specification, CICADA Handbook Volume I, TFTR-10A2-H55.

2.4. Printed Circuit Artwork Specification, CICADA Handbook Volume I, TFTR-10A2-H53A.

2.5. Reliability, Quality Control and Temperature Cycling, CICADA Handbook Volume I, TFTR-10A2-H58.

2.6. Remote Memory Module, CICADA Handbook Volume I, TFTR-10C6-H903.

3. Introduction.

The CAMAC module specified will be used as an interface between elements of the Tokamak Fusion Test Reactor (TFTR) and the Central Instrumentation Control and Data Acquisition (CICADA) computer system. The module will be housed in a CAMAC crate (reference 2.1). The module will function as a histogrammer module with a 20 bit address and 12 bit depth.

Histogrammer

4. Basic Features.

4.1. Histogramming.

The module shall operate in a histogramming mode as follows.

Prior to start of histogramming, the module must be given an ARM Command. This command shall clear all of the Remote Memory by loading each location with a zero value. After this initialization is complete, the module will set a Ready for Input Address (RFIA) flag.

To write data, the external equipment must generate a Write Address Strobe along with a twenty (20) bit address; the module resets the RFIA flag and data from the location addressed in Remote Memory will be incremented by a value of one.

When the module has completed this step it will set the Ready for Input Address (RFIA) flag. A complete histogramming cycle must be completed in a maximum of 2.0 microseconds. If an attempt is made to address non-present memory when histogramming, it will be ignored and a status bit will be set. If an attempt is made to overflow memory word depth of twelve (12) bits, a status bit will be set. Rollover will be strap selectable. Both these status bits will clear with an ARM HISTOGRAM command.

4.2. Dataway From/To Remote Memory.

After receiving an ENABLE READBACK command, this module shall operate in a Dataway mode as follows.

The starting memory address shall be set by the LOAD MAR command. The sequential increment shall be set by the LOAD DELTA command. The MAR will increment by a value of delta, each time a WRITE/READ DATA command is given.

If a WRITE DATA command is being performed, the write data shall be loaded into the remote memory at the address currently stored in the MAR, and MAR will be incremented by delta.

If a READ DATA command is being performed, the value shall be read from remote memory at the MAR, and MAR will be incremented by delta.

It shall be possible to perform Dataway operations at the rates specified in the CAMAC standard (reference 2.1).

4.3. The module shall contain a register (or switches) which shall be hardware settable to the amount of attached remote memory. If an attempt is made to address non-present memory when histogramming it will be ignored, and a status bit will be set.

4.4. The module shall be capable of controlling up to 1 megaword (12 bit words) of remote memory. The remote memory shall be attached to the module through a rear 36 pin edge board connector which mates with a Viking Type 3VH18 or equivalent. The 1 megaword of memory will require 32 remote memory modules so that some of the modules will be located in a second CAMAC crate. The module shall be capable of driving up to 3 feet of cable to a second crate and 32 memories.

4.5. The external port shall attach to the module through a front panel ribbon connector. The external address port shall use a 50 pin ribbon connector AMP Type 88392-1 or equivalent. The module connector shall be capable of accepting a mechanical clamp on the mating ribbon connector.

4.6. The front panel shall have four LED's. LED #1 shall indicate when the module is being addressed from the Dataway. LED #2 shall indicate when the module is being strobed through the external port. LED #3 shall indicate when the module is in Dataway readback mode. LED #4 shall indicate when the module is in Histogramming mode. All indicators must illuminate for a minimum time of approximately 100 milliseconds.

5. Mechanical Characteristics.

5.1. The module shall conform to mechanical specifications as indicated in Reference 2.1.

5.2. The module shall be a single (1x) width CAMAC module.

5.3. The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA Type FR-4 or equivalent. See Reference 2.2.

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5.4. This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate. See Reference 2.1.

5.5. All components are to be identified with a standard manufacturer's part number or standard method of marking (e.g., resistor color coding) and shall have an exact replacement available from a second source manufacturer.

5.6. All electrical components are to be mounted on only one side of the board.

5.7. The operating condition of this module is to be monitored by LED's located on the module front panel. See Figure 11.1 for the suggested front panel layout. All lettering on the front panel shall be either engraved or silkscreened. The front panel material shall be aluminum with an iridite finish with contrasting colored lettering.

5.8. All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross referenced to the manufacturer's part number on the electronic schematic associated with this module. See Reference 2.3.

5.9. The rear auxiliary edge connector 3VH18 shall be used for connection to Remote Memory modules. Pin assignment shall conform to the pin assignment delinated by Figure 11.3. Pin assignments for the external port connector are shown in Figure 11.2.

5.10. The module shall contain conducting covers on both sides. Hardware straps shall be accessible with the component side cover in place.

6. Electrical Characteristics.

6.1. Dataway Interface shall conform to the specification as indicated in Reference 2.1.

6.2. Input Power shall be derived from the standard +/- 6 volt and +/- 24 volt CAMAC supply voltages. Whenever possible, low power circuitry (such as the 74LS series) shall be used.

6.3. The +6 and -6 supply voltages must be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages must be bypassed with electrolytic capacitors of at lesat 6.8 microfarads. In addition, at least

half the integrated circuits must contain a ceramic bypass capacitor of at least .01 microfarads on their supply voltage lines. The .01 microfarad capacitors should be located as close as possible to the integrated circuits and be distributed across the printed circuit board.

6.4. All components on this module must have a MTBF rating as specified in Reference 2.5.

6.5. Timing for the external port strobe and address lines is shown in Figure 11.4.

7. Enviromental Data.

7.1. The module must operate, as defined, over an ambient temperature range of 0 to +50oC.

7.2. The module must operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3. The module must operate, as defined, in the presence of an external magnetic field changing at a maximum rate of 200 gauss per second with a peak magnitude of 100 gauss in any direction.

7.4. The module must operate, as defined, in a radiation environment as follows:

Neutrons:	5 x 10 7 n/CM2/sec
Rad-Dose:	5 x 10 -2 rad (Si)/sec
Integrated Dose:	200 rad (Si)

8. Safety.

All components of this module must be of flame retardant material.

9. Testing.

All modules shall be subjected to a temperature cycling period followed by a functional test prior to shipment. A description of the tests to be performed shall be submitted by the seller for approval and for incorporation into this specification.

10. Reliability and Quality Control.

The module shall meet all applicable requirements specified in Reference 2.5.

11. CAMAC Dataway Commands.

11.1. Initialize or Clear [Z+C] or Power Up

These commands shall reset the module control logic to an initial state of Dataway mode.

11.2. Read MAR [NF(0).A(0)]

In the Dataway/Memory mode, this command gates the contents of the Memory Address Register (MAR) onto Dataway read lines R1-R20 with R1 LSB. R21 through R24 shall return zeroes. Q, X=1 shall be returned for this command, except if it is not in Dataway/Memory mode, in which case Q=0, X=1 shall be returned.

11.3. Read Data [NF(0).A(1)]

In the Dataway/Memory mode, this command gates the contents of Remote Memory at the address residing in MAR, onto Dataway read lines R1-R12 with R1 LSB. The MAR will increment by a value of delta after each read command. If an attempt is made to read from non-present memory or if the module is not in Dataway/Memory mode it will be ignored and a value of Q=0 will be returned, otherwise Q=1, X=1 is returned.

11.4. Load MAR [NF(16).A(0)]

In the Dataway/Memory mode, this command loads the Memory Address Register from Dataway write lines W1 through W20 with the LSB on W1. Q, X=1 shall be returned for this command, except if it is not in Dataway/Memory mode, in which case Q=0, X=1 shall be returned.

11.5. Write Data [NF(16).A(1)]

In the Dataway/Memory mode, this command loads data off Dataway write lines W1 through W12 with LSB on W1, onto Remote Memory at the address residing in MAR. The MAR will increment by a value of

delta after each write. If an attempt is made to write to non-present memory or if the module is not in Dataway/ Memory mode it will be ignored and a value of Q=0 will be returned, otherwise Q=1, X=1 is returned.

11.6. Load Delta [NF(16).A(3)]

In the Dataway/Memory mode, this command loads the sequential increment into the delta register off Dataway write lines W1 through W20 with LSB on W1. Q, X=1 shall be returned for this command, except if it is not in Dataway/Memory mode, in which case Q=0, X=1 will be returned.

11.7. Arm Histogramming [NF(26).A(0)]

This command shall load each location in remote memory with zero. When it has completed zeroing, it shall set the RFIA flag and put the module into histogram mode. It shall take less than or equal to two (2) seconds to complete zeroing. Q, X=1 shall be returned for this command. Any other commands received during this time will not be accepted and will return Q=0, X=1 and R1-R24=0. This command must take precedence over any other command.

11.8. Enable Readback and Disable Histogramming [NF(24).A(0)]

This command shall put the module into Dataway/Memory mode and clear the RFIA flag. It shall set the MAR=0 and set the Delta=1. Q, X=1 shall be returned for this command.

11.9. Read Status [NF(0).A(2)]

This command gates the contents of the status register onto Dataway lines R1 through R22.

R1-R5		= Number of memory modules present
R6	"1"	= Rollover has been enabled
R21-R22	"00"	= Dataway Mode
	"01"	= Histogram Mode
	"10"	= Zeroing Mode
R23	"1"	= Non-Present memory has been addressed

R24 "1" = Word Depth Has Been Exceeded

Q, X=1 shall be returned for this command in either mode.

11.10. Read ID [NF(6).A(0)]

This command gates a value of decimal 356 onto the Dataway read lines. Q, X=1 shall be returned for this command.

12. Suggested Command Sequence.

The suggested command sequence is as follows:

1. ARM Histogramming [NF(26).A(0)]
2. Wait 2 seconds until zeroing is done
3. Start Histogramming [RFIA becomes active]
4. Enable Readback [NF(24).A(0)]
5. Load Starting MAR [NF(16).A(0)]
6. Load Delta [NF(16).A(3)]
7. Read Data [NF(0).A(1)]

Histogrammer

EXTERNAL SIGNALS

RFIA	Ready for Input Address Flag to external equipment indicating that module is ready to accept WAS - ACTIVE LOW
WAS	Write Address Strobe Signal generated by external equipment, strobe valid address into module - ACTIVE LOW
ADDR 1-20	Address lines - ACTIVE H1

PRINCETON PLASMA PHYSICS LABORATORY

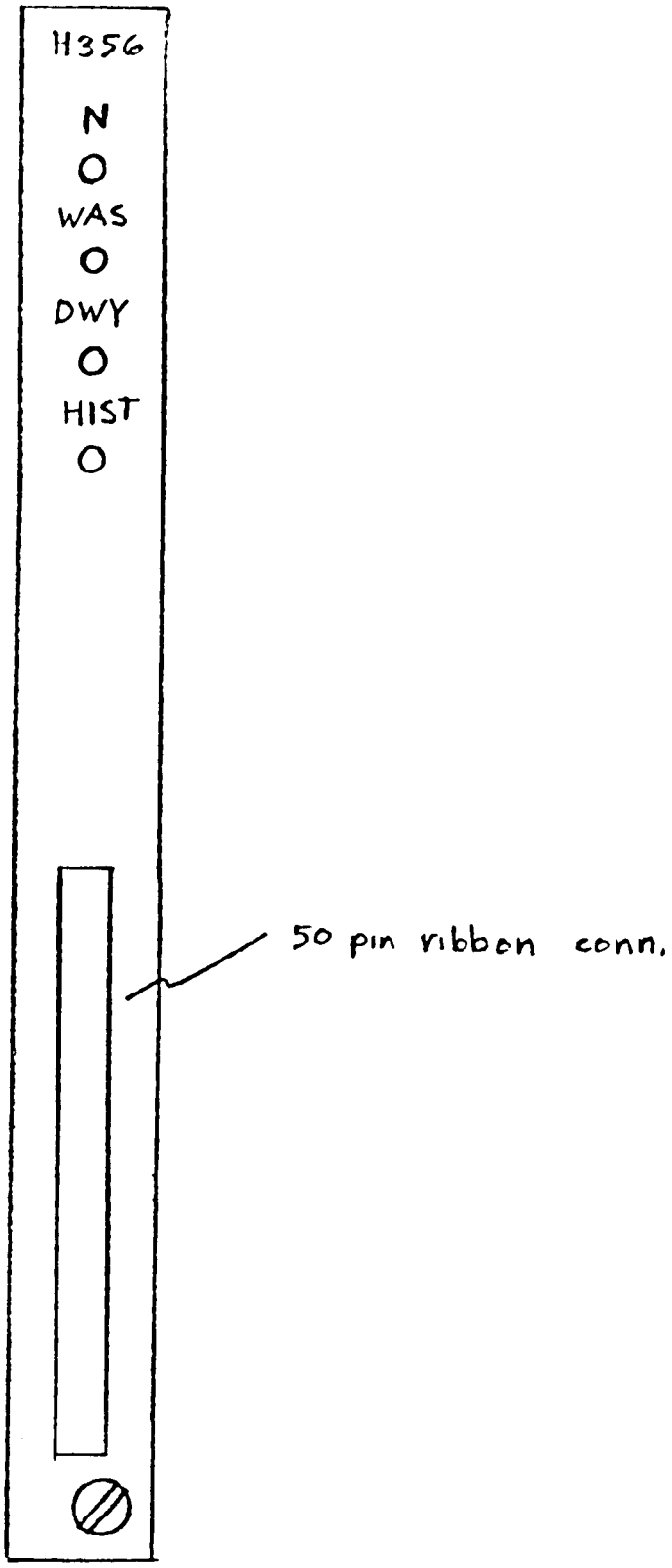
ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT

FRONT PANEL LAYOUT

NAME	
DATE	REVISION DATE



FRONT PANEL LAYOUT

FIG 11.1

Histogrammer

PIN	FUNCTION	PIN	FUNCTION
2	GND	1	A1
4	GND	3	A2
6	GND	5	A3
8	GND	7	A4
10	GND	9	A5
12	GND	11	A6
14	GND	13	A7
16	GND	15	A8
18	GND	17	A9
20	GND	19	A10
22	GND	21	A11
24	GND	23	A12
26	GND	25	A13
28	GND	27	A14
30	GND	29	A15
32	GND	31	A16
34	GND	33	A17
36	GND	35	A18
38	GND	37	A19
40	GND	39	A20
42	GND	41	WAS
44	GND	43	RFIA
46	GND	45	
48	GND	47	
50	GND	49	

FRONT CONNECTOR

PIN ASSIGNMENT

FIGURE 11.2

Histogrammer

PIN	FUNCTION	PIN	FUNCTION
1B	MAB 19	1A	MAB 1
2B	MAB 18	2A	MAB 0
3B	MAB 17	3A	GND
4B	MAB 16	4A	DB 11
5B	MAB 15	5A	DB 10
6B	MAB 14	6A	DB 9
7B	MAB 13	7A	DB 8
8B	MAB 12	8A	DB 7
9B	MAB 11	9A	DB 6
10B	MAB 10	10A	DB 5
11B	MAB 9	11A	DB 4
12B	MAB 8	12A	DB 3
13B	MAB 7	13A	DB 2
14B	MAB 6	14A	DB 1
15B	MAB 5	15A	DB 0
16B	MAB 4	16A	GND
17B	MAB 3	17A	Write Strobe
18B	MAB 2	18A	Read Strobe

AUXILIARY CONNECTOR

PIN ASSIGNMENT

FIGURE 11.3

PRINCETON PLASMA PHYSICS LABORATORY

ENGINEERING NOTE

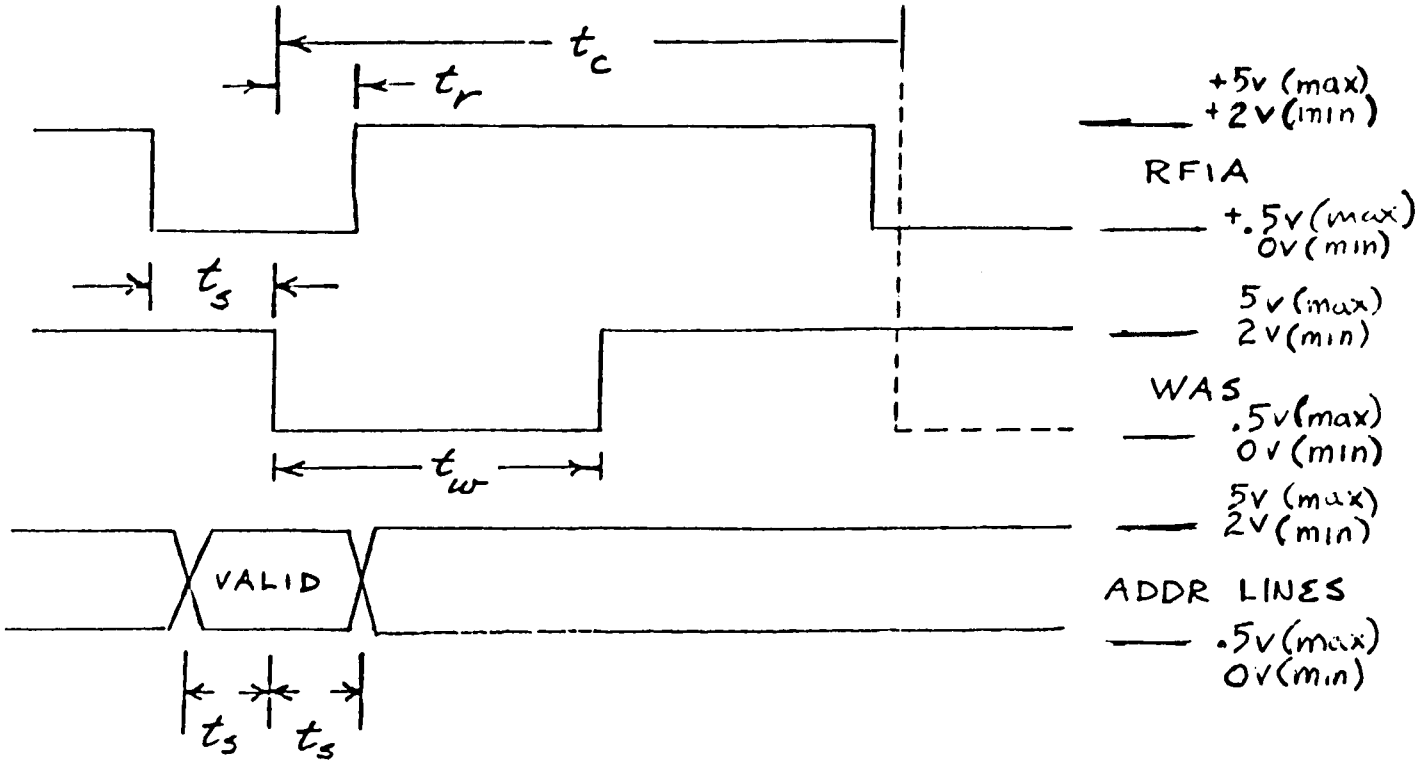
SUBJECT

EXTERNAL TIMING DIAGRAM

NAME

DATE

REVISION DATE



t_c = 2 μs (min)

t_w = 200 ns (min)
500 ns (max)

t_r = 100 ns

t_s = 50 ns (min)

EXTERNAL PORT TIMING

FIG 11.4