	CICADA ENGINEERING SPECIFICATION	DOCUMENT NO. TFTR-10B4-H401
		PAGE 1 OF 17
		DATE- 1/24/78
SUBJECT Facility Clock Subsystem		PREPARED BY H. Del Gatto

APPROVED BY

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REVISIONS

DATE	DESCRIPTION

1.0 Abstract

This specification, in conjunction with referenced documents, sets forth all characteristics of the subject subsystem (Facility Clock System). The intended use of this document is to provide a minimum design goal for the subsystem as well as a working document for subsequent users.

2.0 Reference Documents

2.1 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), 1975. The Institute of Electrical and Electronic Engineers, Inc.

2.2 Telemetry Standards (revised January 1971) IRIG, Document NO. 106-71.

2.3 USA Standard Codes for Information Exchanges, USAS X3.4-1968, ANSI X3.15-1966, ANSI X3.16-1966.

2.4 Printed Circuit Artwork Specification, TFTR-10A2-H53.

2.5 Printed Circuit Board Fabrication and Assembly Specification, TFTR-10A2-H54.

2.6 Electronic Schematic Specification, TFTR-10A2-H55.

2.7 Standard Timing Signal Specification, TFTR-10A2-H57.

2.8 Reliability, Quality Control and Temperature Cycling Specification, TFTR-10A2-H58.

3.0 Introduction

The Facility Clock Subsystem (FCS) when used with appropriate decoding receivers provides the means for generating multiple timing signals throughout a distributed computerized instrumentation, control and data acquistion (CICADA) system. The FCS will be used at the Tokamak Fusion Test Reactor (TFTR) site at Princeton, for the purpose of providing a means of accomplishing synchronous control throughout the facility.

3.1 The timing signal characteristic of the system is accomplished by distributing a coded clock signal to various functional parts of the CICADA system. Remote receivers may utilize this clock to achieve real time synchronism as well as derive a common reference clock signal. In normal operation, a remote receiver will monitor the facility clock and take a specific action upon recognition of a particular code. Among the many functional characteristics possible for a remote receiver will be for a receiver to start a count of clock pulses. At the conclusion of this count the remote receiver may initiate the transmission of a second code. In this manner various codes could be made to exist in defined time intervals to provide the capability for real time synchronism at various remote locations.

3.2 The Power Conversion Clock output of the FCS will be used for control of a high current power conversion system. The power conversion system will utilize a multiple phase motor generator set as its input. Output control will be accomplished by varying the duty cycle of individual phases. The FCS will facilitate the power conversion system by providing a clock signal whose frequency is directly proportional to the varying frequency counting circuits to provide precise control of the power conversion equipment over the variable frequency range of the motor generator set.

4.0 Basic Features

The Facility Clock System will be comprised of two separate assemblies. The two assemblies are defined as the Clock Generator Module (CGM) and the Clock Encoder Module (CEM). Each assembly shall be housed in a CAMAC module and shall conform to the requirements defined by the CAMAC standard (Reference Document 2.1). The primary input/output of the modules shall be implemented through use of a rear mounted auxiliary connector. Electrical interfaces to the modules front panel will be for monitoring and are referenced as secondary interfaces, and will be primarily used during initial system integration.

4.1 Clock Generator Module (CGM) Model 401-1

The CGM shall be a single width CAMAC module and shall be capable of functioning in a CAMAC crate as a stand alone system. The CGM shall have three separate output signals that are derived from the characteristics of an AC input source signal. The output signals of the CGM are defined as the Power Conversion Clock, the Twelve Phase Clock and the Zero Crossing Clock. Each output of the CGM shall be simultaneously available at the rear auxiliary connector and at a front panel connector. Outputs shall be suitably isolated so that loading factors may be considered independently.

4.1.1 The frequency of the Power Conversion Clock shall be directly proportioned to the frequency of the AC input source in the ratio of 16,668 to 1. Corrections to the output frequency shall be made for each cycle of the source voltage and error shall be accumulated. A possible method of achieving this characteristic is delineated in Figure 10.1. With this method the accumulative counter is not cleared so that no counts are lost over long periods of time. The error counter, however, will be cleared after each input cycle and facilitate more rapid response to changing input source frequency.

4.1.2 The Twelve Phase Clock output shall be a continuous pulse train whose frequency shall be directly proportioned to the frequency of the AC input source in the ratio of 12 to 1. The phasing of this output will be such that every twelfth pulse be coincident with the Zero Crossing Clock.

4.2 Clock Encoder Module (CEM) Model 401-2

The CEM shall be housed in a double width CAMAC module. The module shall have thirty-two "priority level" input ports, an "external clock" input port and one "encoded clock" output port; implemented through the rear auxiliary connector. In addition, one "encoded clock" output port and one "external clock" input port shall be simultaneously available to front panel connectors. All outputs shall be suitably isolated so that loading factors for each may be considered independently. The functional requirement of the CEM is to monitor thirty-two (32) priority level input ports and encode upon the clock a seven (7) bit ASCII character code associated with the highest priority level sensed. In addition, the module shall respond to CAMAC Dataway commands and on a lowest priority level, encode the clock with 8 bits of data transferred from the Dataway. The source of the main data clock shall be selected by switch to be either from an internal 1 MHz oscillator or from an external clock input port.

4.2.1 Priority Level Inputs

Each of the thirty-two (32) priority level input ports shall have a seven (7) bit ASCII character code (as defined by Reference Document 2.3) assigned to it. Upon receipt of an input signal the CEM shall encode upon the clock the associated code. Upon recognition of more than one input signal the module shall first encode the data corresponding to the highest level of priority sensed. Each input port shall have an asynchronous storage cell associated with it. The storage cell shall be "set" upon receipt of input and not "reset" until transmission of the code is complete. The CEM will continue to encode and transmit data until all its input cells are clear.

4.2.2 Dataway Interface

The Dataway Interface shall be a standard CAMAC interface conforming to all requirements of reference 2.1. The module will respond to two CAMAC commands as delineated in section 6.6.1.3.

4.2.3 External Clock Input

The External Clock Input shall be a variable frequency TTL compatible clock. The Clock Encoder Module shall be capable of operating at over the full range of the Power Conversion Clock as defined by Sections 3.2 and 6.5.1.

5.0 Mechanical Characteristics

The Clock Generator and the Clock Encoder Module shall be CAMAC modules and conform to the general mechanical requirements outlined in Reference Document 2.1.

5.1 Electrical component mounting for front panels shall be as indicated by applicable Figures 10.2 or 10.3. Circuit board components shall be mounted on a high quality printed circuit board conforming to all the requirements of Reference Document 2.5.

5.2 Mechanical artwork shall be supplied with the modules and shall comply with the requirements of Reference Documents 2.4 and 2.5.

5.3 Auxiliary connectors shall be accessible from the rear of the modules and mounted above the Dataway plug as indicated by Reference Document 2.1, Figures 3 and 4. The CGM shall utilize two thirty-six (36) pin edge type connectors, one (1) in each of two (2) adjacent CAMAC stations. Auxiliary connect shall mate with a Viking connector 3V18 (or equivalent). The card edge connector(s) must be marked with pin 1 on top and pin 18 on the bottom; in addition, the letter 'A' shall be marked on the side of the card adjacent to the next lower numbered CAMAC station.

5.4 Connector pin assignments shall conform to Figure 10.4 and 10.5 as applicable.

6.0 Electrical Characteristics

6.1 The modules must conform to the electrical requirements outlined in reference specifications 2.1 and 2.2.

6.2 Input Power shall be derived from the standard ± 6 volt and ± 24 volt CAMAC supply voltages. Whenever possible, low power circuitry (such as the 74LS series) shall be used to minimize power dissipation.

6.3 The +6 and -6 volt supply voltages must be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages must be bypassed with electrolytic capacitors of at least 6.8 microfarads. In addition, at least half the integrated circuits must contain a ceramic bypass capacitor of at least .01 microfarads on their supply voltage lines. The .01 microfarad capacitors should be located as close as possible to the integrated circuits.

6.4 The use of insulated sandwich type busses for carrying the +5 volt and ground lines for TTL logic is strongly encouraged to provide additional noise suppression and to simplify printed circuit layout design.

6.5 Clock Generator Module

6.5.1 The CGM shall have one AC input signal. The input shall be a sinusoidal signal with a nominal amplitude of 10 volts RMS. The frequency of the AC input signal shall be variable and be derived either from the public utility line (60 Hz) or from the output of a motor-generator set (50 Hz to 100 Hz). The maximum rate of change shall be 3 Hertz per second over an approximate period of 15 seconds. The input/output transfer ratio shall be 16668 pulses per input cycle, effecting an approximate relationship of 1 MHz to 60 Hz. The module shall make use of transformer coupling for isolation, and utilize filters and/or integrators for noise rejection.

6.5.2 The CGM shall have six (6) output circuits as defined by Section 4.1. The outputs shall be transformer coupled and capable of driving properly selected cable terminated with 50 Ohms. The characteristics of the Power Conversion Clock are depicted by Figure 10.6. The characteristics of the Zero Crossing Clock and the Twelve Phase Clock are depicted by Figure 10.7.

6.6 Clock Encoder Module

6.6.1 The Clock Encoder Module shall accommodate thirty-two (32) priority level inputs, one clock input and the standard CAMAC Dataway interface.

6.6.1.1 The clock input shall be a TTL level input, terminated with 50 Ohms. A typical application of this input shall be to interface the CEM with the power conversion clock. An internally mounted switch (not accessible from front panel) will be used to select this input for the facility clock encoding. The CEM shall operate at over the full range of the power conversion clock.

6.6.1.2 The priority level inputs shall be transformer coupled and shall be compatible with a "Standard Timing Pulse" (Reference 2.7).

6.6.1.3 The CEM shall provide for a standard CAMAC Dataway interface and respond to the following commands:

Command #1 - Read Module Number -[F(6)·A(0)]

This command gates the module identification number (decimal 401, binary 000110010001) onto the Dataway read lines R1 through R12 with the LSB on R1.

Command #2 - Write Code - [F(16)·A(0)]

This command writes an 8 bit code from the Dataway write lines W1 through W8. The module will transmit the code received on the Facility Clock on a lowest priority basis. The code received from the Dataway shall be checked for parity and for conflict with dedicated codes (140_8 through 177_8). The module will not respond and will not return X for Dataway "Write Code" commands that violate parity or for those that attempt to write dedicated codes.

The module will return Q as a logical "1" for all addressed commands received.

The module will return X as a logical "1" for command #1 and conditionally as delineated above for command #2.

6.6.2 Clock Encoder Module Outputs (2) shall be TTL compatible and capable of driving a properly selected cable terminated with 50 Ohms. The outputs shall be a serial pulse train encoded in Bi-Phase-Level (or Split Phase, Manchester II ± 180) as defined by Reference 2.2, Paragraph 5.5.2.5 and Figure 4. The protocol for the data encoding shall utilize a ten (10) bit frame as shown in Figure 10.8. Each ten bit frame shall consist of a start bit (logic '0') followed by seven data bits (ASCII coded format, LSB first) an "even parity" bit and a stop bit. The module shall transmit a continuous stream of logic "ones" when no data is being transmitted. The on-time mark of the encoded clock group shall be the trailing edge of the Stop bit, and the maximum delay between event occurrence and the on-time mark shall be twelve (12ms) microseconds for the highest priority event when the CEM is not transmitting and twenty-two (22ms) if a code is being transmitted when the event is sensed.

6.7 The Clock Encoder Module shall provide one LED indicator mounted on the front panel. The LED must illuminate for a minimum time of approximately 200 milliseconds. The indicator shall illuminate when N is received.

6.8 All components on this module must have a MTBF rating as specified in reference 2.5.

7.0 Environmental Data

7.1 The module must operate, as defined, over an ambient temperature range of 0 to +50°C.

7.2 The module must operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must not be affected by an external magnetic field changing at a maximum rate of 100 gauss per second with a peak magnitude of 50 gauss in any direction.

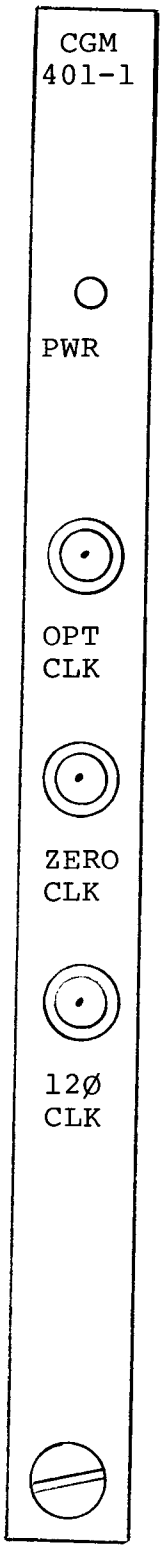
7.4 The module must operate, as defined, in a radiation environment of 1 rad/second (peak) with a total integrated lifetime dose of 1000 rad.

8.0 Safety

All components of this module must be of flame retardant material.

9.0 Testing

9.1 The module shall undergo all tests normally performed by the Seller. A description of the test performed on this module and the results obtained shall be furnished by the Seller. Successful performance of the tests does not relieve the Seller of the responsibility of certifying that all requirements specified herein are met.

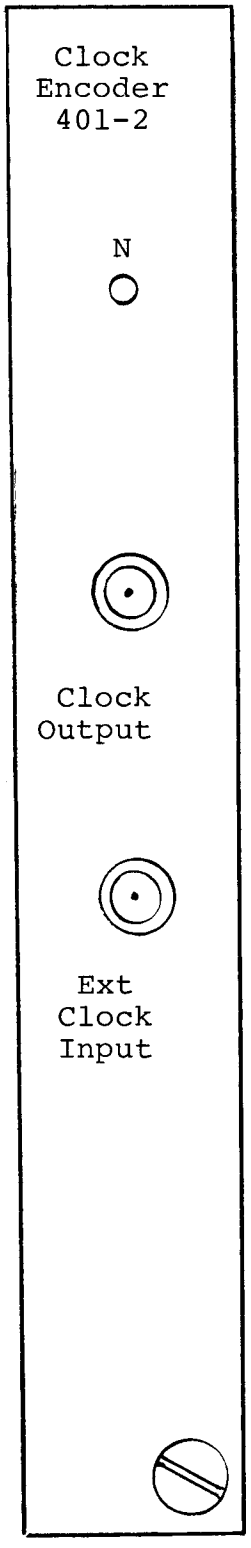


Finish: Iridite
Lettering: Silkscreen

Connectors
Insulated BNC

Jack Screw

Figure 10.2
Front Panel Layout
Clock Generator Module



Finish: Iridite
Lettering: Silkscreen

Connectors:
Insulated BNC

Jack Screw

Figure 10.3
Front Panel Layout
Clock Encoder Module

AUXILIARY CONNECTOR

(VIEWED FROM FRONT OF CRATE)

PIN DESIGNATION

Input Source Input ------	1B	1A	---Input Source Return
Clean Earth ------	2B	2A	--- Clean Earth
Output Clock High ------	3B	3A	--- Output CLock Low
Clean Earth ------	4B	4A	-- Clean Earth
Zero Crossing High ----	5B	5A	-- Zero Crossing Low
Clean Earth ------	6B	6A	-- Clean Earth
12Ø Clock High ------	7B	7A	-- 12Ø Clock Low
	8B	8A	
	9B	9A	
	10B	10A	
	11B	11A	
	12B	12A	
	13B	13A	
	14B	14A	
	15B	15A	
	16B	16A	
	17B	17A	
	18B	18A	

FIGURE 10.4

PIN ASSIGNMENT CLOCK GENERATOR MODULE

AUXILIARY CONNECTOR I

(LEFT MOST CONNECTOR VIEWED FROM FRONT OF CRATE)

Priority Input	1	1B	1A	Ret 1
	2	2B	2A	2
	3	3B	3A	3
	4	4B	4A	4
	5	5B	5A	5
	6	6B	6A	6
	7	7B	7A	7
	8	8B	8A	8
	9	9B	9A	9
	10	10B	10A	10
	11	11B	11A	11
	12	12B	12A	12
	13	13B	13A	13
	14	14B	14A	14
	15	15B	15A	15
Priority Input	16	16B	16A	Ret 16
		17B	17A	
		18B	18A	

AUXILIARY CONNECTOR II

(RIGHT MOST CONNECTOR VIEWED FROM FRONT OF CRATE)

Priority Input	17	1B	1A	Ret 17
	18	2B	2A	18
	19	3B	3A	19
	20	4B	4A	20
	21	5B	5A	21
	22	6B	6A	22
	23	7B	7A	23
	24	8B	8A	24
	25	9B	9A	25
	26	10B	10A	26
	27	11B	11A	27
	28	12B	12A	28
	29	13B	13A	29
	30	14B	14A	30
	31	15B	15A	31
Priority Input	32	16B	16A	Ret 32
		17B	17A	
		18B	18A	

FIGURE 10.5
PIN ASSIGNMENT
CLOCK ENCODER MODULE

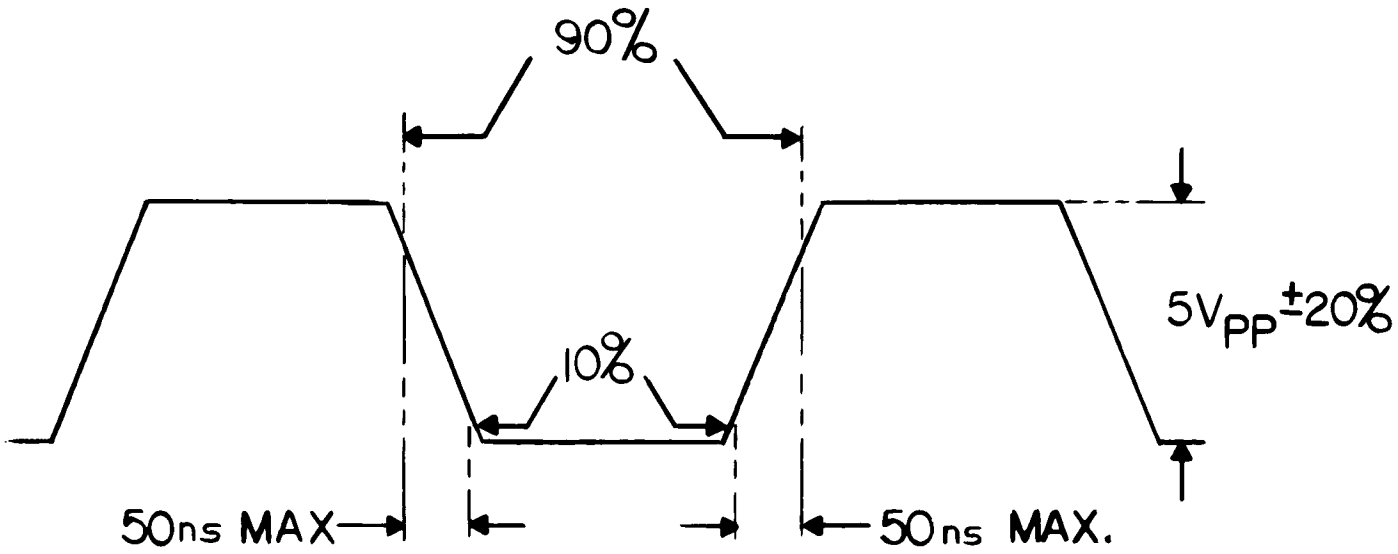


FIG. 10.6
FACILITY CLOCK CHARACTERISTICS

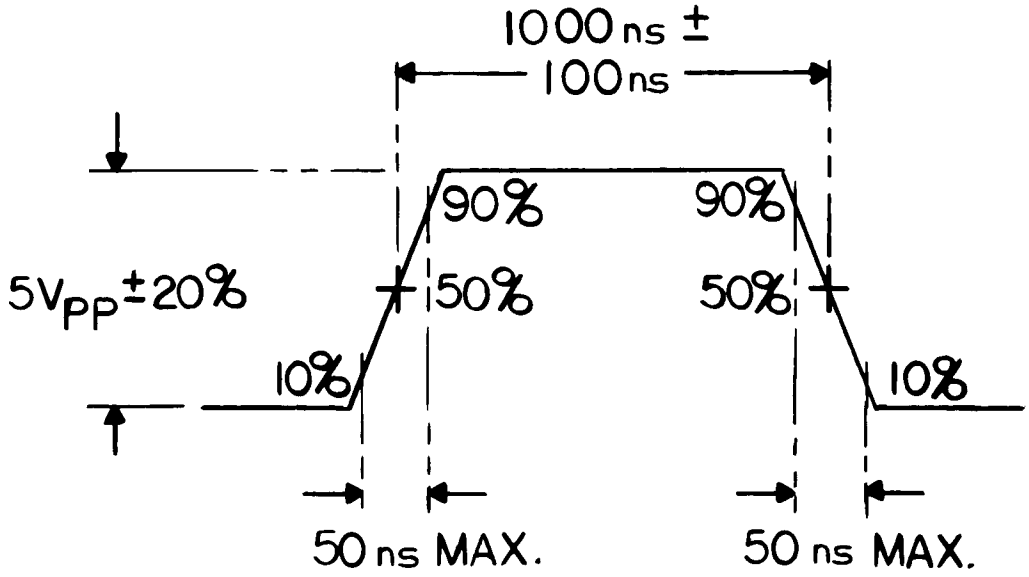


FIG. 10.7
ZERO CROSSING CLOCK

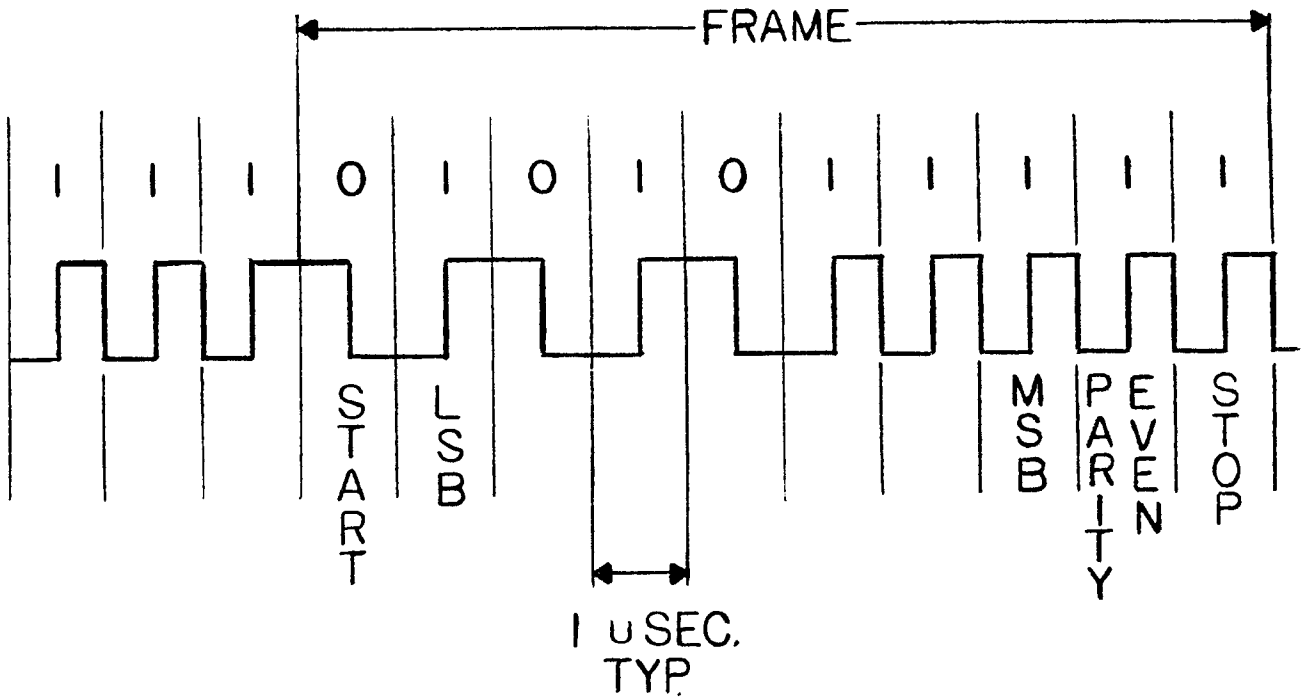


FIG. 10.8 BI-PHASE ENCODED DATA-165