CICADA ENGINEERING SPECIFICATION	DOCUMENT NO. TFTR-10B4-H408
	PAGE 0 of 13
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DATE	DESCRIPTION

TFTR-10B4-H408
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1. Abstract.

This specification, in conjunction with the referenced documents, sets forth all the characteristics of the "serial time interval counter" module. This document provides a minimum design goal for the module as well as a working document for users.

2. Reference Documents.

2.1. Modular Instrumentation and Digital Interface System (CAMAC), IEEE Standard 583-1975.

2.2. Printed Circuit Board Fabrication and Assembly Specification, Document Number TFTR-10A2-H54A.

2.3. Printed Circuit Artwork Specification, Document Number TFTR-10A2-H53

2.4. Electronic Schematic Specification, Document Number TFTR-10A2-H55.

2.5. Reliability, Quality Control and Temperature Cycling, Document Number TFTR-10A2-H58.

2.6. Standard Timing Pulse Specification, Document Number TFTR-10B4-H57.

3. Introduction.

The CAMAC module specified will be used as an interface between elements of the TOKAMAK Fusion Test Reactor (TFTR) and the Central Instrumentation Control and Data Acquistion (CICADA) computer system. The module will be housed in a CAMAC crate (Reference document 2.1). The module will measure the time intervals between a start pulse and 1024 following stop pulses.

4. Basic Features.

The serial time interval counter module is a single width CAMAC module that measures the time intervals between a start pulse and a series of stop pulses. The time intervals are measured by counting clock pulses. The module will save 1024 time interval counts of 24 bits each.

The CAMAC Arm command sets the time interval counter and the address register to zero. When the first start pulse is received after an Arm command, the module begins counting clock pulses. All subsequent start pulses will be ignored until the module is armed again. When a stop pulse is received, the module will save the time interval count.

The module stops saving time interval counts when all memory locations are filled or when the time interval counter overflows (i.e. the counter reaches $FFFFFF_{16}$). In either case the module sets the time interval counter and the address register to zero. The module cannot begin counting again until after an Arm command is received.

The module stops saving time interval counts when it receives an Arm command. The module will clear the time interval counter, set the address register to zero and start counting again when the module receives a start pulse.

The module stops saving time interval counts if it receives a Disarm command or an external Disarm pulse. In either case the module clears the time interval counter and sets the address register to zero. The module can not begin counting again until after an Arm command and a start pulse are received.

The module has two clock sources for counting the timing intervals. The module can use the clock signal on Dataway pin P2 or an external clock signal which inputs through a connector on the front panel.

The module provides three additional clock signals whose frequencies are counted down from the selected clock frequency in the ratios of 1/10, 1/100 and 1/1000. These three ratios are applicable to either internal or external clock. Selection of internal or external clock and the ratio of the clock is accomplished by hardware switches.

The start pulse, the series of stop pulses, the external Disarm pulse and the external clock signal are received through connectors on the front panel of the module.

The module interfaces to the Dataway through the following registers:

Command #	Code	Description
1	Z+C	Initialize or Clear
2	F(0)*A(0)	Read Address Register
3	F(1)*A(0)	Read Status Register
4	F(2)*A(0)	Read Time Interval Count
5	F(6)*A(0)	Read Module Number
6	F(16)*A(0)	Write Address Register
7	F(24)*A(0)	Disarm
8	F(26)*A(0)	Arm

5. Mechanical Characteristics.

5.1. The module shall conform to mechanical specifications as indicated in reference 2.1.

5.2. The module shall be a single (1x) width CAMAC module.

5.3. The electrical components of this module are mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA type FR-4 or equivalent. See reference 2.2.

5.4. This module contains all necessary mechanical components for insertion into a standard CAMAC crate. See reference 2.1.

5.5. All components are identified with a standard manufacturer's part number or standard method of marking (e.g. resistor color coding).

5.6. All electrical components are mounted on only one side of the board.

5.7. The condition of this module is monitored by LED's located on the module front panel. See Figure 11.1 for the suggested front panel layout. All lettering on the front panel is either engraved or silkscreened. The front panel material is aluminum with an iridite finish with contrasting colored lettering.

5.8. All components are assigned an identifying part name (e.g. R1, C2, etc.) which is cross referenced to the manufacturer's part number on the electronic schematic associated with this module. See reference specifications 2.3 and 2.4.

5.9. The three connectors mounted on the front panel as per figure 11.1 are LEMO bulkhead connectors, part number RGOB303CA222 or equivalent. These connectors are wired as per figure 11.2.

6. Electrical Characteristics.

6.1. The module shall conform to electrical specifications as indicated in reference 2.1.

6.2. Input Power shall be derived from the standard ± 6 and ± 24 volt CAMAC supply voltages. Whenever possible, low power circuitry (such as the 74LS series) shall be used. Power consumption for this module is less than 8 watts.

6.3. The -6 and +6 supply voltages must be bypassed with electrolytic capacitors of at least 33 microfarads. The -24 and +24 supply voltages must be bypassed with electrolytic capacitors of at least 6.8 microfarads. At least one half the integrated circuits must have a ceramic bypass capacitor of at least 0.01 microfarads on their supply voltage lines. The 0.01 microfarad capacitors should be located as close as possible to the integrated circuits and equally distributed across the board.

6.4. All components on this module must have a MTBF rating as specified in reference 2.5.

6.5. All the front panel external inputs are optically isolated from the module circuitry. See figure 11.2.

6.6. The start, stop and disarm external front panel inputs are standard timing pulses as per reference 2.6. The stop pulses are received serially on the stop input line.

6.7. The start pulse and the first stop pulse should be at least 1 microsecond apart. If the first stop pulse arrives sooner than 1 microsecond after the start pulse, inaccuracies in the time interval count may occur.

6.8. Stop pulses should be at least 1 microsecond apart. The rising edge of one stop pulse should be at least 1 microsecond after the falling edge of the previous stop pulse. If stop pulses are received more frequently, inaccuracies in the time interval count may occur.

6.9. The time interval counter cannot be read directly. It is only read by the module and its value saved in memory when a valid stop pulse is received. When the time interval counter is set to zero, no accessible data is lost.

6.10. Hardware dip switches mounted on the PC board select either internal or external clock and the ratio of the clock.

6.11. The external clock input is a TTL compatible input.

	Min	Max	
High level voltage	3.0	5.5	volts
Low level voltage	-0.7	0.8	volts
Frequency	0	2	megahertz
Rise and fall times		50	nanoseconds
High voltage pulse width	200		nanoseconds
Low voltage pulse width	200		nanoseconds

6.12. The internal clock signal is on Dataway pin P2 and is TTL compatible. This signal is a 1 megahertz signal and has the following characteristics.

	Min	Max	
High level voltage	3.0	5.5	volts
Low level voltage	-0.7	0.8	volts
Frequency	0.9	1.1	megahertz
Rise and fall times		50	nanoseconds
High voltage pulse width	200		nanoseconds
Low voltage pulse width	200		nanoseconds

6.13. The module provides three additional clock signals whose frequencies are counted down from the selected clock frequency in the ratios of 1/10, 1/100 and 1/1000. These three ratios are applicable to either internal or external clock.

6.14. The module will be disarmed when first powered up. The module cannot begin a count until it receives an Arm command and a start pulse.

6.15. The module stops saving time interval counts when the time interval counter overflows, i.e. the counter reaches $FFFFFF_{16}$. The module sets the time interval counter and the address register to zero. The module cannot begin counting again until after an Arm command and then a start pulse are received.

6.16. When the module fills the 1024th memory location, it stops saving time interval counts. The module clears the time interval counter and sets the address register to zero. A new count cannot begin until the module receives an Arm command. The module will not overwrite previous data until after an Arm command is received.

6.17. The module stops saving time interval counts when it receives an Arm command. The module sets the time interval counter and the address register to zero. The module will begin counting again when a start pulse is received.

6.18. The module stops saving time interval counts if it receives a Disarm command or an external Disarm pulse. In either case the module sets the time interval counter and the address register to zero. The module can not begin counting again until after an Arm command and a start pulse are received.

6.19. The module returns an X equal to one for all commands it is equipped to perform.

6.20. CAMAC Command Description.

6.20.1. Command #1. Initialize or Clear [Z+C]

This command disarms the module. After this command the module must receive an Arm command and a start pulse before a count can begin. This command stops the count if the module is counting and sets the time interval counter and the address register [F(16)*A(0)] to zero. This command clears bits R1 through R10 and R20 through R24 of the Status register [F(1)*A(0)].

6.20.2. Command #2. Read Address Register [F(0)*A(0)]

This command gates the address register onto Dataway lines R1 through R10 with the least significant bit on R1. Bits R11 through R24 are always equal to zero. This register is the address to be accessed for the data in the Read Interval Count register, [F(2)*A(0)]. This address register is incremented by one after each read of the Read Interval Count register [F(2)*A(0)]. The address register will be set to zero when an Arm or a Disarm command is received, when the counter reaches $FFFFFF_{16}$, when all the memory locations have been filled during a count or when an external Disarm pulse is received.

The interval count between the start pulse and the first stop pulse is stored in location 000 and the interval count between the start pulse and the 1024th stop pulse is stored in location $3FF_{16}$.

While the module is armed, it will not perform this command and returns Q equal to zero when it receives this command. When the module is not armed, it will perform this command and return Q equal to one.

6.20.3. Command #3. Read Status Register [F(1)*A(0)]

This command gates the status register onto Dataway read lines R1 through R24. The module returns Q equal to one each time it receives this command.

The number of valid stop pulses that have been received since the last valid start pulse is gated onto Dataway lines R1 through R10 with the least significant bit on R1. Bits R1 through R10 are cleared by an Arm command or by an initialize or clear command (Z+C). Bits R11 through R16 are always zero.

A valid start pulse is the first start pulse received after an Arm command. A valid stop pulse is a stop pulse received after a valid start pulse and before the time interval counter reaches $FFFFFF_{16}$. There are only 1024 possible valid stop pulses after each valid start pulse.

While the module is armed the data in bits R1 through R10 is unstable and an accurate reading of the data may not always be possible. Bits R11 through R16 are always zero.

R17=1 External clock input selected.
R17=0 Internal clock input selected (pin P2).

R19	R18	Clock
0	0	Selected Clock
0	1	1/10
1	0	1/100
1	1	1/1000

R20=1 The module is armed.
R20=0 The module is disarmed.

R21=1 The module is counting.
R21=0 The module is not counting.

R22=1 1024 stop pulses have been received during this count.
R22=0 Fewer than 1024 stop pulses have been received during this count.

R23=1 The time interval counter has overflowed, i.e. reached $FFFFFF_{16}$.
R23=0 The time interval counter has not overflowed since the last Arm command.

R24=1 A stop pulse arrived after the counter overflowed.
R24=0 No stop pulse has arrived after the counter overflowed during this count.

6.20.4. Command #4. Read Time Interval Count [F(2)*A(0)]

This command gates an interval time count onto Dataway read lines R1 through R24 with the least significant bit on R1. This time interval count is the data at the address supplied by the address register [F(0)*A(0)]. After this command is performed, the address register is automatically incremented by one.

The interval count between the start pulse and the first stop pulse is stored in location 000 and the interval count between the start pulse and the 1024th stop pulse is stored in location $3FF_{16}$.

While the module is armed, it will not perform this command. It will return Q equal to zero when it receives this command. When the module is not armed, it will perform this command and return Q equal to one.

6.20.5. Command #5. Read Module Number [F(6)*A(0)]

This command gates the module identification number (decimal 408, hexadecimal 198) onto Dataway read lines R1 through R12. The least significant bit is on R1. Bits R13 through R24 are zero.

The module returns Q equal to one each time it receives this command.

6.20.6. Command #6. Write Address Register [F(16)*A(0)]

This command writes the data on Dataway lines W1 through W10 into the address register, with the least significant bit on W1. This register is the address to be accessed for the data in the Read Time Interval Count register [F(2)*A(0)].

This address register is incremented by one after each read of the Read Interval Count register [F(2)*A(0)]. The address register will be set to zero when an Arm or a Disarm command is received, when the counter reaches $FFFFFF_{16}$, when all the memory locations have been filled during a count or when an external Disarm pulse is received.

The interval count between the start pulse and the first stop pulse is stored in location 000 and the interval count between the start pulse and the 1024th stop pulse is stored in location $3FF_{16}$.

While the module is armed, it will not perform this command. It will return Q equal to zero when it receives this command. When the module is not armed, it will perform this command and return Q equal to one.

6.20.7. Command #7. Disarm [F(24)*A(0)]

This command stops the count if the module is counting. It sets the time interval counter and the address register to zero. A new count cannot begin until the module receives an Arm command and a start pulse.

The module returns Q equal to one each time it receives this command.

6.20.8. Command #8. Arm [F(26)*A(0)]

After the module receives this command, the next start pulse will begin the count. The module cannot begin a count until it receives this command. If the module is counting when this command is received, the count will stop. This command sets the time interval counter and the address register to zero.

The module begins counting when it receives the first start pulse after it receives an Arm command. Subsequent start pulses are ignored until the next Arm command.

The module returns Q equal to one each time it receives this command.

6.21. The LEDs described in this section are mounted on the front panel as illustrated in figure 11.1.

The N LED is turned on for a minimum of 100 milliseconds whenever the module receives an N signal.

The ARMED LED is turned on whenever the module receives an Arm command. This LED is turned off when the module is disarmed. The module is disarmed after a Disarm command or an external Disarm pulse is received. After a count is begun, the module is disarmed when all the memory locations are filled, i.e. 1024 stop pulses have been received or when the counter overflows, i.e. reaches $FFFFFF_{16}$.

The COUNT LED is turned on whenever the module is counting, i.e. after a valid start pulse. It is turned off whenever the module is disarmed.

The OVRFLW LED turns on when a stop pulse is received after the counter has overflowed. This LED is turned off when an Arm command is received.

The four LEDs labelled CLK FQ will show the selected clock frequency. The bits R19 and R18 are from command #3, F(1).A(0).

LED On	R19	R18	Clock
LED 1	0	0	Selected Clock
LED 2	0	1	1/10
LED 3	1	0	1/100
LED 4	1	1	1/1000

The EX CLK LED turns on when the external clock signal is selected. If this LED is turned off, the internal clock has been selected.

The START LED turns on for at least 100 milliseconds whenever a start pulse is received, whether it is a valid start pulse or not.

The STOP LED turns on for at least 100 milliseconds each time a stop pulse is received, whether it is a valid stop pulse or not.

The DISARM LED turns on for at least 100 milliseconds whenever a disarm pulse is received.

7. Environmental Data.

7.1. The module must operate, as defined, over an ambient temperature range of 0 to +50 degrees C.

7.2. The module must operate, as defined, over a relative humidity range of 10% to 90%. The module need not operate under conditions of water condensation.

7.3. The module must operate, as defined, in the presence of an external magnetic field changing at a maximum rate of 200 gauss per second with a peak magnitude of 100 gauss in any direction.

7.4. The module must operate, as defined, in a radiation environment as follows:

Neutrons: 2×10^{7} n/cm^2/sec

Rad-Dose: 5×10^{-2} rad (Si)/sec

Integrated Dose: 200 rad (Si)

8. Safety.

All components of this module must be of flame retardant material.

9. Testing.

9.1. The module shall undergo all tests normally performed by the seller. A description of the tests to be performed shall be furnished by the seller.

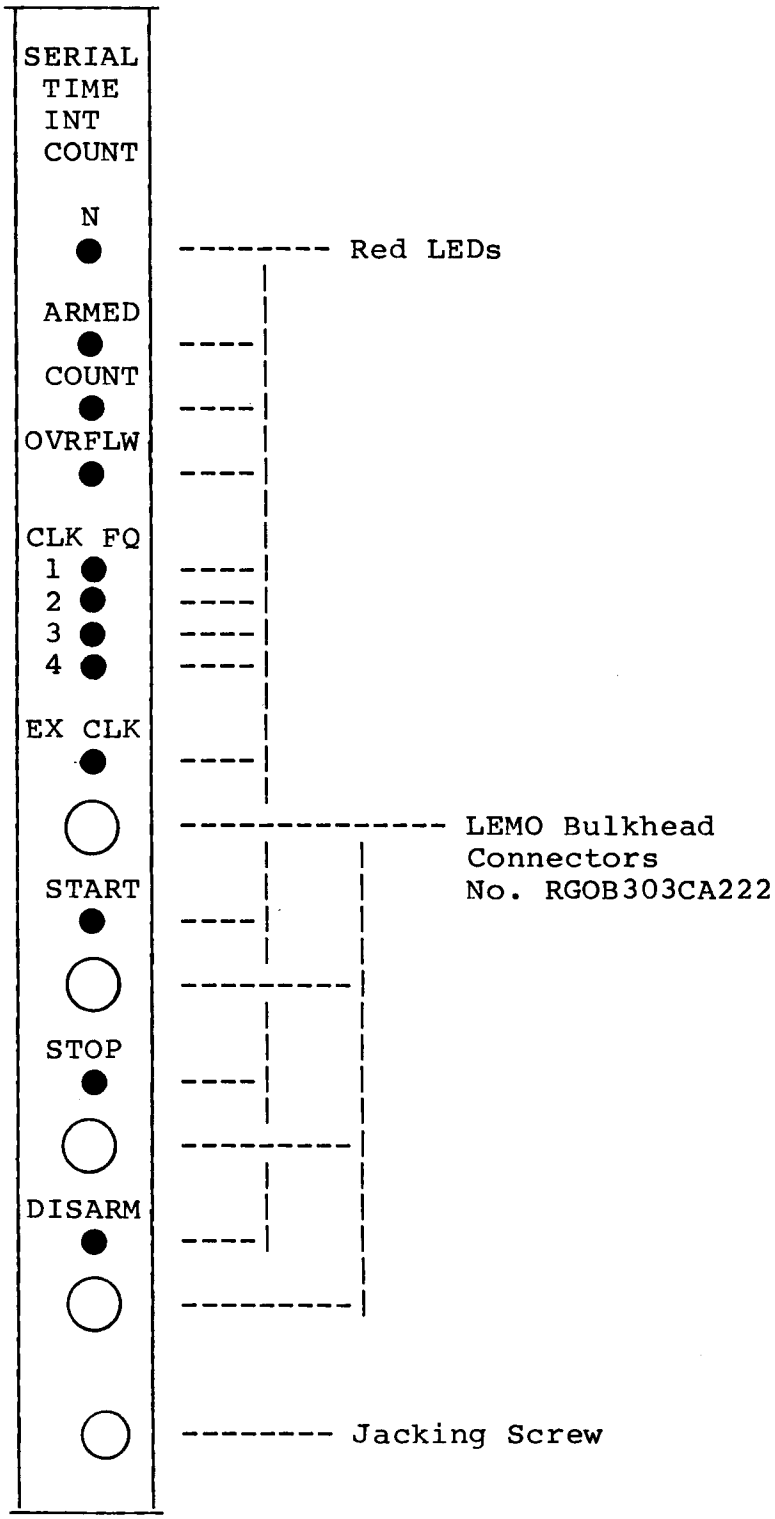
9.2. The module under test must be tested in a CAMAC crate equipped with ± 6 and ± 24 volts supplied via a standard CAMAC power supply.

9.3. The Dataway signals and timing must meet the conditions specified in reference 2.1.

9.4. Tests will be performed after temperature cycling.

10. Quality Control.

10.1. This equipment shall meet all applicable requirements specified in reference 2.5.



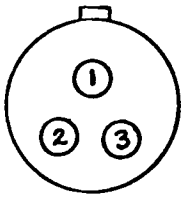
Front Panel Layout

Figure 11.1

LEMO Bulkhead Connector (3 pin)
Part Number RGOB303CA222

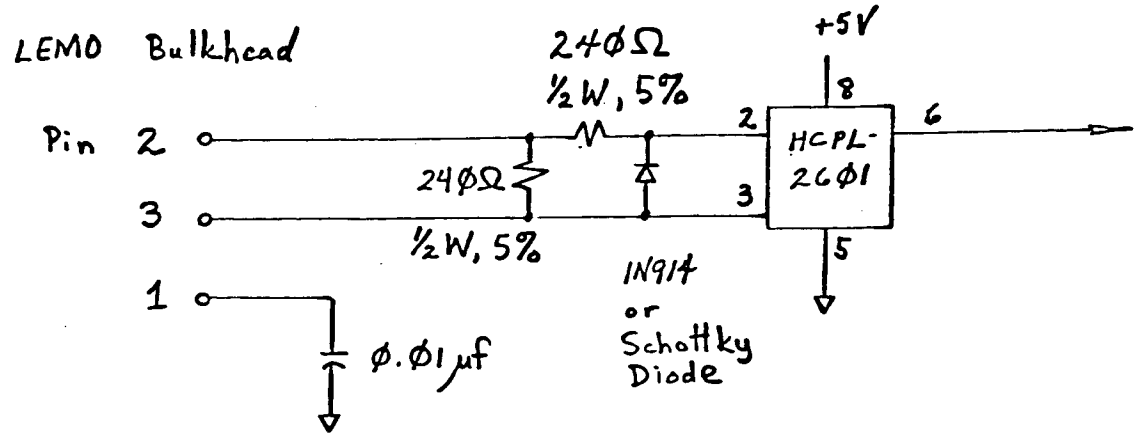
Alignment Key

View from solder cup (or crimp) side



Pin 1: 0.001 f capacitor to ground
Pin 2: + Signal
Pin 3: - Signal

Typical Connector Circuitry



Connector Wiring

Figure 11.2

P2 GLITCH PROBLEM

John Wertenbaker 3/17/00

It was discovered that the P2 line on the CAMAC dataway can contain glitches that are caused by the capacitive coupling of the 1Mhz P2 line and the function (F) lines. The F(16) line, which is just opposite of P2 has the greatest coupling, but the more F lines that are active, the larger the glitch will be on P2. This glitch can vary from crate to crate, and from slot to slot, but, in one case it was measured at 2 volts.

The glitch can cause any module that uses the P2 line, like the 408, 409, 412, 413, and 908 modules, to count an extra clock pulse, causing timing errors in any system that uses those modules. Below is a list of the modules that derive their clock from the P2 line, and a description of the input circuitry in each module.

408 P2 input goes to a 74LS28, which is a NOR gate.
409 P2 input goes to a 74123 one-shot.
412 P2 input goes to a 74LS38, which is a NAND gate.
413 P2 input goes to a 74LS02.
904 P2 input goes to a 74LS14 Schmitt-trigger inverter.
908 P2 input goes to 3 74LS74's and 2 74LS08's.
910 P2 input goes to a 74LS14 Schmitt-trigger inverter.
912R P2 input goes to a 74LS14 Schmitt-trigger inverter.
914 does not use the P2 line.

The 409 Timed Gate module was the only module that was tested and proven to be susceptible to this glitch. The 408, 412, 413, and 908 modules are assumed to be susceptible, also, based on their input circuitry. The 904, 910, and 912R modules are much more tolerant of this glitch, due to the Schmitt-trigger inputs, and are probably not affected. The 914 module generates its own 1Mhz, and is independent of the P2 line.

This occurrence of this problem is rare due to the nature of clock cycles in NSTX, and its predecessor, TFTR. In those machines, most modules are set up and armed long before any trigger pulse starts the counting of P2 clock pulses. Very few CAMAC commands are performed after these arm and setup commands. In most cases, the only commands that come through during the counting times are read-back commands and L-2 crate controller wakeup commands. These happened every 2 seconds in TFTR, and even less often than that in NSTX. Also, most of the time, the 1Mhz P2 line is divided down to a much lower frequency, so a few microseconds of inaccuracy would not be noticed.

For the rare cases when the glitches can cause problems, such as the Facility Clock Generator crates, the recommended fix is to insert a P2 Capacitor Filter Module in the crate as close as possible to the module that uses the P2 line. This module contains a 1000pf capacitor from the P2 line to ground. This attenuates the high frequency of the glitch, without seriously rounding off the edges of the 1Mhz P2 signal.

It should be noted that the 404A had a similar problem with the P1 line. The BUSY line, which is an un-terminated line in the crate, was coupling a glitch over to the P1 line. The repair for that problem was to install a Schottky diode on the BUSY line to clamp the negative-going overshoot at the low-going transition of the BUSY pulse, and replace the 74LS04 with a Schmitt-trigger 74LS14 at the P1 input. However, it was not considered practical to modify every module that uses the P2 line because the problem is much more rare than the P1 problem, due to the nature of when the glitch occurs.

408 Memory Depth Discrepancy

John Wertenbaker 07/11/2008

The specification for the 408 Timing and Sequencing Module was written before BiRa designed the 408. However, BiRa added the capability for storing 2048 interval counts, instead of the 1024 counts that the specification calls for. BiRa provided a jumper to limit the memory to 1024, but they shipped all their modules to us in the 2048 configuration. Consequently, none of the 408 modules at PPPL match the specification. The differences are in the commands F(0) A(0), F(1) A(0), and F(16) A(0). The next 8 pages in this document are the original BiRa manual for the 408. Please refer to the BiRa manual when learning the above mentioned CAMAC commands.

Bi Ra Systems, Inc.

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MODEL 2408
SERIAL TIME INTERVAL COUNTER

OPERATIONS MANUAL

MARCH 1982

TABLE OF CONTENTS

FIGURE

Serial Time Interval Counter
Operations Manual Model 2408

1.0 Introduction

The 2408 Module was designed by Bi Ra for use as an interface between elements of the TOKAMAK Fusion Test Reactor (TFTR) and the Central Instrumentation Control and Data Acquisition (CICADA) Computer system. The module will measure the time intervals between a START PULSE and up to 2048 successive STOP PULSES. STOP PULSES are switch selectable for 1024 or 2048.

2.0 Description and Basic Features

The unit is a one (1) wide CAMAC module that measures the time intervals between a START PULSE and a series of STOP PULSES with rates of occurrance up to 1.0 MHz. The module will save up to the selected number (1024 or 2048) time interval counts of 24 bits each.

The CAMAC ARM command sets the TIME INTERVAL COUNTER and the memory address register to zero. When the first START pulse is received after an ARM command, the module begins counting clock pulses. All subsequent START pulses will be ignored until the module is ARMED again. When STOP pulses are received the module stores each TIME INTERVAL count at successive memory location.

The module stops saving TIME INTERVAL counts when all memory locations are filled or when the TIME INTERVAL COUNTER reaches hexidecimal FFFFFF. In either case the module sets the TIME INTERVAL counter and MEMORY ADDRESS register to ZERO.

The module stops saving TIME INTERVAL counts when it receives an ARM command. The ARM will CLEAR the TIME INTERVAL COUNTER, SET the MEMORY ADDRESS REGISTER to ZERO and start counting again when the module receives a START PULSE.

The module stops saving TIME INTERVAL counts when it receives a DISARM command or an EXTERNAL DISARM pulse. For either, the TIME INTERVAL counter is CLEARED and the MEMORY ADDRESS register is set to ZERO. The module cannot begin counting again until after an ARM Command followed by a START pulse is received.

The module has TWO (2) switch selectable CLOCK sources for counting time intervals. The module can use the clock signal on DATAWAY pin P2 or an EXTERNAL clock which inputs via a front panel connector. The selected clock is switch selectable for division 1, 10, 100 and 1,000. P2 clock loading is less than one TTL load.

3.0 Front Panel Input Signals/Connectors

Front Panel inputs are EXTERNAL CLOCK, START, STOP, and DISARM. All inputs are via HCPL 2601 opto isolators and LEMO type RG.OB.303 Connectors. Mating connectors are FG.OB.303. Pin orientation and input circuits are shown is Figure 3.0. The input circuit requires a minimum input voltage level for logic "1" of 2.2V at 15ma. Turn ON/OFF is less than 150ns for 3.0 to 5.5V (approx. 38ma) and a logic zero of less than approximately 1.2V (5ma). Recommended logic "1" voltage range is between +3 and +5.5V; logic "0" between -0.7 and +0.8. The terminating input resistance can be altered for reduced logic "1" current but reflections and degraded operation may result.

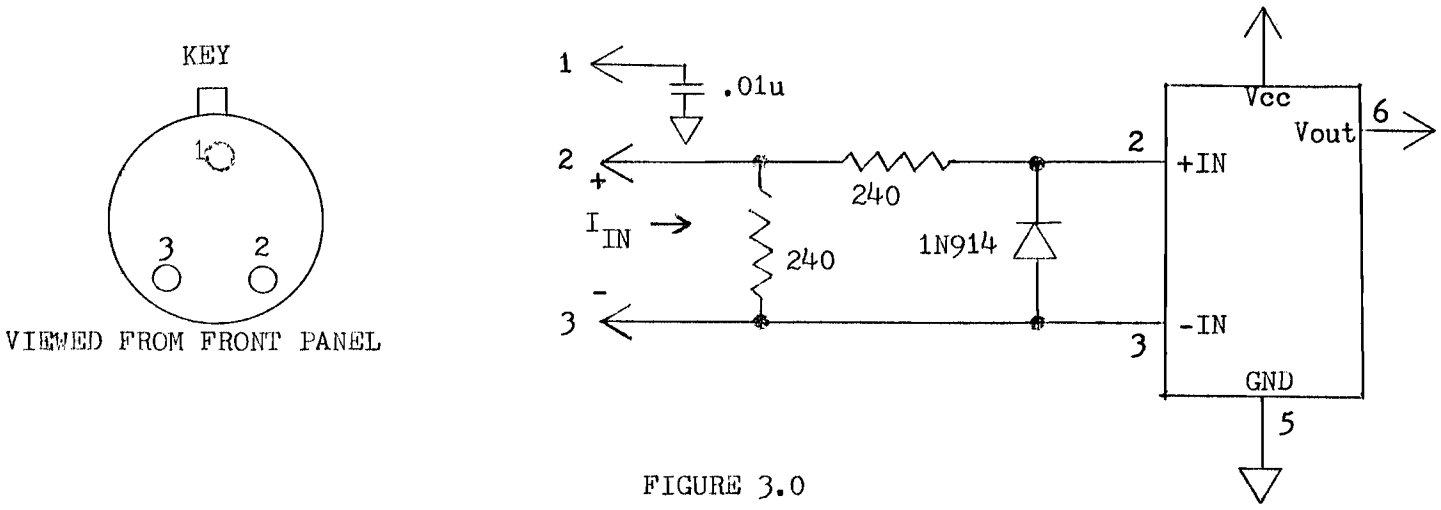

FIGURE 3.0

MODEL 2408 SERIAL TIME INTERVAL COUNTER
Input Connector Orientation and Input Circuit Configuation

4.0 Commands

Dataway X is returned for all commands (except Z + C). Q is conditionally returned.

Z + C - Initialize OR Clear, NO Q

Disarms module. Stops Time Interval Counter if counting. Resets Time Interval Counter, Memory Address Register to zero and clears R1-R12, R20-R24 Status data.

F0A0 - Read Address Register, Q if NOT ARMED and valid.

Gates Memory Address to Dataway R1(LSB) through R11 and R12, 1K = 1, 2K = 0 (selected Memory Length 1K or 2K). R13 through R24 are zero.

F1A0 - Read Status, Q for each command

Gates Status to Dataway R1 through R24. R1(LSB) through R12 is the number of Valid Stop pulses that have been received since the last Valid Start pulse. R13-R16 are zero.

A Valid Start pulse is the FIRST Start pulse received after an ARM Command. A Valid STOP pulse is a STOP pulse received after a Valid Start pulse and before the Time Interval Counter reaches hexidecimal FFFFFF. There are 1024 or 2048 possible Valid Stop pulses after each Valid Start pulse depending upon the Memory Length selection.

NOTE: While the module is ARMED the R1-R12 data bits are unstable and an accurate reading is not always possible.

R13-R16 always zero.
R17 1 is External Clock selected; 0= Internal P2 Clock.

R19	R18	Clock Selected Clock frequency
0	0	
0	1	÷10
1	0	÷100
1	1	÷1000

R20 = 1 - Module ARMED; 0 Module DISARMED
R21 = 1 - Module is counting; 0 = not counting
R22 = 1 - Selected number of Stop pulses (1024 or 2048) have been received during this count; 0 = less than Selected number of Stop pulse have been received during this count.
R23 = 1 - Time Interval counter has overflowed, i.e. reached hexidecimal FFFFFF; 0 = no overflow since last ARM command.
R24 = 1 - A Stop pulse arrived after Time Interval Counter overflow; 0 = no Stop pulse received after overflow.

F2A0 - Read Time Interval Count, Q if NOT ARMED and Valid.

Valid Command Gates an interval time count to Dataway R1 (LSB) through R24. The data is the 24 bit interval stored at the memory location determined by the Memory Address register. After a valid command the Memory Address register is automatically incremented by one.

NOTE: The interval count (Time Interval counter) between the Start pulse and the First Stop pulse is stored at Memory Address zero; the last at hexadecimal Memory Address 3FF (1024 selected) or 7FF (2048 selected) provided no Time Interval Counter overflow.

F6A0 - Read Module Number, Q for each command.

Gates the module I.D. (decimal 408, hexadecimal 198) an Dataway R1 (LSB) through R24. i.e. R4,R5,R8 R9 logical "1"; remaining dataway R lines logical "0".

F16A0 - Write Address Register, Q if NOT ARMED and Valid

Valid command enters W1 (LSB) through W11 in the Memory Address Register is reset to zero when an ARM or DISARM command (F26A0 or F24A0 respectively) is received, when the Time Interval Counter overflows (hexidecimal FFFFFF), when all Memory locations have been filled during a count, or when External DISARM is received.

F24A0 - Disarm, Q for each command

Stops Time Interval Count if counting. Clears Time Interval Counter and Memory Address Register to zero. New Count cannot begin until the module receives an ARM followed by a Start pulse.

F26A0 - ARM, Q for each command.

Module cannot begin a count until it receives this ARM command. The next Start pulse starts the count. All successive Start pulses are ignored. If the module is counting when this command is received, the count will stop. Time Interval Counter and Memory Address registers are cleared to zero.

5.0 Front Panel Indicators

A Total of thirteen (13) red LED's allow visual monitor of the state of the module. Each LED is plainly identified and lighted as defined on next page:

N - Flashes for approx. 100ms when the module N line is active.

ARM - Turned ON when the module receives an ARM commands. Turned OFF when DISARMED by dataway command or an external DISARM and when all memory locations are filled or when the Time Interval count has overflowed.

COUNT - Lighted when the module is counting. Turned OFF when module is DISARMED.

OVRFLO - Turned ON when STOP pulse is received after the counter has overflowed. Turned OFF when an ARM is received.

MEM 1K - ON when 1024 STOP pulse capability is selected. OFF for 2048.

CLK FQ - Four (4) Clock Frequency lamps are provided:
1 - Selected (no division).
2 - Divided by 10.
3 - Divided by 100.
4 - Divided by 1000.

EX CLK - Turns ON when EXTERNAL CLOCK is selected. OFF when Internal Clock is selected.

START - Flashes ON for approx. 100ms when a START pulse is received whether it is a valid pulse or not.

STOP - Flashes ON for approx. 100ms when a STOP pulse is received whether it is a valid pulse or not.

DISARM - Flashes ON for approx. 100ms when a DISARM is received whether it is a valid pulse or not.

6.0 Switch Settings

Three sets of switches control clock origin, clock frequency and selection of either 1024 or 2048 Stop inputs. Switches are accessible via left panel cutout.

6.1 Clock Origin - Switch nearest the front panel.
INTERNAL - Rocker to C3 position, Princeton Units Rocker to C1
EXTERNAL - Rocker to C4 position, Princeton Units Rocker to C2

6.2 Clock Frequency - SW2 two rocker (1,2) switch located upper front of board. 1 = ON, 0 = OFF

Frequency	1	2
input	0	0
input ÷ 10	0	1
input ÷ 100	1	0
input ÷ 1000	1	1

6.3 STOP Pulse Select (NOTE: PRINCETON UNITS PERMANENTLY STRAPPED FOR 2048)

1024 - Rocker to C1
2048 - Rocker to C2

7.0 Operating Procedures

7.1 Preliminary

Never install or remove the module from the CAMAC crate with crate Power ON or the module may be damaged. Prior to use, visually inspect the module for any damage and repair unit if required.

7.2 Switch Settings.

Refer to Para 6.0 and select Clock origin either INTERNAL or EXTERNAL. Select the division ratio of clock for 1 to 1, division by 10, 100, or 1000. Set the number of STOP pulses for 1024, or 2048. Princeton units are not switch selectable and are strapped for 2048.

7.3 Installation

Select desired Crate Slot location and install the module firmly in position.

Acquire cables and verify input signals are as defined in Para. 3.0. Install front panel cables mates in corresponding connectors. And apply Crate Power.

7.4 Operation

Each application of the module is unique, but each requires use of the commands listed in Para. 4.0. With the use of the commands the unit may be controlled to perform its intended use. It is assumed that the CLOCK FREQUENCY INTERNAL/EXTERNAL CLOCK and memory length switches have been set. Respective front panel lamps will indicate selected parameter.

A typical sequence of operation may be as follows:

N led flashes and Dataway X is returned each time the module is addressed.

1. Initial power-up of the crate will DISARM the module.
   DISARM LED will light, all others OFF.

2. Issue Z + C. No change of module status will be apparent. Any READ command may be issued to verify status while the module is DISARMED. Module ID, and Read Status Commands are always active. See Para 4.0 Commands.

3. F26A0 lights ARM led, DISARM OFF. Q, X returned

4. The next front panel START input after ARM command, Allows Time Interval Counter to function, turns COUNT led ON and START led flashes for minimum of 100ms. Subsequent START pulses after ARM will have no affect except to cause the START led to flash.

5. STOP pulses input at the front panel will enter Time Interval Count in memory such that the first pulse occurrance is stored at memory address ZERO, second at location ONE etc; the last STOP pulse will be stored at the last selected memory address. STOP led will flash for a minimum of 100ms for each STOP pulse. If the Time Interval Counter

overflows (reaches Hex FFFFFF) prior to the occurrance of the selected number of STOP pulses the module stops saving Time Interval Counts. For either case the module stops saving Time Interval counts, Time Interval counter. Memory Address Registers are reset to zero, module is DISARMED and can not begin counting until after an ARM command followed by a START pulse is received. For this condition DISARM led and lighted front panel lamps depict the module status.

NOTE: During the counting sequence an EXTERNAL or commanded DISARM will stop the counting sequence.

6. When DISARMED and Q is returned, an F16A0 command will allow random access of the STOP pulse data via dataway write lines. i.e. Memory Address ZERO (0) will contain the Time Interval Count for the first STOP pulse which occurs after a valid START, address NINE (9) contains NUMBER TEN (10) STOP pulse etc.

7. To READ ADDRESS REGISTER, STATUS or TIME INTERVAL count the respective F0A0, F1A0, F2A0 commands are issued.

8. The next cycle of operation is initiated by ARM followed by a START pulse.