CICADA ENGINEERING SPECIFICATION	DOCUMENT NO. TFTR-10B4-H409
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SUBJECT: Digital Timed Gate	PREPARED BY: J. Montague J. Montague

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REVISIONS

DATE	DESCRIPTION

1. Abstract.

This specification, in conjunction with the referenced documents, sets forth all the characteristics of the Timed Gate module. This document provides a minimum design goal for the module as well as a working document for users.

2. Reference Documents.

2.1. Modular Instrumentation and Digital Interface System (CAMAC), IEEE Standard 583-1975.

2.2. Printed Circuit Board Fabrication Specification, Document TFTR-10A2-H54A.

2.3. Electronics Schematic Specification, Document TFTR-10A2-H55A.

2.4. Printed Circuit Artwork Specification, Document TFTR-10A2-H53A.

2.5. Reliability, Quality Control and Temperature Cycling, Document TFTR-10A2-H58.

2.6. Standard Timing Pulse Specification, Document TFTR-10B4-H57.

2.7. U-Port Adapter and LAM Grader, Document TFTR-10B3-H313.

3. Introduction.

The CAMAC module specified will be used as an interface between elements of the Tokamak Fusion Test Reactor (TFTR) and the Central Instrumentation Control and Data Acquisition (CICADA) computer system. The module will be housed in a CAMAC crate and will be controlled by the CAMAC Dataway (reference 2.1). The module has four independent channels whose outputs are active for a programmable period of time.

4. Basic Features.

The Timed Gate module is a single width module with four independent timing channels whose outputs are active for a programmable period of time. Each channel can be triggered by an input pulse from the auxiliary connector or by a Dataway command. When a channel is triggered, it goes to the ON state. When a channel is in an ON state, the open collector outputs will conduct current. When a channel is in OFF state, these outputs will not conduct current.

The duration of each output ON state will be determined by a timing register which is loaded by Dataway command. Each output channel has its own timing register and independent timing logic.

There will be three outputs per channel. Each channel shall have an open collector, optically isolated output, an open collector driver output and a transformer coupled pulse output.

The transformer coupled pulse output will be triggered when the channel's output goes from the ON state to the OFF state. These outputs are the end-of-gate outputs.

Each channel can be independently enabled and disabled by CAMAC command. When a channel is disabled, it will not respond to external trigger pulses. Dataway trigger commands will automatically enable the appropriate channel. After power turn-on, all channels are disabled.

The module shall use the 1 Megahertz clock signal on Dataway pin P2 to count time durations. Each channel shall be able to use one of four possible clocks: the 1 megahertz signal on P2 or one of three frequencies counted down from this signal in the ratios 1/10, 1/100 or 1/1000. Selection of the clock is accomplished by CAMAC command.

Each channel can be strapped to retrigger. If a channel is in the OFF state (and enabled, in the case of external trigger pulses) when it receives a trigger, the channel will go to the ON state regardless of the retrigger strapping. If a channel is strapped to retrigger and is in the ON state when it receives a trigger, it will restart its counters while staying in the ON state. In this case, the total ON time will be the duration in the time duration register plus the time the channel has already been in the ON state.

If a channel is strapped in the non-retrigger position, the channel will be triggerable only if it is in the OFF state (and enabled, in the case of external trigger pulses), when it receives a trigger. When a channel is in an ON state, it will ignore all trigger commands and external trigger pulses. The ON state duration will be exactly what is in the time duration register.

The module shall have an external stop input. This input will be a Standard Timing Pulse (reference 2.6) and will set all outputs to the OFF state. When the module receives an external stop pulse, all outputs in the ON state will be set to the OFF state, but no end-of-gate signals will be transmitted.

The module shall respond to the commands as follows:

Command	Description	Code
1	Initialize or Clear	Z+C
2	Read Status Register	F(0).A(*)
3	Read Time Duration	F(1).A(*)
4	Read Clock Selection	F(2).A(*)
5	Read Module ID Number	F(6).A(0)
6	Write Time Duration	F(16).A(*)
7	Write Clock Selection	F(17).A(*)
8	Selective Trigger	F(18).A(0)
9	Selective Enable Channels	F(19).A(0)
10	Load and Go	F(20).A(*)
11	Selective Stop	F(21).A(0)
12	Selective Disable Channels	F(22).A(0)
13	Enable All Channels	F(26).A(0)

* Refers to subaddresses 0 to 3.

5. Mechanical Characteristics.

5.1. The module must conform to the mechanical specifications as indicated in reference 2.1.

5.2. The module shall be a single (1x) width CAMAC module.

5.3. The electrical components of this module must be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA Type FR-4 or equivalent. See reference 2.2.

5.4. This module must contain all necessary mechanical components for insertion into a standard CAMAC crate as per reference 2.1.

5.5. All components must be identified with a standard manufacturer's part number or standard method of marking (e.g. resistor color coding).

5.6. All electrical components must be mounted on only one side of the board.

5.7. The state of this module must be monitored by LEDs located on the module's front panel. See Figure 11.1 for the suggested front panel layout. All lettering on the front panel must be either engraved or silkscreened. The front panel material must be aluminum with an iridite finish with contrasting colored lettering.

5.8. All components must be assigned an identifying part name (e.g. R1, C2, etc.) which must be cross-referenced to the manufacturer's part number on the corresponding electrical schematic as indicated in references 2.3 and 2.4.

5.9. All hardware straps must be accessible from the component side of the board when the cover panel is in place.

5.10. The 36 pin edge connector must mate with a Viking 3V18 connector (or equivalent). The card edge connector must be marked with pin 1 on top and pin 18 on the bottom on each side of the card. Pin assignments shall be as shown in figure 11.2.

6. Electrical Characteristics.

6.1. The module shall conform to electrical specifications as indicated in reference 2.1.

6.2. Input Power shall be derived from the standard ±6 and ±24 volt CAMAC supply voltages. Whenever possible, low power circuitry (such as the 74LS series) shall be used.

6.3. The -6 and +6 supply voltages must be bypassed with electrolytic capacitors of at least 33 microfarads. The -24 and +24 supply voltages must be bypassed with electrolytic capacitors of at least 6.8 microfarads. At least one half the integrated circuits must have a ceramic bypass capacitor of at least 0.01 microfarads on their supply voltage lines. The 0.01 microfarad capacitors should be located as close as possible to the integrated circuits and equally distributed across the board.

6.4. All components on this module must have a MTBF rating as specified in reference 2.5.

6.5. The module must be designed so that if any hardware strapping is set incorrectly, the module will not sustain internal physical damage. The status of all hardware straps must be accessible from the Dataway.

6.6. When the module is powered off, all the outputs shall be in the OFF state. The outputs will remain in the OFF state during power turn-on. The voltage in the transformer coupled outputs will remain below 0.8 volts. After power turn-on, all channels will be disabled. After power turn on, all outputs will remain in the OFF state until they are enabled and triggered.

6.7. The module uses the 1 Megahertz clock signal on Dataway pin P2 to count time durations (reference 2.7). Each channel shall be able to use one of four possible clocks: the 1 megahertz signal on P2 or one of three frequencies counted down from this signal in the ratios 1/10, 1/100 or 1/1000. Selection of the clock is accomplished by CAMAC command. The clock on P2 has the following characteristics.

	Min	Max	
High level voltage	3.0	5.5	volts
Low level voltage	0.0	0.8	volts
Frequency	0.8	1.6	megahertz
Rise and fall times		50	nanoseconds
High voltage pulse width	200		nanoseconds
Low voltage pulse width	200		nanoseconds
Current (sink)		1.5	milliamps

6.8. The module shall have an external stop input. This input will be a Standard Timing Pulse (reference 2.6) and will set all outputs to the OFF state. When the module receives an external stop pulse, all outputs in the ON state will be set to the OFF state, but no end-of-gate signals will be transmitted.

6.9. Each channel can be triggered independently by an external input pulse from the auxiliary connector. Pin assignments shall be as shown in figure 11.2.

6.10. There are two types of input signals, trigger pulses and the stop pulse. These input pulses are Standard Timing Pulses as per reference 2.6. These input pulses are received through the auxiliary connector as per figure 11.2. These inputs are transformer coupled and terminated in 100 ohms. Typical circuitry for these inputs is shown in figure 11.3. These inputs shall respond to pulses which have the following characteristics:

	Min	Max	
High level voltage	3.0	5.5	volts
Low level voltage	-0.7	0.8	volts
Rise and fall times		50	nanoseconds
High voltage pulse width	0.9	1.1	microseconds

6.11. Each channel has a transformer coupled output signal that occurs when the channel goes from the ON state to the OFF state, except when a external stop pulse is received. See paragraph 6.7. These outputs are the end-of-gate outputs.

6.12. The end-of-gate output signals are Standard Timing Pulses as per reference 2.6 and are available on the auxiliary connector. See figure 11.2. Typical circuitry for these outputs is shown in figure 11.3. These outputs must have the following characteristics:

	Min	Max	
High level voltage	4.0	5.5	volts
Low level voltage	-0.7	0.8	volts
Rise and fall times		50	nanoseconds
High voltage pulse width	0.9	1.1	microseconds
Output Current		50	milliamps

6.13. A channel is in the ON state when the open collector output will conduct current. A channel is in the OFF state when the open collector output will not conduct current.

6.14. The optically isolated open collector outputs must be isolated to ±1.0 KV with respect to ground (continuous) and ±1.5KV for 100 nanosecond surges. Typical circuitry for these outputs is shown in figure 11.3. These outputs must be rated for the following:

Output Transistor Collector to Emitter	Maximum
Breakdown Voltage	30 VDC
Saturation Voltage at 16 mAmps collector current	0.7 volts
Leakage current with no diode current	10 microamps
Collector current of 16 mA	
Rise Time	5 microseconds
Fall Time	5 microseconds

Maximum collector current of at least 16 milliamps.

6.15. The open collector driver outputs must have the following characteristics:

Output Transistor Collector to Emitter	Maximum
Breakdown Voltage	30 VDC
Saturation Voltage at 16 mAmps collector current	0.7 volts
Transistor off leakage current	50 microamps
Collector current of 16 mA	
Rise Time	50 nanoseconds
Fall Time	50 nanoseconds

Maximum collector current of at least 16 milliamps.

6.16. Each output channel can count up to 1,048,575 clock periods (period of the selected clock). The accuracy of the outputs shall be measured in P2 clock periods which are specified in paragraph 6.6.

The accuracy of the output ON duration shall be ± 1 P2 clock period and shall be measured from the leading edge of the trigger pulse to the leading edge of the end-of-gate pulse.

The maximum time delay between the leading edge of the trigger pulse and the leading edge of the opto-isolator output shall be 5.0 microseconds. The maximum time delay between the leading edge of the end-of-gate pulse and the trailing edge of the opto-isolator output shall be 10.0 microseconds.

The maximum time delay from the leading edge of the trigger pulse to the leading edge of the open collector output shall be 500 nanoseconds. The maximum time delay between the leading edge of the end-of-gate pulse and the trailing edge of the open collector output shall be 500 nanoseconds.

6.17. Each channel can be strapped to retrigger. If a channel is enabled and strapped to retrigger, it will always respond to trigger commands and external trigger pulse inputs. If the channel is in the OFF state when it receives a trigger, it will go to the ON state for the duration in the time duration register (unless it is retriggered). If the channel is in the ON state, it will begin the cycle again and add the duration in the time duration register to the ON time without going to the OFF state. When a channel is retriggered, the total ON time

will be the duration in the time duration register plus the time the channel has already been in the ON state.

6.18. If a channel is strapped in the non-retrigger position and the channel is in the ON state, it will ignore all trigger commands and external trigger pulses. The ON state duration will be exactly what is in the duration register. The channel will be triggerable only if it is in the OFF state (and enabled, in the case of external trigger pulses), when the trigger is received.

6.19. The module returns an X signal equal to one for all commands it is equipped to perform.

6.20. CAMAC Command Description.

6.20.1. Command #1. Initialize or Clear [Z+C]

These commands must set all outputs to the OFF state and disable all channels.

6.20.2. Command #2. Read Status Register [F(0).A(*)]

This command gates the status register for the assigned channel to the Dataway read lines R1 through R3. The channel is assigned by the subaddress A(*) where the asterisk is a subaddress 0 through 3. R4 through R24 must be zero for this command. The module returns Q equal to one each time it receives this command.

Bit R1 of this register monitors the ON status of the channel. If the channel is in the ON state, bit R1 will be a logical one. If the channel is in the OFF state, bit R1 will be a logical zero.

Bit R2 of this register monitors the channel enable status. If the channel is enabled, bit R2 will be a logical one. If the channel is disabled, bit R2 will be a logical zero.

Bit R3 monitors the retrigger strapping status. If the channel is strapped to retrigger, bit R3 will be a logical one. If the channel is not strapped to retrigger, bit R3 will be a logical zero.

6.20.3. Command #3. Read Time Duration [F(1).A(*)]

This command gates the time duration register onto Dataway lines R1 through R20 for the assigned channel. Lines R21 through R24 must be zero for this command. The channel is assigned by the subaddress A(*) where the asterisk is a

subaddress 0 through 3. Channel 1 is at subaddress 0. The information on lines R1 through R20 is the output ON state duration in binary format with the least significant bit on R1. The module returns Q equal to one each time it receives this command.

If the time duration register contains B2196 in hexadecimal and the clock selection register contains 3, the output will be in the ON state for 12 minutes and 9.494 seconds.

6.20.4. Command #4. Read Clock Selection [F(2).A(*)]

This command gates the clock selection register onto Dataway lines R1 through R2 for the assigned channel. The channel is assigned by the subaddress A(*) where the asterisk is a subaddress 0 through 3. Channel 1 is at subaddress 0. R3 through R24 must be zero for this command. The module returns Q equal to one each time it receives this command. The information on lines R1 and R2 determines the assigned clock as shown below.

Clock	R2	R1	Delay Units
1MHz	0	0	1 microsecond
100KHz	0	1	10 microseconds
10KHz	1	0	100 microseconds
1KHz	1	1	1 millisecond

If the time duration register contains B2196 in hexadecimal and the clock selection register contains 3, the output will be in the ON state for 12 minutes and 9.494 seconds.

6.20.5. Command #5. Read Module ID Number [F(6).A(0)]

This command gates the identification number (decimal 409, 199_{16}) onto the read lines R1 through R12 with the least significant bit on R1. R13 through R24 must be zero for this command. The module returns Q equal to one each time it receives this command.

6.20.6. Command #6. Write Time Duration [F(16).A(*)]

This command loads the information on Dataway lines W1 through W20 to set the time duration for the assigned channel. The channel is assigned by the subaddress A(*) where the asterisk is a subaddress 0 through 3. Channel 1 is at subaddress 0. The information on lines W1 through W20 is the output ON state duration in binary format with the least significant bit on W1. The module returns Q equal to one each time it receives this command.

If the time duration register contains F600E in hexadecimal and the clock selection register contains 2, the output will be in the ON state for 1 minute and 40.763 seconds.

6.20.7. Command #7. Write Clock Selection [F(17).A(*)]

This command loads the information on Dataway lines W1 through W2 to set the clock for the assigned channel. The channel is assigned by the subaddress A(*) where the asterisk is a subaddress 0 through 3. Channel 1 is at subaddress 0. The module returns Q equal to one each time it receives this command. The information on lines W1 and W2 determines the assigned clock as shown below.

Clock	W2	W1	Delay Units
1MHz	0	0	1 microsecond
100KHz	0	1	10 microseconds
10KHz	1	0	100 microseconds
1KHz	1	1	1 millisecond

If the time duration register contains F600E in hexadecimal and the clock selection register contains 2, the output will be in the ON state for 1 minute and 40.763 seconds.

6.20.8. Command #8. Selective Trigger [F(18).A(0)]

This command loads the write lines W1 through W4 to independently enable and trigger the timing channels, where W1 corresponds to channel 1. For those channels in the OFF state, if a write line is a logical one, the corresponding channel will be enabled, triggered, go to the ON state for the amount of time specified in the time duration register for the channel (unless it is retriggered). In this case, the module returns Q equal to one each time it receives this command.

For those channels strapped to retrigger and already in the ON state, if a write line is a logical one, the corresponding channel will be enabled and triggered. The total channel ON time will be the duration in the time duration register plus the time the channel has already been in the ON state. In this case, the module returns Q equal to one each time it receives this command.

For those channels not strapped to retrigger and already in the ON state, if a write line is a logical one, the corresponding channel will not be affected, but the module will return a Q signal equal to zero. In this case, this command will not affect the current ON time duration. The module

will return a Q signal equal to zero if any of the four write lines is trying to trigger a channel in the ON state if that channel is not strapped to retrigger.

The write lines that are logical zero will have no effect on any outputs.

6.20.9. Command #9. Selective Enable Channels [F(19).A(0)]

This command loads the write lines W1 through W4 into the channel enables, where W1 corresponds to channel 1. If a write line is a logical one, the corresponding channel will be enabled and will respond to trigger signals. The module returns Q equal to one each time it receives this command.

The write lines that are logical zero will have no effect on the status of the channel enables.

6.20.10. Command #10. Load and Go [F(20).A(*)]

This command loads the information on Dataway lines W1 through W20 to set the time duration register for the assigned channel, it enables the assigned channel and triggers it. The channel is assigned by the subaddress A(*) where the asterisk is a subaddress 0 through 3. Channel 1 is at subaddress 0. The information on lines W1 through W20 is the output ON state duration in binary format with the least significant bit on W1. The time duration register is enabled and loaded with data at S1 and the corresponding channel is triggered at S2.

For those channels in the OFF state, this command will load the time duration register, enable the channel and trigger the channel. In this case, the module returns Q equal to one each time it receives this command.

For those channels strapped to retrigger and already in the ON state, this command will load the time duration register, enable and trigger the channel. The total channel ON time will be the new duration in the time duration register plus the time the channel has already been in the ON state. In this case, the module returns Q equal to one each time it receives this command.

For those channels not strapped to retrigger and already in the ON state, the module will ignore this command and return Q equal to zero. In this case, this command will not affect the current ON time duration.

If the time duration register contains E7439 in hexadecimal and the clock selection register contains 0, the output will be in the ON state for 947.257 milliseconds.

6.20.11. Command #11. Selective Stop [F(21).A(0)]

This command loads the write lines W1 through W4 to stop the timing channels, where W1 corresponds to channel 1. If a write line is a logical one, the corresponding channel will be set to the OFF state. If the channel is in the ON state when it receives this command, it will go to the OFF state and output an end-of-gate signal.

The write lines that are logical zero will have no effect on any outputs.

6.20.12. Command #12. Selective Disable Channels [F(22).A(0)]

This command loads the write lines W1 through W4 into the channel disables, where W1 corresponds to channel 1. If a write line is a logical one, the corresponding channel will be disabled and the channel will not respond to external trigger pulses. If the channel is disabled while it is in an ON state, the channel will complete the current time duration and output an end-of-gate pulse, but an external trigger pulse will not be able to retrigger the channel.

The write lines that are logical zero will have no effect on the status of the channel enables.

6.20.13. Command #13. Enable All Channels [F(26).A(0)]

This command enables all four channels. All channels will respond to external trigger pulses after the module receives this command. The module returns Q equal to one each time it receives this command.

6.21. The N LED shall go on for at least 100 milliseconds when the module receives an N signal.

6.22. Each channel shall have a monitoring LED on the front panel. Each LED will be on whenever the corresponding channel is in the ON state. However, each LED will go on for a minimum of 100 milliseconds each time it goes on.

6.23. Each channel shall have an LED monitor the state of the channel enables. The LED will be on if the channel is enabled.

6.24. Each channel shall have an LED monitor the state of the retrigger strapping. The LED will be on if the channel is strapped to retrigger.

7. Enviromental Data.

7.1. The module must operate, as defined, over an ambient temperature range of 0 to +50 degrees C.

7.2. The module must operate, as defined, over a relative humidty range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3. The module must operate, as defined, in an external magnetic field changing at a maximum rate of 200 gauss per second with a peak of 100 gauss in any direction.

7.4. The module must operate, as defined, in a radiation environment as follows:

Neutrons: 2×10^{7} n/cm^{2}/sec

Rad-Dose: 5×10^{-2} rad (Si)/sec

Integrated Dose: 200 rad (Si)

8. Safety.

All components used in this module must be of flame retardant materal.

9. Testing.

9.1. The module shall undergo all tests normally performed by the seller. A description of the tests to be performed shall be furnished by the seller.

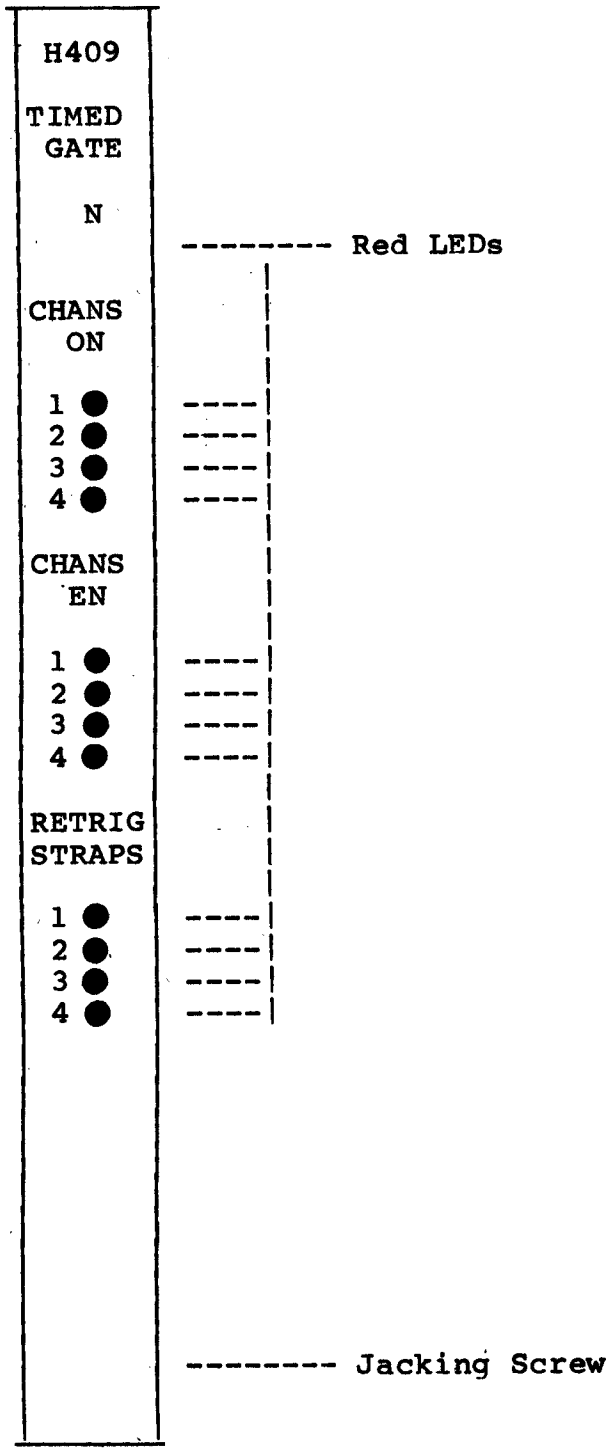
9.2. The module under test must be tested in a CAMAC crate equipped with $\pm$6 and $\pm$24 volts supplied via a standard CAMAC power supply.

9.3. The Dataway signals and timing must meet the conditions specified in reference 2.1.

9.4. Tests will be performed after temperature cycling.

10. Reliability and Quality Control.

10.1. This equipment meets all applicable requirements specified in reference 2.5.



Front Panel Layout

Figure 11.1

Transformer Coupled Inputs

	Signal	Return
Channel 1	1B	1A
Channel 2	2B	2A
Channel 3	3B	3A
Channel 4	4B	4A

Transformer Coupled Outputs

	Signal	Return
Channel 1	5B	5A
Channel 2	6B	6A
Channel 3	7B	7A
Channel 4	8B	8A

Optoisolator Outputs

	Collector	Emitter
Channel 1	9B	9A
Channel 2	10B	10A
Channel 3	11B	11A
Channel 4	12B	12A

Open Collector Driver Outputs

	Signal	Ground
Channel 1	13B	13A
Channel 2	14B	14A
Channel 3	15B	15A
Channel 4	16B	16A

Stop Input

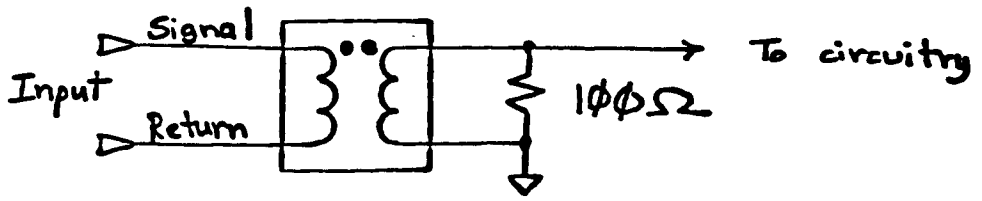
Signal	Return
17B	17A

*B - Component side of board

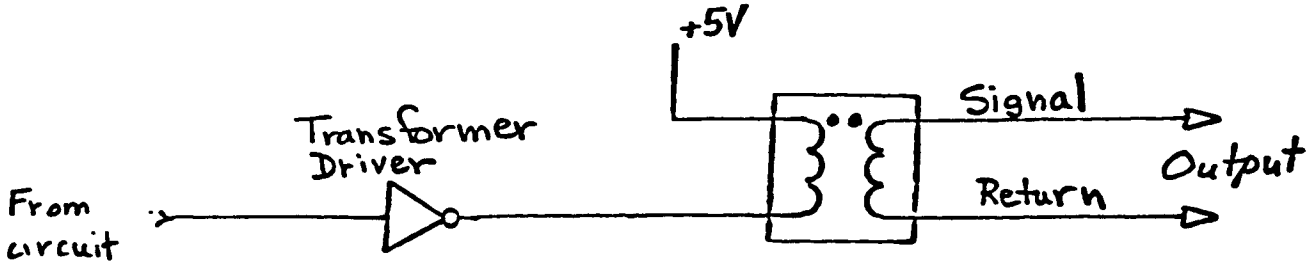
Auxiliary Connector Pin Allocation

Figure 11.2

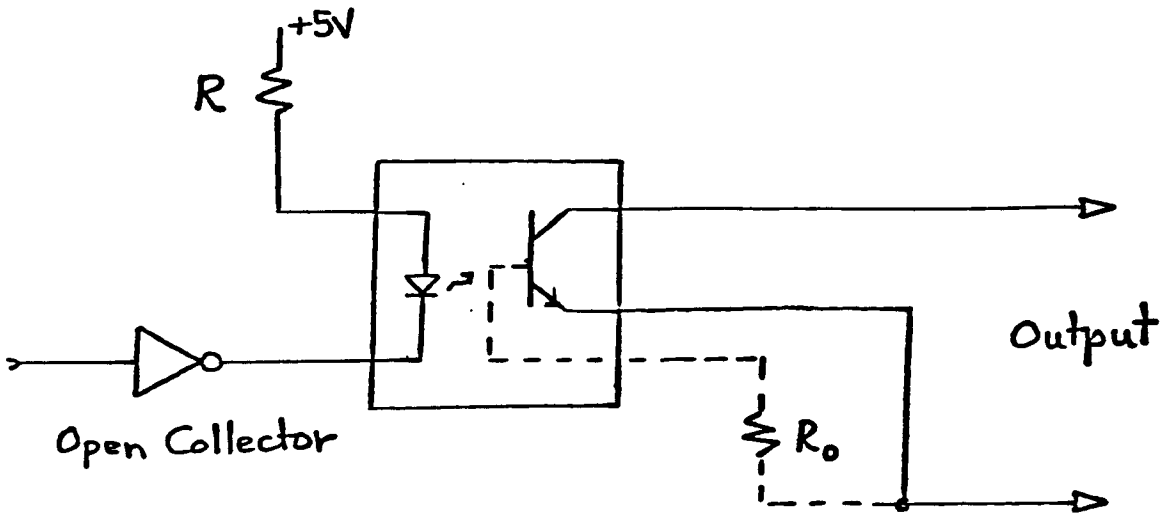
Transformer Coupled Input



Transformer Coupled Output



Opto-isolator Output



Typical Input and Output Circuitry

Figure 11.3

APPENDIX A

This section is a example of a software sequence which correctly sets up the Timed Gate module. This is not the only possible sequence.

If the Timed Gate is being initialized for a TFTR pulse, the time duration and clock registers are entered when the Device Setting event occurs.

		Data
Write Time Duration	F(16).A(*)	0F FF FF
Write Clock Selection	F(17).A(*)	00 00 03

When the arming event occurs, the appropriate channels should be enabled. F(26).A(0) will enable all the channels. F(19).A(0) will enable individual channels.

		Data
Enable Channels	F(19).A(0)	00 00 0F
or		
Enable All Channels	F(26).A(0)	

The enabled channels will be subsequently triggered by external trigger pulses.

P2 GLITCH PROBLEM

John Wertenbaker 3/17/00

It was discovered that the P2 line on the CAMAC dataway can contain glitches that are caused by the capacitive coupling of the 1Mhz P2 line and the function (F) lines. The F(16) line, which is just opposite of P2 has the greatest coupling, but the more F lines that are active, the larger the glitch will be on P2. This glitch can vary from crate to crate, and from slot to slot, but, in one case it was measured at 2 volts.

The glitch can cause any module that uses the P2 line, like the 408, 409, 412, 413, and 908 modules, to count an extra clock pulse, causing timing errors in any system that uses those modules. Below is a list of the modules that derive their clock from the P2 line, and a description of the input circuitry in each module.

408 P2 input goes to a 74LS28, which is a NOR gate.
409 P2 input goes to a 74123 one-shot.
412 P2 input goes to a 74LS38, which is a NAND gate.
413 P2 input goes to a 74LS02.
904 P2 input goes to a 74LS14 Schmitt-trigger inverter.
908 P2 input goes to 3 74LS74's and 2 74LS08's.
910 P2 input goes to a 74LS14 Schmitt-trigger inverter.
912R P2 input goes to a 74LS14 Schmitt-trigger inverter.
914 does not use the P2 line.

The 409 Timed Gate module was the only module that was tested and proven to be susceptible to this glitch. The 408, 412, 413, and 908 modules are assumed to be susceptible, also, based on their input circuitry. The 904, 910, and 912R modules are much more tolerant of this glitch, due to the Schmitt-trigger inputs, and are probably not affected. The 914 module generates its own 1Mhz, and is independent of the P2 line.

This occurrence of this problem is rare due to the nature of clock cycles in NSTX, and its predecessor, TFTR. In those machines, most modules are set up and armed long before any trigger pulse starts the counting of P2 clock pulses. Very few CAMAC commands are performed after these arm and setup commands. In most cases, the only commands that come through during the counting times are read-back commands and L-2 crate controller wakeup commands. These happened every 2 seconds in TFTR, and even less often than that in NSTX. Also, most of the time, the 1Mhz P2 line is divided down to a much lower frequency, so a few microseconds of inaccuracy would not be noticed.

For the rare cases when the glitches can cause problems, such as the Facility Clock Generator crates, the recommended fix is to insert a P2 Capacitor Filter Module in the crate as close as possible to the module that uses the P2 line. This module contains a 1000pf capacitor from the P2 line to ground. This attenuates the high frequency of the glitch, without seriously rounding off the edges of the 1Mhz P2 signal.

It should be noted that the 404A had a similar problem with the P1 line. The BUSY line, which is an un-terminated line in the crate, was coupling a glitch over to the P1 line. The repair for that problem was to install a Schottky diode on the BUSY line to clamp the negative-going overshoot at the low-going transition of the BUSY pulse, and replace the 74LS04 with a Schmitt-trigger 74LS14 at the P1 input. However, it was not considered practical to modify every module that uses the P2 line because the problem is much more rare than the P1 problem, due to the nature of when the glitch occurs.