TYPE 2 TRANSIENT DIGITIZER (SINGLE CHANNEL)

1. ABSTRACT

This specification, in conjunction with referenced documents, sets forth all characteristics of subject module. This specification shall take precedence where areas of overlap with referenced documents occur. The intended use of this document is to provide a minimum design goal for the module as well as a working document for subsequent users.

2. REFERENCE DOCUMENTS

2.1. IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Std. 583-1975.

2.2. Printed Circuit Board Fabrication and Assembly Specification, CICADA Handbook Volume I TFTR-10A2-H54B.

2.3. Electronic Schematic Specification, CICADA Handbook Volume I, TFTR-10A2-H55

2.4. Printed Circuit Artwork Specification, CICADA Handbook Volume I, TFTR-10A2-H53A.

2.5. Reliability, Quality Control and Temperature Cycling, CICADA Handbook Volume I, TFTR-10A2-H58.

2.6. Standard Timing Pulse, CICADA Handbook Volume I, TFTR-10A2-H57.

2.7. Facility Clock Subsystem, CICADA Handbook Volume I,TFTR-10B4-H401.

2.8. Remote Memory Module, CICADA Handbook Volume I, TFTR-10C6-H903

2.9. Controller Module, CICADA Handbook Volume I, TFTR-10C6-H912

3. INTRODUCTION

The CAMAC module specified will be used as an interface between elements of the Tokamak Fusion Test Reactor (TFTR) and the Central Instrumentation Control and Data Acquisition (CICADA) computer system. The module will be housed in a CAMAC crate (Reference 2.1). The module will function as a l2 bit ADC device capable of operating at rates up to 500 KHz.

4. BASIC FEATURES

4.1 Memory Loading

The module shall be a single width CAMAC module that shall operate in conjunction with an external controller module (see Reference 2.9). The module shall contain a 12 Bit high speed analog to digital converter system, 8K of internal memory, a self test wave generator, and a CAMAC Dataway interface. In addition, the module shall be capable of having its internal memory disabled and use external memory modules connected through its rear auxiliary connector. The module shall utilize connectors on the front panel for analog input and for command input signals from a controller module. In response to a "convert" pulse signal sensed at the front panel connector (control port), the module shall perform a twelve bit conversion on its analog input, present this data to its companion memory (8K internal or external), and issue a write strobe to load the data into the memory. The module shall not be capable of controlling the memory address lines and thus requires that a controller module perform this function. When the internal memory array is used, the module will use the absolute address available at its rear connector for its internal memory.

4.2 Memory Unloading

Unloading of the system memory will be accomplished through the Digitizer module under control of the Controller module. Each Digitizer in a system must be assigned a unique channel address from 1 to 15. This address shall be set by PC mount switches on the Digitizer module. The unload channel address shall be implemented through the use of four (4) dedicated lines on the front panel control port. During data acquisition sequences, this four bit address will be set

for address zero. This zero address shall cause all Digitizers to operate in their data acquisition mode and allow response to the "convert" command pulse. Whenever any address other than the zero address is present on this 4-bit bus then all Digitizers shall cease to operate in the data acquisition mode. The Digitizer module whose address is sensed (1 to 15) will then respond to "read" command pulses from the control port by enabling the data currently on its Data bus to be imposed upon the CAMAC read lines. The data transferred will be either from its internal memory array or from the external memory data bus, depending upon how the module is configured. During unload sequences, the module will have no control of the absolute memory address. As with data acquisition sequences, the module shall use the externally supplied address from its rear connector for its internal memory when this memory is used.

4.3 CAMAC Commands

The module shall include CAMAC decoding circuitry for the purpose of responding to three (3) CAMAC commands. The module shall respond to commands, "Read Module ID," "Read Module Status," and "Read Last Data" (real time readout).

The module shall maintain a dedicated register to allow the transfer of the value of the last converted data onto the Dataway. This register shall be reloaded whenever a new data word is acquired and shall be available for readout onto the Dataway during all modes of operation.

4.4 Self Test Feature

The module shall have a relay switching system on the analog input port to allow an alternate (self test) input to be used. The analog input circuit shall be switched to two dedicated pins on the command bus connector in response to a self test command from the command bus connector. Whenever the "self test" command signal is present, the normal analog input port shall be open circuited and the analog input circuit shall be connected to the self test input signal.

5. MECHANICAL CHARACTERISTICS

5.1 The module will conform to mechanical specifications as indicated in Reference 2.1.

5.2 The module shall be a single width CAMAC module.

5.3 The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA Type FR-4 or equivalent. The circuit board shall be a two sided printed circuit board with etched conductors. The fabrication of the circuit board shall be in compliance with Reference 2.2.

5.4 All components are to be identified with a standard manufacturer's part number or standard method of marking (e.g., resistor color coding) and shall have an exact replacement available from a second source manufacturer whenever possible.

5.5 This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate. See Reference specification 2.1.

5.6 All electrical components are to be mounted on only one side of the board.

5.7 The condition of this module is to be monitored by LED's located on the module front panel. See Figure 11.1 for the suggested front panel layout. All lettering on the front panel shall be either engraved or silkscreened. The front panel material shall be aluminum with an iridite finish with contrasting colored lettering.

5.8 All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part number on the electronic schematic associated with this module. See Reference specifications 2.3 and 2.4.

5.9 The front panel connectors J1 and J2 shall be used for analog input and for control input, respectively. J1 shall be a three pin LEMO connector. J2 shall be a 20-position double row right angle header with latch. The rear auxiliary connector shall be used for connection to the module controller and/or external memory modules. Pin assignments for the connectors are given in Figures 11.2 and 11.3.

5.10 The mechanical construction of the module shall be designed to facilitate calibration and maintenance. All switches, pots, and jumpers must be accessible without module disassembly.

5.11 The module shall be equipped with grounded, conductive side panels.

6. ELECTRICAL CHARACTERISTICS

6.1 Dataway Interface shall conform to specification as indicated in Reference 2.1.

6.2 Input Power shall be derived from the standard +/- 6 volt and +/- 24 volt CAMAC supply voltages. Whenever possible, low power circuitry (such as the 74LS series) shall be used.

6.3 The +6 and -6 supply voltages must be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages must be bypassed with electrolytic capacitors of at least 6.8 microfarads. In addition, at least half the integrated circuits must contain a ceramic bypass capacitor of at least .01 microfarads on their supply voltage lines. The .01 microfarad capacitors should be distributed on the circuit board and be located as close as possible to noise sensitive components.

6.4 All components on this module must have a MTBF rating as specified in Reference 2.5.

6.5 Analog Input Characteristics:

6.5.1 The analog input shall be a differential input and shall utilize a high impedance differential amplifier (10 meg ohm minimum) shunted by an appropriate resistor to obtain an impedance of 10,000 ohms +/- 1% from DC to 200KHz.

6.5.2 The input range shall be selectable through use of printed circuit mounted DIP switches. Selectable ranges shall be for full scale differential voltages:

0 to +10.237
0 to +5.118

-10.240 to +10.235
-5.120 to +5.118

6.5.3 Common Mode Rejection Ratio:
DC - 1KHz 60 db minimum
1KHz - 200khz 40 db minimum

6.5.4 Bandwidth:
The module gain shall be +/- 0.10db from DC to 200KHz and roll off at the rate of no greater than 6 db/octave for frequencies above 200 KHz. Filter requirements for specific application shall be installed external to the module to avoid aliasing.

6.5.5 The module shall operate as specified under conditions of common mode voltage offset, providing that the voltage on any input does not exceed +/- 15 volts, as referenced to ground.

6.5.6 Overvoltage:
The module shall be capable of withstanding a DC input voltage of up to +/- 100 volts without sustaining damage except to the protective input resistors. The module will recover to specified accuracy within 100 milliseconds following a maximum specified overvoltage condition (100 volts) which lasts for a duration of one hundred (100) milli-seconds or less.

6.6 Module Conversion Characteristics

6.6.1 Resolution: 12 bits

6.6.2 Absolute Accuracy at 20 deg C: +/- 0.1% of FS +/- 1/2 LSB maximum

6.6.3 Nonlinearity: +/- 1/2 LSB maximum

6.6.4 Temperature Coefficient of Gain: +/- 40 PPM/deg C maximum

6.6.5 Conversion Time 2.0 microsecond maximum

6.6.6 Throughput Up to and including 500,000 samples/second

6.6.7 Output Coding

The data output coding for transfer onto the Dataway read lines shall be implemented in two's complement format, with the sign extended to sixteen (16) bits. The module shall provide DIP switches or movable jumpers to accomplish the sign extension for either unipolar or bipolar utilization of the ADC. Bit weighting for data returned shall always be .00125 volt/bit. When the module is set to operate with a nominal full scale swing of ten (10) volts the least significant bit (LSB) shall always be set to zero.

UNIPOLAR (0V to +10.24V)

SCALE	VOLTAGE	BINARY CODE
+FS - 1 LSB	+10.237 V	0001 1111 1111 1110
+ 1/2 FS	+ 5.120 V	0001 0000 0000 0000
0	0.000 V	0000 0000 0000 0000

UNIPOLAR (0V to +5.12V)

SCALE	VOLTAGE	BINARY CODE
+FS - 1 LSB	5.118 V	0000 1111 1111 1111
+ 1/2 LSB	2.560 V	0000 1000 0000 0000
0	0.000 V	0000 0000 0000 0000

BIPOLAR (-10.24V to +10.235V)

SCALE	VOLTAGE	BINARY CODE
+FS-12SB	10.23S	0001 1111 1111 1100
0	0.000	0000 0000 0000 0000
-FS	-10.240	1110 0000 0000 0000

BIPOLAR (-5.1200V to +5.1175V)

SCALE	VOLTAGE	BINARY CODE
+FS - 1 LSB	+ 5.117 V	0000 1111 1111 1110
0	0.000 V	0000 0000 0000 0000
-FS	- 5.120 V	1111 0000 0000 0000

It should be noted that the interpretation and subsequent conversion of the binary data to engineering units (software routines) will always be done in the same way without regard to the scale setting.

6.7 Memory Control

The module shall use a 36 position rear card edge connector (standard auxiliary connector) to facilitate memory control. This connector shall provide a twenty (20) bit address bus, a twelve (12) bit data bus as well as read and write strobes (see Figure 11.3).

When the module is configured, through the use of PC mount switches for internal memory only, the 8K words of internal memory may be used. While operating in this configuration, the module shall use the thirteen LSB's of the address bus (ABO-AB12) from the auxiliary connector for its internal memory array. The module circuitry will simply buffer this address and impose the address directly onto its memory components. This address shall not be latched in the module and thus will require that the address supplied externally be stable during read and write cycles. The module will not use the seven MSB's (AB13 - AB19) of the address bus for internal memory operations (these bits will be ignored by the module circuitry). The signal convention for the rear auxiliary connector shall be TTL level and the logic convention for the address lines shall be "high true." The module data bus interface to the auxiliary connector shall use tristate drivers to allow the use of up to thirty two (32) auxiliary memory modules. When the Digitizer module is receiving data from external memory modules (during unload periods), the module shall impose a load of no more than one standard TTL load on the data bus and the address bus.

6.8 System Timing

The critical parameters for system timing is given by Figure 11.5. Both the signals "convert" and "unload" shall be low true TTL levels. The active edge shall be the high to low transition. During data acquisition, this transition of the "convert" signal shall be used to switch the module's track and hold circuitry from the track to the hold state. The system aperture time delay uncertainty (jitter) shall be less than 500 x 10E-12 seconds for digitizer modules connected to a common controller.

Timing for memory loading and unloading is given in Figure 11.4. During data acquisition, memory loading shall occur during valid address period. During memory unloading, the module shall take the data available at either the rear auxiliary connector data bus or the data available from its internal memory array and impose the data upon the CAMAC Dataway. As delineated in Section 6.6.7, the data must be displaced either 0, 1, or 2 places and must be sign extended to 16 bits for presentation to the Dataway. As shown in Figure 11.4, the module shall cause the Dataway read lines to be driven within 100 x 10E-9 seconds of receipt of the unload command. Memory address data during memory unload sequences shall be valid for at least 500 x 10E-9 seconds prior to and throughout the "unload" command.

6.9. Front Panel "Command" Port

The front panel mounted command port shall be a 20 position header that shall be used in conjunction with a ribbon bus connector string. The pin assignment is given by Figure 11.4. All control signals on the command port shall be TTL level low true. The module shall impose a maximum load of one standard TTL level load on each of the input lines. Two of the pins on the command port shall be used to supply an analog "self test" signal. The self test waveform shall be present whenever the self test command is true (low state).

6.10. Self Test Capability

The module input circuit may be switched over to a self test signal that shall be supplied to the module through the front panel command bus. This self test signal shall be switched through use of a relay(s) and shall cause this differential signal to be routed through all input components. The switch over to this self test signal shall be maintained as long as the self test command on the command is in the true (low) state.

6.11. Status Registers

The module shall maintain two status registers that may be read out by CAMAC command. The specific bit utilization for the registers is given in Section 6.13. In summary, status register 1 shall be used to ascertain the module configuration and operating mode. Status register 2 shall be used to ascertain the value of the last data word acquired.

The binary representation of the last data acquired must be consistent with data readout during normal memory unload (LSB = 1.25 MV, sign extended to 16 Bits). The module circuitry for this readout shall be designed to ensure stable data during all addressed operations. This stability requirement may be implemented by inhibiting the register load signal whenever the CAMAC signal "N" is sensed.

6.12. CAMAC Commands

The module shall accept commands from the CAMAC dataway in compliance with Reference 2.1.

6.12.1. Command 1 Read Status F(0).A(0).(Data Returned)

This command gates the module status onto the dataway read lines. The data returned shall be interpreted as follows:

Bit R1 shall be set whenever the channel address sensed or the command port is zero. (Data Acquisition Mode)

Bit R2 shall be set whenever the channel address sensed or the command port corresponds to the module channel address. (Unload Mode)

Bit R3 shall be set whenever the module is in self test mode.

Bit R4 shall be set when internal memory is used.

Bits R5 - R6 shall indicate module gain setting (full scale)

0 = 0 to 10 Volts (nominal)
1 = 0 to 5 Volts (nominal)
2 = -10 V to +10 Volts (nominal)
3 = -5 V to +5 Volts (nominal)

Bits R7 - R24 always zero

6.12.2. Command 2 Read Last Sample Acquired F(0).A(1).(Data Returned)

This command gates the binary representation of the last value digitized onto the CAMAC read lines R1 - R16 (R17 - R24 always zero). The data shall be

presented in two's complement format with the LSB weight of 1.25 x 10E-3 volts and with the sign extended to 16 bits. The module will respond to this command during all modes of operation.

6.12.3. Command 3 Read Module Number F(6).A(0).(Data Returned)

This command gates the module identification number (decimal 907, hexadecimal 38B) onto the Dataway read lines R1 through R12 (R13 - R24 always zero).

6.12.4. Data Responses Q X

The module will return Q = 1 and X = 1 for all addressed commands that the module is equipped to perform (commands 1 through 3).

The module shall return Q = 0 and X = 0 for any other addressed command.

6.12.5. Common Controls Z, C, I

The module shall have no electrical connection to the signals Z,C, I.

6.13 Front Panel Indicators

The module shall provide four (4) LED indicators mounted for visibility from the front panel.

LED #1 "N" shall illuminate for approximately 100 milliseconds whenever N is received.

LED #2 "LD" shall illuminate for approximately 100 milliseconds whenever a memory load occurs.

LED #3 "UNLD" shall illuminate for approximately 100 milliseconds whenever the module unloads data to the Dataway in response to an unload command from the module control port. (Does not illuminate when unloading a last sample data, Command 2.)

LED #4 "ST" shall illuminate whenever the self test feature is active.

7. ENVIRONMENTAL DATA

7.1 The module must operate, as defined, over an ambient temperature range of 0 to +50 degrees C.

7.2 The module must operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must operate, as defined, in the presence of an external magnetic field changing at a maximum rate of 200 gauss per second with a peak magnitude of 100 gauss in any direction. No components, such as reed relays, with known susceptibility to such magnetic fields shall be used.

7.4 The module must operate, as defined, in a radiation environment as listed below. No components, such as dynamic RAM, with known susceptibility to such radiation shall be used.

Neutrons:	2 x 10 7 N/CM2/sec
Rad-Dose:	5 x 10 -2 rad (Si)/sec
Integrated Dose:	200 rad (Si)

8. SAFETY

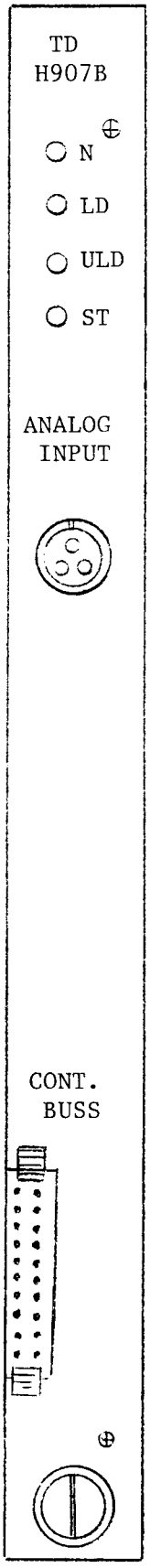
All components of this module must be of flame retardant material.

9. TESTING

All modules shall be subjected to a temperature cycling period followed by a functional test prior to shipment. A description of the tests performed shall be submitted by the vendor for incorporation into this specification.

10. RELIABILITY AND QUALITY CONTROL

The module shall meet all applicable requirements specified in Reference 2.5.



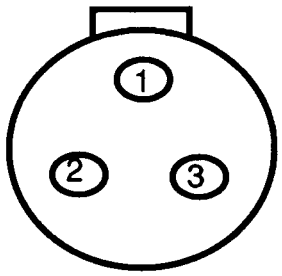
Suggested Front Panel Layout
Figure 11.1

LEMO Type RG0B303 CA22

PIN	TYPE	USE
1	female	*
2	female	signal high
3	female	signal low

Alignment Key

View from solder cup (or crimp) side



Typical Connector Circuitry

* Pin 1 shall be connected to a printed circuit strap jumper to allow connection to the ground through a series .01 microfarad capacitor. The module will be initially shipped with the capacitor installed, and with the jumper not connected.

Figure 11.2

AUXILIARY CONNECTOR

(Viewed from Front of Crate)

PIN	FUNCTION	PIN	FUNCTION
1B	MAB 19	1A	MAB 1
2B	MAB 18	2A	MAB 0
3B	MAB 17	3A	GND
4B	MAB 16	4A	DB 11
5B	MAB 15	5A	DB 10
6B	MAB 14	6A	DB 9
7B	MAB 13	7A	DB 8
8B	MAB 12	8A	DB 7
9B	MAB 11	9A	DB 6
10B	MAB 10	10A	DB 5
11B	MAB 9	11A	DB 4
12B	MAB 8	12A	DB 3
13B	MAB 7	13A	DB 2
14B	MAB 6	14A	DB 1
15B	MAB 5	15A	DB 0
16B	MAB 4	16A	GND
17B	MAB 3	17A	Write Strobe
18B	MAB 2	18A	Read Strobe

AUXILIARY CONNECTOR

PIN ASSIGNMENTS

Figure 11.3

Type 2 Transient Digitizer (Single Channel)

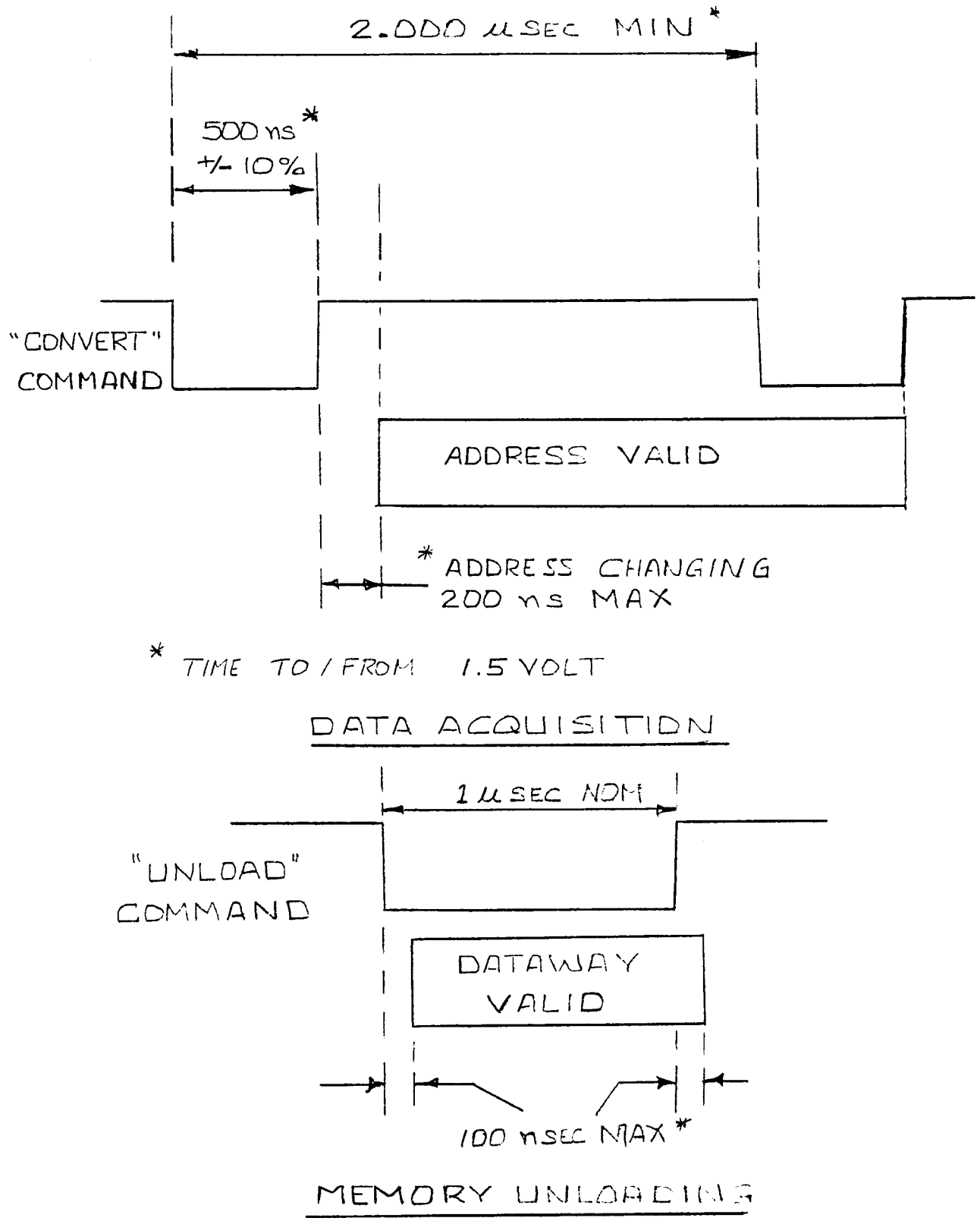
Control Port

Pin Assignment

(Connector As Viewed From Front of Crate)

Pin Number	Function		Pin Number	Function
1	Unload Pulse		2	Ground
3	Self Test Command		4	Ground
5	Chan. Ad(3) MSB		6	Ground
7	Chan. Ad(2)		8	Ground
9	Chan. Ad(1)		10	Ground
11	Chan. Ad(0) LSB		12	Ground
13	"Convert" Pulse		14	Ground
15	Unused		16	Ground
17	Self-Test Low		18	Ground
19	Self-Test High		20	Ground

Figure 11.4



SYSTEM TIMING

FIGURE 11.5