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1.0 Abstract

This specification, in conjunction with referenced documents, sets forth all characteristics of subject module. The intended use of this document is to provide a minimum design goal for the module as well as a working document for subsequent users.

2.0 Reference Documents

2.1 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Std. 583-1975.

2.2 CAMAC - A Modular Instrumentation System for Data Handling. AEC TID-25875.

2.3 Printed Circuit Board Fabrication and Assembly Specification, Document No. TFTR-10A2-H54B.

2.4 Electronic Schematic Specification, Document No. TFTR-10A2-H55.

2.5 Printed Circuit Artwork Specification, Document No. TFTR-10A2-H53A.

2.6 Reliability, Quality Control and Temperature Cycling. Document No. TFTR-10A2-H58.

2.7 Standard Timing Pulse, Document No. TFTR-10A2-H57.

2.8 Facility Clock Subsystem, Document No. TFTR-10B4-H401.

2.9 Remote Memory Module, Document No. TFTR-10C6-H903.

2.10 Time Base Module, Document No. TFTR-10C6-H904.

3.0 Introduction

The CAMAC module specified will be used as an interface between elements of the Tokamak Fusion Test Reactor (TFTR) and the Central Instrumentation Control and Data Acquisition (CICADA) computer system. The module will be housed in a CAMAC crate (reference 2.1). The module will function as a multi-channel 12 bit analog to digital converter to be used as a transient digitizer.

4.0 Basic Features

The module shall be a three (3) wide CAMAC module and will interface to thirty-two (32) differential analog inputs. Each input shall have a dedicated track and hold circuit associated with it to allow "simultaneous" sampling. Analog to digital conversion of thirty-two (32) input voltages shall be accomplished through use of a twelve (12) bit ADC. Digitized input voltages shall be stored in memory modules external to the digitizer (reference 2.9). The module shall have the necessary circuitry to both load the external memory from the ADC output or unload the memory to the CAMAC Dataway. Maximum utilization of available memory for cases where less than thirty-two (32) channels are active shall be implemented through the use of CAMAC command. Through use of CAMAC commands the module may serve as either a pre-trigger or post-trigger device. When operating in the pre-trigger mode, the quantity of post-trigger samples is settable through CAMAC commands.

Module timing and synchronization shall be accomplished through use of an internal oscillator of software selectable frequency or an external clock signal. Module triggering shall be accomplished through use of CAMAC commands or through use of an external trigger pulse signal.

Each input to the module shall be capable of being switched to an internal analog wave form, for the purpose of exercising a self test.

4.1 Analog Features

The module shall provide thirty-two (32) differential input channels. Each channel shall have a dedicated track and hold circuit that will be switched from the track mode to hold mode to provide simultaneity of data for all active channels. Track and hold triggering shall be accomplished through use of either an externally supplied clock or an internal clock of selectable frequency. Through CAMAC command the module may be configured to serve as a 32, 16, 8 or 4 channel device. The minimum allowable sampling clock period shall be a function of the number of active channels and shall be equal to five (5) microseconds per active channel (N) plus five (5) microseconds [$(5N+5) \times 10^{-6}$ seconds]. The maximum sampling rate shall therefore be 40KHz with four (4) active channels and approximately 6KHz with thirty-two (32) active channels.

4.2 Memory Control

4.2.1 Memory Loading

The module shall contain all the circuitry necessary for the control of external memory modules. Memory modules may be connected in parallel to the Digitizer to form an external memory up to 1 megaword deep. Memory loading shall be accomplished sequentially from channel 1 to the last active channel. The number of active channels (4, 8, 16 or 32) shall be loaded into the digitizer through CAMAC command.

4.2.1.1 Post-Trigger Mode

This mode of operation causes the module to fill all of its available memory with data samples after an event trigger. After being armed in this mode the module sets its address pointer to the zero location and awaits an incoming event trigger. After receipt of the trigger the module shall scan the active channel track and hold circuits (4, 8, 16, or 32) and load the ADC data into its available memory. The clock signal that switches the Track and Hold devices into the Hold mode and then starts the digitizing scan may be either of internal or external origin. When the internal digitizing clock is in use the module circuitry shall insure time stability of the first set of data stored (4, 8, 16, or 32 data words) and the incoming event trigger. The internal clocking circuit shall be designed so that the first data set shall be sampled at a fixed and repeatable time after the event trigger with a maximum value of one clock period (selected clock as per paragraph 4.2.4) after the event trigger. The accuracy of this first time interval (clock jitter) shall be less than one microsecond (1×10^{-6} second).

The digitizing sequence shall continue until such time as the entire available memory has been filled with new data or such time as the sequence is terminated by CAMAC command (see paragraph 6.13.8, Command #8). At the conclusion of the sequence, the module shall set an internal "End of Record" (EOR) flag and then ignore subsequent clocks and triggers until it is rearmed by CAMAC command.

The number of active channels to be scanned by the digitizer shall be determined by bits of a status register loaded by CAMAC command. The size of the external memory available to the module shall be determined by board mounted switches.

4.2.1.2 Pre-Trigger Mode

This mode of operation allows the user, through CAMAC command, to retain selectable quantities of data that were digitized both before and after the receipt of the event trigger. At the conclusion of a typical sequence the entire available memory will be filled with new data with part of the data recorded before event trigger and part after event trigger.

When armed in the pre-trigger mode by CAMAC command (paragraph 6.13.6, Command #6) the module shall immediately commence loading memory in response to the selected digitizing clock (either internal or external). The memory shall be loaded in a round-robin fashion as the memory overwrites itself to provide continuous data file of the digitizing analog inputs. The memory size and the number of active channels is determined in the same fashion as in post-trigger mode (paragraph 4.2.1.1). Upon receipt of an event trigger the module will continue the digitizing sequence until the preselected number of post-trigger samples are taken. The number of post-trigger samples required will be determined by CAMAC command as the module is initially armed (paragraph 6.13.6, Command #6). The memory overwriting sequence shall be terminated, the EOR flag set and the next address saved, after an event trigger and after the required number of post-trigger samples have been taken. The address saved for unloading purposes shall be the

address of the oldest recorded data for input channel 0. To accommodate situations when the entire memory has not been overwritten because of early receipt of event trigger, a second register will be provided. The data stored in the second register shall indicate the number of valid data samples loaded in memory. This register shall be set to zero when the Digitizer is armed and is incremented when a new sample is taken for channel 0. The register (counter) shall be designed to inhibit "roll over" in normal cases when the entire memory has been overwritten. After receipt of the first event trigger the Digitizer shall ignore subsequent triggers until it is rearmed via the dataway.

When the internal clock is selected the clock circuit must not be affected by the event trigger as it is in post-trigger mode. Since the event trigger is asynchronous with the internal clock, a one sample uncertainty may be experienced if the event trigger happens to occur at the same time as an internal clocking edge occurs. Under no circumstances should the clock period be altered by the event trigger. For applications requiring exact timing relationships between the first post-trigger sample and the event trigger an external clock will be supplied and the event trigger will be forced to occur between clock pulses.

4.2.2 Memory Unloading

Memory unloading shall be accomplished by first placing the Digitizer into the unload mode and subsequently issuing read memory data commands. The command causing the Digitizer to commence unload mode shall provide data indicating the channel number desired as well as the relative sample number. The Digitizer circuitry shall find the first word requested by performing the following arithmetic function:

ADDR = (OLDEST ADDR) + (CHA) (SAMPLE NO.) + CHN

where

ADDR = First data word requested

OLDEST ADDR = Address of oldest data for CH0

CHA = Channels active (4, 8, 16, or 32)

CHN = Channel requested (0 to 31)

SAMPLE NO = Quantity loaded by CAMAC Command #7

(See paragraph 6.13.7)

The Digitizer will fetch the appropriate word requested and queue the data into a Dataway buffer register. The Digitizer shall continue to load the buffer after each "read buffer" cycle incrementing the memory address to provide the next available word for the requested input channel (increment to be equal to the number of active channels 4, 8, 16, or 32). The Digitizer will utilize the response line "Q" to indicate whether a valid data request is being made (i.e., requested channel not digitized).

4.2.3 Self Test

The Digitizer shall be capable of switching its thirty-two (32) input ports to an internal function generator. The self test signal generated shall be a periodic monotonically increasing triangular signal varying from 0V (-0 +50 millivolts) to +10V (+0 -50 millivolts) at a frequency of 200Hz. In response to the self test CAMAC command, the module shall switch the input ports to the internal waveform for an approximate period of two (2) seconds and shall internally generate a trigger pulse approximately one (1) second after receipt of the command. The module will respond to the internally generated trigger in the same fashion as it would respond to an external trigger. The number of pre-trigger and post-trigger data recorded will be a function of the module set up before the issuance of the self test command. The module must be "armed" for the self test feature to function properly.

4.2.4 Digitizer Clocking

The Digitizer may be set up through use of a CAMAC command to use either an internally generated clock signal or an external clock signal. The clock rates for the internal clock shall be selectable through CAMAC command. Available internal sampling rates shall be 40KHz, 20KHz, 10KHz, 5KHz, 2KHz, 1KHz, .5KHz, .2KHz, and .1KHz.

4.2.5 Digitizer Triggering

The Digitizer may be triggered from the front panel connector and/or by CAMAC command. The module will respond to the two (2) trigger sources in the same way. Trigger sources will effectively by "OR-ed" together within the Digitizer circuitry.

5.0 Mechanical Characteristics

5.1 The module shall conform to mechanical specifications as indicated in reference 2.].

5.2 The module shall be a three (3) wide CAMAC module.

5.3 The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA Type FR-4 or equivalent. The circuit boards shall be either a "two sided" printed circuit board with etched conductors or a two sided board using "Multiwire" technology. The fabrication of the circuit board shall be in compliance to reference specification 2.3.

5.4 This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate. See reference specification 2.1 and 2.2.

5.5 All components are to be identified with a standard manufacturer's part number or standard method of marking (e.g., resistor color coding) and shall preferably have an exact replacement available from a second source manufacturer. Components available from only a single vendor (source) shall be clearly identified as such and the source for any such components shall be identified.

5.6 All electrical components are to be mounted on only one side of the board.

5.7 The condition of this module is to be monitored by LED's located on the module front panel. (See Figure 11.1 for the suggested front panel layout). All lettering on the front panel shall be either engraved or silkscreened. The front panel material shall be aluminum with an iridite finish with contrasting colored lettering.

5.8 All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part number on the electronic schematic associated with this module. See reference specification 2.4.

5.9 The front panel connectors (LEMO or Kings Loc) shall be provided for interface with the analog inputs, event trigger and external clock. The rear edge type auxiliary connector shall be used for connection to external memory modules. Pin assignment for connectors shall conform to Figure 11.2.

5.10 The printed circuit design layout shall provide pads for the possible addition of filtering and impedance matching components. Provision shall be made for future incorporation of a single pole filter onto each of the thirty-two (32) inputs as well as a matching resistor on each of the thirty-two (32) inputs.

5.11 The mechanical construction of the module shall be designed to facilitate calibration and maintenance. All switches and pots must be accessible without module disassembly. All board to board electrical connections shall utilize connectors. Under no circumstances will "hard soldered" wire connections occur between boards. Cables to the front panel may be soldered to printed circuit boards providing enough stock is allowed for disassembly (if required) for calibration, test and maintenance purposes. Like circuit boards shall be mechanically and electrically interchangeable from Digitizer to Digitizer.

6.0 Electrical Characteristics

6.1 Dataway Interface shall conform to specification as indicated in reference 2.1.

6.2 Input Power shall be derived from the standard $\pm$6 volt and $\pm$24 volt CAMAC supply voltages. Whenever possible, low power circuitry (such as the 74LS series) shall be used.

6.3 The +6 and -6 supply voltages must be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages must be bypassed with electrolytic capacitors of at least 6.8 microfarads. In addition, at least half the integrated circuits must contain a ceramic bypass capacitor of at least .01 microfards on their supply voltage lines. The .01 microfarad capacitors shall be distributed on the circuit board and be located as close as possible to noise sensitive components.

6.4 All components on this module must have a MTBF rating as specified in reference 2.6.

6.5 Analog Input Characteristics

6.5.1 All inputs shall be differential with input impedance of 10,000 ohms $\pm$1% from DC to 20KHz.

6.5.2 The input range shall be selectable for all channels simultaneously through use of printed circuit mounted DIP switches. Selectable ranges shall be for full scale differential voltages:

0 to +10.2375

0 to 5.11875

-5 to -5.1200 to +5.11875

-2.5 to +2.5 volts -2.56 to +2.559375

6.5.3 Common Mode Rejection Ratio

DC - 1KHz 60db minimum

1KH - 20KHz 40db minimum

6.5.4 Bandwidth

The selected module gain shall be flat to ±0.1db from DC to 20KHz. Filter requirements for specific applications shall be installed external to the module.

6.5.5 The module shall operate as specified under conditions of common mode voltage offset, providing that the voltage on any input does not exceed ±15 volts referenced to chassis ground.

6.5.6 The module shall be capable of withstanding input voltage of up to plus or minus one hundred (100) volts to ground on any input without sustaining damage except to the protective input resistors or adjacent area of printed circuit board due to heat generated by the protective resistors.

6.5.7 The module will recover to specified accuracy within 100μsec following a maximum specified over voltage (100 volts) which lasts for a duration of one hundred (100) milliseconds or for a duration and duty cycle which does not degrade the protective resistors.

6.5.8 The interchannel cross talk between any pair of channels shall be 60db or greater including the condition when the input is ±100 volts.

6.6 Module Conversion Characteristics

6.6.1 Resolution - 12 bits

6.6.2 Absolute accuracy for all channels from 20°C to 50°C: ±.03% of FS ± 1/2 LSB maximum.

6.6.3 Monotonicity - No missing codes from 20°C to 50°C.

6.6.4 Nonlinearity - ± 1/2 LSB maximum from 20°C to 50°C.

6.6.5 Temperature coefficient of gain - ± 40 PPM/°C maximum.

6.6.6 Maximum Conversion Time

5 microsecond/channel + 5 microsecond overhead

165 microsecond/32 channel

6.6.7 Throughput

Digitizing - 160 x 10^3 samples/second minimum

(4 active channels)

192 x 10^3 samples/second minimum

(32 active channels)

Unloading - 500 x 10^3 words/second minimum

6.6.8 Output Coding

The data output coding for transfer onto the Dataway read lines shall be implemented in two's complement format, with the sign extended to sixteen (16) bits. The module shall provide DIP switches or movable jumpers to accomplish the sign extension for either unipolar or bipolar utilization of the ADC. Bit weighting for data returned shall always be .00125 volt/bit. When the module is set to operate with a full scale swing of ten (10) volts the least significant bit (LSB) shall always be set to zero.

UNIPOLAR (0V to +10.24V, 12 bit ADC)

SCALE	VOLTAGE	BINARY CODE
+FS	+10.2375V	0001 1111 1111 1110
+ 1/2 FS	+ 5.1200V	0001 0000 0000 0000
0	0.0000V	0000 0000 0000 0000

BIPOLAR (-5.1200V to +5.1175V, 12 bit ADC)

SCALE	VOLTAGE	BINARY CODE
+FS	+ 5.1175V	0000 1111 1111 1110
0	0.0000V	0000 0000 0000 0000
-FS	- 5.1200V	1111 0000 0000 0000

6.7.9 Track and Hold

Each input shall have a dedicated Track and Hold circuit to insure simultaneity of sampled data. The characteristics of the Track and Hold circuit shall be consistent with the maximum sampling rate (40KHz) and a maximum analog input frequency of 20KHz. The acquisition time, droop rate and accuracy shall be consistent with the overall speed and accuracy of the digitizer system. It should be noted that the last channel digitized (CH3, CH7, CH15 or CH31) will be the determining factor in the Track and Hold design since these channels will have the shortest acquisition time and the longest hold time.

The channel-to-channel uncertainty shall be a maximum of 10ns. Individual channel aperture jitter shall be a maximum of 5ns.

6.8 Memory Interface

The module shall interface to external memory modules through use of the thirty-six (36) pin rear auxiliary connector. Signals on the memory conductor shall be implemented through use of tri-state TTL level devices. The output signals shall utilize "Buss Drivers" to allow the use of as many as thirty-two (32) auxiliary memory modules (reference 2.9). Memory modules may be located up to five feet (5 ft) from the Digitizer. The data convention shall be high-true with timing compatible with companion memory modules (reference 2.9).

6.9 Clock Driver Interface

The module shall interface to an external clock signal through use of the two (2) pin front panel connector. The clock input circuit shall utilize an optoisolator such as HCPL 2601 or equivalent with pads for series and terminating 1/4 watt resistors. Termination for the clock shall be external to the module.

6.10 Event Trigger Interface

The module shall receive event trigger pulses through use of the front panel LEMO connector. The event trigger input shall utilize an optoisolator such as the HCPL 2601 or equivalent with pads for series and terminating 1/4 watt resistors. Cable terminators for the event trigger port shall be external to the module. When operating in post-trigger mode the module shall use the trigger input to start the digitizing/memory loading sequence that continues until the available memory is full. When operating in pre-trigger mode the module shall use the trigger input to signal its internal circuitry that the next data word loaded for channel 0 is the first post-trigger sample. The module circuitry shall operate as specified providing teh trigger pulse either leads or lags clock pulse (internal or external) by a minimum of one half (0.5 S) microsecond. Trigger pulses occurring within the one microsecond (1 S) window may result in a one sample uncertainty between modules running in parallel.

6.11 Analog Input Interface

The module shall interface up to thirty-two (32) analog input voltages through use of front panel "LEMO" type connectors. Three (3) pin connectors (RGOB303CA222) shall be utilized as follows:

Pin	Type	Use
1	female	chassis ground
2	female	signal high
3	female	signal low

As viewed from the front panel, pin 1 is in line with the alignment key and proceeding clockwise.

6.12 Operating Sequence

A typical operating sequence would start with the module being armed in one of its digitizing modes. Upon receipt of the "arm" command the internal "End of Record" flag will be cleared and the memory address registers of the module will be set to start taking data. Upon receipt of an event trigger pulse (post trigger operation only) the module shall commence loading the remote memory in the appropriate manner. At the conclusion of the digitizing period, the module will set its "End of Record" flag and ignore subsequent event and clock pulses. Throughout the sequence, the module shall update its internal status register for possible transfer onto the Dataway. Through all operating modes, the module status register shall be readable via CAMAC command.

Unloading of the remote memory shall be accomplished through the module memory control circuitry. Upon receipt of an "unload" command, the module shall fetch the appropriate data word from the remote memory and load the word into the dataway buffer register. The dataway buffer register will subsequently be unloaded by CAMAC command. After the dataway buffer is unloaded the module will increment the address register and reload the buffer with the next data word within two microseconds (2us) of the dataway cycle. The module remains in the unload mode until a new "mode select" command is received. When digitizing in pre-trigger mode the module will determine the starting memory location and will increment around the memory to return the data in the same order that it was stored. The memory increment shall be consistent with the number of active channels. The memory size data required for "wrapping around" memory during loading and unloading shall be determined by the position of board mounted DIP switches.

6.13 CAMAC Commands

The module shall accept commands from the CAMAC dataway in compliance with reference 2.1. The module response to various CAMAC commands will be a function of the module operating status; four (4) states of operation are defined below. The module will always be operating in one of the following states. The module status register will provide a means of determining the module status.

State 0 - an inactive state that will exist after "power up" or after receipt of appropriate command. The module, when in "State 0" will not respond to input clock signals or to input event triggers.

State 1 - a commanded state that will exist after the module has been placed in a "load" mode of operation but has not yet received an event trigger to commence digitizing.

State 2 - a triggered state that will exist after an event trigger has occurred and the module is in the process of digitizing data and loading the remote memory.

State 3 - a state that will exist after the digitizer has been initially triggered and has completed memory loading and has set its internal "End of Record" flag.

6.13.1 Command #1 Read Status [F(0).A(0)]

This command gates the contents of the module status register onto the Dataway. The contents of the status register shall be interpreted as follows:

Bits R1-R3 Operating Mode

0 = Mode 0 (Clear)

1 = Post Trigger Mode

2 = Pre Trigger Mode

3 = Unload Mode

Bits R4-R5 Operating State

0 = State 0, Clear

1 = State 1, Armed

2 = State 2, Armed and Digitizing

3 = State 3, Digitizing Sequence Complete

Bits R6-R10 Available Memory

0 = 32K

1 = 64K

⋮

30 = 992K

31 = 1 Meg

Bits R11-R12 Module Gain (Scale) Setting

0 = 0 to +10 volts

1 = 0 to +5 volts

2 = -5 to +5 volts

3 = -2.5 to +2.5 volts

Bits R13-R14 Number of Active Channels

0 = 32 channels

1 = 16 channels

2 = 8 channels

3 = 4 channels

Bits R15-R18 Clock Selected

0 = External Clock

1 = 40KHz (internal)

2 = 20KHz (internal)

3 = 10KHz (internal)

4 = 5KHz (internal)

5 = 2KHz (internal)

6 = 1KHz (internal)

7 = .5KHz (internal)

8 = .2KHz (internal)

9 = .1KHz (internal)

The module will respond to Command #1 in all modes and states of operation.

6.13.2 Command #2 Read Post-Trigger Sample Count [F(0).A(1)]

This command gates the contents of register R1 onto the CAMAC read lines R1 through R20. The quantity returned (pre-set by command F(16).A(0) represents the number of post-trigger sample blocks (16 word block) programmed to be taken.

6.13.3 Command #3 Read Register R2 [F(0).A(2)]

This command gates the contents of register R2 onto the dataway read lines R1 through R19. The quantity returned will indicate the number of valid data samples taken for channel 0. This command will be used to determine if the module was stopped before filling available memory (see paragraph 4.2.1.2). In addition, bit R20 shall be set whenever all available memory contains new data.

6.13.4 Command #4 Read Memory Buffer [F(2).A(X)]

This command gates the contents of the memory buffer register onto the Dataway. After completing the Dataway cycle the module will increment its internal memory address register by a sufficient quantity to obtain the next desired word for the channel unloading. The absolute increment shall be determined by the module circuitry dependent upon the subaddress A(X) and the number of channels active. The intent of this command is to read every Xth word for a given channel from 1 to 16 corresponding to X=0 to 15, and then reload the memory buffer with the new data word. The data transfer to the Dataway read lines shall be right justified (LSB on R1) with the sign extended to sixteen (16) bits. The module will respond to this command only after the module has successfully been put into the data unload mode by CAMAC Command #7. Attempts to read the memory buffer prior to setting up the unload mode will result in a CAMAC response of Q=0 and a CAMAC data return of all zeros.

6.13.5 Command #5 Read Module Number [F(6).A(0)]

This command gates the module identification number (decimal 908, hexadecimal 38C) onto the Dataway read lines R1 through R12. The module will respond to Command #5 in all modes and states of operation.

6.13.6 Command #6 Arm Module [F(16).A(0).D($YYYYYY_H$)]

This command sets up the digitizing mode of operation and is required to be issued prior to any digitizing sequence. The command clears the End of Record (EOR) flag if set and sets the module memory address pointer to location zero. This command makes use of the CAMAC data field W1 through W24 as follows:

Bit W1 Set Operating Mode

0 = Post-Trigger Mode

1 = Pre-Trigger Mode

Bits W2-W5 Set Digitizing Clock

0 = External Clock

1 = 40KHz Internal Clock

2 = 20KHz Internal Clock

3 = 10KHz Internal Clock

4 = 5KHz Internal Clock

5 = 2KHz Internal Clock

6 = 1KHz Internal Clock

7 = .5KHz Internal Clock

8 = .2KHz Internal Clock

9 = .1KHz Internal Clock

A-F = Unassigned

Bits W6-W7 Set Active Channels

0 = 32 channels active

1 = 16 channels active

2 = 8 channels active

3 = 4 channels active

W8 Unused

Bits W9-W24 Set Post-Trigger Sample Count

The quantity represented by this sixteen (16) bit sub-field indicates the number of blocks of post-trigger data required. Each block shall be sixteen (16) samples deep. The range of post-trigger data for each active channel shall be from 0 to 1,048,575 samples.

6.13.7 Command #7 Enable Unload [F(16).A(1).D($YYYYYY_H$)

This command sets up the memory unloading sequence and is required prior to reading of memory data onto the dataway. The command utilizes the CAMAC data field W1 through W24 as follows:

Bits W1-W18 Relative Address of Requested Channel Data

The quantity represented by this field shall indicate the relative address of the first data word to be transferred onto the Dataway. The quantity indicated is added to the address of the oldest available data for a given channel.

Bits 19-23 Channel Number

The quantity from 0 to 31 represented by this field indicates the input channel data desired. The module will return Q=0 for this command if the requested channel was not digitized since the last arm command.

6.13.8 Command #8 Set "End of Record" Flag [F(25).A(0)]

This command forces the EOR flag to the "set" status. The potential use of this command would be for forcing the module to stop loading memory in the event of a failed clock input signal.

6.13.9 Command #9 Start Self Test [F(25).A(1)]

This command starts a self test sequence as delinated in paragraph 4.2.3. The module will return Q=0 for this command if the module is not armed when the command is received.

6.13.10 Command #10 Trigger Module [F(25).A(2)]

This command triggers the module within its commanded mode. The module will respond to this command in the same fashion as it responds to an external trigger.

6.13.11 Dataway Responses Q and X

The module will return X=1 for all addressed commands if it recognizes the command as one it is equipped to perform. The module will return Q=1 conditionally if the module is ready to participate in the commanded function.

6.13.12 Initialize and Clear Z+C

The module will respond to Z or to C by clearing all its associated memory locations and set the module to mode 0. The module ignores all dataway operations for up to 2 seconds after receipt of either initialize or clear, to allow time to cycle through all its memory functions.

6.14 Power on Reset

The module shall provide a "power on reset" circuit to effectively perform the same function as CAMAC command Z+C. The "power on reset" condition may exist for up to 2 seconds after power on.

6.15 Front Panel LED's

The module shall provide five (5) LED indicators mounted for visibility from the front panel. The indicators shall function as follows:

LED #1 ("N") shall illuminate for a minimum time of 100 milliseconds whenever N is received.

LED #2 ("ARMED") shall illuminate whenever the module is armed and awaiting event trigger. The minimum time for illumination shall be 100 milliseconds.*

LED #3 ("ACT") shall illuminate whenever the module is digitizing and loading memory

LED #4 ("EOR") shall illuminate whenever the internal "End of Record" flag is set.

LED #5 ("TRIG") shall illuminate for a minimum time of 100 milliseconds whenever an event trigger is received.

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* Note that in pre-trigger mode LED #2 and LED #3 shall both illuminate until the event trigger is received. In post-trigger mode LED #2 is turned off at the same time that LED #3 is turned on.

7.0 Environmental Data

7.1 The module must operate, as defined, over an ambient temperature range of 0 to $+50^{o}C$.

7.2 The module must operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must operate, as defined, in the presence of an external magnetic field changing at a maximum rate of 100 gauss per second with a peak magnitude of 200 gauss in any direction.

7.4 The module must operate, as defined, in a radiation environment as follows:

Neutrons	2×10^{7} n/CM^{2}/sec
Rad-dose	5×10^{-2} rad (Si)/sec
Integrated Dose	200 rad (Si)

8.0 Safety

All components of this module must be of flame retardant material.

9.0 Testing and Calibration

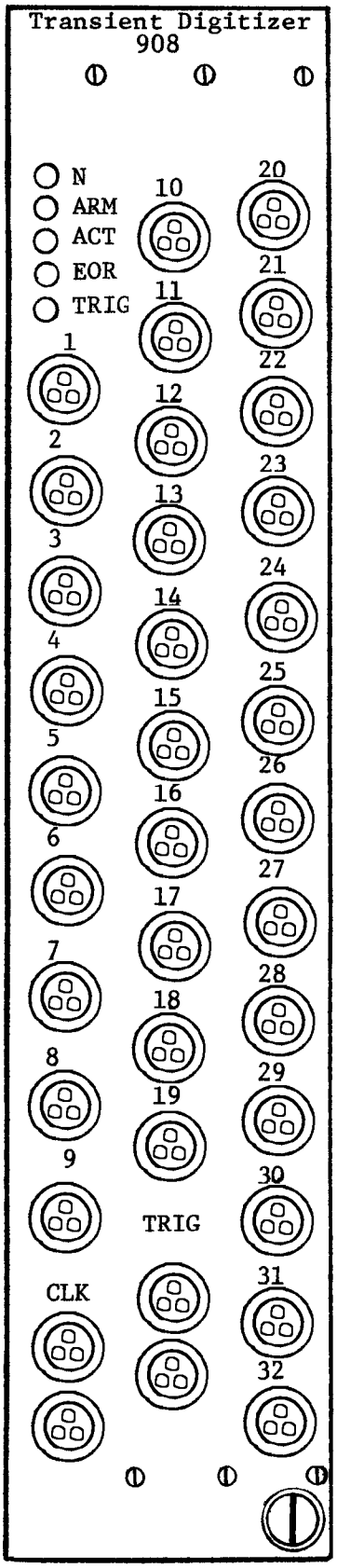
All modules shall be subjected to a temperature cycling period followed by a functional test prior to release for use. A description of the tests to be performed shall be submitted by the vendor for incorporation into this specification. Acceptance tests must be conducted in standard CAMAC crates with the Digitizer module under test connected to one megaword of Remote Memory (see reference 2.9). All operating modes must be tested with dynamic input signals with sufficient rates of change to verify the system accuracy and bandwidth. Data analysis must be computer based so that some

reasonable number of different configurations (active, channels, clock rates, etc.) may be exercised.

A calibration procedure shall be submitted by the vendor for incorporation into this specification. The procedure shall be based upon the use of standard calibration instruments and standard CAMAC crates and modules. Equipment needed to perform the calibration shall be clearly stated as well as equipment set-up and interconnectors. Calibration shall be accomplished by potentiometer adjustments and shall not require component matching or replacement unless a component failure has occurred. The procedure shall include a copy of a report format to be filled out by the person performing the calibration that shall include space for entries of final readings as well as space for the signature of the person performing the procedure.

10.0 Reliability and Quality Control

The module shall meet all applicable requirements specified in reference 2.6.



(5) Status LED's

(32) 3-Pin LEMO or equal for analog input

(4) 3-Pin LEMO or equal for external clock and external trigger

Front Panel Layout

Figure 11.1

Auxiliary Connector

(viewed from front of crate)

Pin	Function	Pin	Function
1B	MAB 19	1A	MAB 1
2B	MAB 18	2A	MAB 0
3B	MAB 17	3A	GND
4B	MAB 16	4A	DB 11
5B	MAB 15	5A	DB 10
6B	MAB 14	6A	DB 9
7B	MAB 13	7A	DB 8
8B	MAB 12	8A	DB 7
9B	MAB 11	9A	DB 6
10B	MAB 10	10A	DB 5
11B	MAB 9	11A	DB 4
12B	MAB 8	12A	DB 3
13B	MAB 7	13A	DB 2
14B	MAB 6	14A	DB 1
15B	MAB 5	15A	DB 0
16B	MAB 4	16A	GND
17B	MAB 3	17A	Write Strobe
18B	MAB 2	18A	Read Strobe

PIN ASSIGNMENTS

FIGURE 11.2

908 and 3232 Command Chart

Command Name	Sample Rate	Chans	F(16) A(0) Hex	F(16) A(0) Dec	Note
ARM	40Khz	4	62	98	908 & 3232
ARM	20Khz	4	64	100	908 & 3232
ARM	10Khz	4	66	102	908 & 3232
ARM	5Khz	4	68	104	908 & 3232
ARM	2Khz	4	6A	106	908 & 3232
ARM	1Khz	4	6C	108	908 & 3232
ARM	500Hz	4	6E	110	908 & 3232
ARM	200Hz	4	70	112	908 & 3232
ARM	100Hz	4	72	114	908 & 3232
ARM	40Khz	8	42	66	3232 Only
ARM	20Khz	8	44	68	908 & 3232
ARM	10Khz	8	46	70	908 & 3232
ARM	5Khz	8	48	72	908 & 3232
ARM	2Khz	8	4A	74	908 & 3232
ARM	1Khz	8	4C	76	908 & 3232
ARM	500Hz	8	4E	78	908 & 3232
ARM	200Hz	8	50	80	908 & 3232
ARM	100Hz	8	52	82	908 & 3232
ARM	20Khz	16	24	36	3232 Only
ARM	10Khz	16	26	38	908 & 3232
ARM	5Khz	16	28	40	908 & 3232
ARM	2Khz	16	2A	42	908 & 3232
ARM	1Khz	16	2C	44	908 & 3232
ARM	500Hz	16	2E	46	908 & 3232
ARM	200Hz	16	30	48	908 & 3232
ARM	100Hz	16	32	50	908 & 3232
ARM	10Khz	32	06	6	3232 Only
ARM	5Khz	32	08	8	908 & 3232
ARM	2Khz	32	0A	10	908 & 3232
ARM	1Khz	32	0C	12	908 & 3232
ARM	500Hz	32	0E	14	908 & 3232
ARM	200Hz	32	10	16	908 & 3232
ARM	100Hz	32	12	18	908 & 3232

908 and 3232 Command Chart (cont)

Trigger		F(25) (2)	F(25) (2)	
Enable Unload	**Chan**	**F(16) A(1) Hex**	**F(16) A(1) Decimal**	
Enable Unload	1	000000	0	
Enable Unload	2	040000	262,144	
Enable Unload	3	080000	524,288	
Enable Unload	4	0C0000	786,432	
Enable Unload	5	100000	1,048,576	
Enable Unload	6	140000	1,310,720	
Enable Unload	7	180000	1,572,864	
Enable Unload	8	1C0000	1,835,008	
Enable Unload	9	200000	2,097,152	
Enable Unload	10	240000	2,359,296	
Enable Unload	11	280000	2,621,440	
Enable Unload	12	2C0000	2,883,584	
Enable Unload	13	300000	3,145,728	
Enable Unload	14	340000	3,407,872	
Enable Unload	15	380000	3,670,016	
Enable Unload	16	3C0000	3,932,160	
Enable Unload	17	400000	4,194,304	
Enable Unload	18	440000	4,456,448	
Enable Unload	19	480000	4,718,592	
Enable Unload	20	4C0000	4,980,736	
Enable Unload	21	500000	5,242,880	
Enable Unload	22	540000	5,505,024	
Enable Unload	23	580000	5,767,168	
Enable Unload	24	5C0000	6,029,312	
Enable Unload	25	600000	6,291,456	
Enable Unload	26	640000	6,553,600	
Enable Unload	27	680000	6,815,744	
Enable Unload	28	6C0000	7,077,888	
Enable Unload	29	700000	7,340,032	
Enable Unload	30	740000	7,602,176	
Enable Unload	31	780000	7,864,320	
Enable Unload	32	7C0000	8,126,464	
Unload		**F(2) A(Increment)**	**F(2) A(Increment)**	1 Smpl at a time

P2 GLITCH PROBLEM

John Wertenbaker 3/17/00

It was discovered that the P2 line on the CAMAC dataway can contain glitches that are caused by the capacitive coupling of the 1Mhz P2 line and the function (F) lines. The F(16) line, which is just opposite of P2 has the greatest coupling, but the more F lines that are active, the larger the glitch will be on P2. This glitch can vary from crate to crate, and from slot to slot, but, in one case it was measured at 2 volts.

The glitch can cause any module that uses the P2 line, like the 408, 409, 412, 413, and 908 modules, to count an extra clock pulse, causing timing errors in any system that uses those modules. Below is a list of the modules that derive their clock from the P2 line, and a description of the input circuitry in each module.

408 P2 input goes to a 74LS28, which is a NOR gate.
409 P2 input goes to a 74123 one-shot.
412 P2 input goes to a 74LS38, which is a NAND gate.
413 P2 input goes to a 74LS02.
904 P2 input goes to a 74LS14 Schmitt-trigger inverter.
908 P2 input goes to 3 74LS74's and 2 74LS08's.
910 P2 input goes to a 74LS14 Schmitt-trigger inverter.
912R P2 input goes to a 74LS14 Schmitt-trigger inverter.
914 does not use the P2 line.

The 409 Timed Gate module was the only module that was tested and proven to be susceptible to this glitch. The 408, 412, 413, and 908 modules are assumed to be susceptible, also, based on their input circuitry. The 904, 910, and 912R modules are much more tolerant of this glitch, due to the Schmitt-trigger inputs, and are probably not affected. The 914 module generates its own 1Mhz, and is independent of the P2 line.

This occurrence of this problem is rare due to the nature of clock cycles in NSTX, and its predecessor, TFTR. In those machines, most modules are set up and armed long before any trigger pulse starts the counting of P2 clock pulses. Very few CAMAC commands are performed after these arm and setup commands. In most cases, the only commands that come through during the counting times are read-back commands and L-2 crate controller wakeup commands. These happened every 2 seconds in TFTR, and even less often than that in NSTX. Also, most of the time, the 1Mhz P2 line is divided down to a much lower frequency, so a few microseconds of inaccuracy would not be noticed.

For the rare cases when the glitches can cause problems, such as the Facility Clock Generator crates, the recommended fix is to insert a P2 Capacitor Filter Module in the crate as close as possible to the module that uses the P2 line. This module contains a 1000pf capacitor from the P2 line to ground. This attenuates the high frequency of the glitch, without seriously rounding off the edges of the 1Mhz P2 signal.

It should be noted that the 404A had a similar problem with the P1 line. The BUSY line, which is an un-terminated line in the crate, was coupling a glitch over to the P1 line. The repair for that problem was to install a Schottky diode on the BUSY line to clamp the negative-going overshoot at the low-going transition of the BUSY pulse, and replace the 74LS04 with a Schmitt-trigger 74LS14 at the P1 input. However, it was not considered practical to modify every module that uses the P2 line because the problem is much more rare than the P1 problem, due to the nature of when the glitch occurs.

Princeton University: PPPL Computer Division

To: Distribution Date: July 16, 1987

From: W. Rauch Subject: Overdriven H911 Scaler and H908/3232 Digitizer CAMAC Module Input Optical Device

W Rauch

==========

H911 PROBLEM

The H911 Scaler receives and counts pulses on 32 optical isolated inputs. The receiver chips are Hewlett Packard 2601's. Each contains a light emitting diode, thereby providing optical isolation. The anomaly identified is a tendency for some of these chips to turn back on during turn-off. This turn-on, turn-off, turn-on, turn-off transition exceeds the logic thresholds of the succeeding logic buffer (TTL chip) and results in two pulses when actually only one was received at the input. This is shown in Fig. 1.

H911 RESOLUTION

Further examination (see attachment A) shows that the existing H911 2601 forward light emitting diode current (I_F) could be as great as 35 ma. However, its absolute maximum specified rating is only 20 ma. For the H911 it was shown that the series terminating resistor should be approximately 390 Ω instead of 100 Ω to provide the recommended I_F of 6.3 ma (see attachment B). Figure 2 substantiates the effect of changing this resistor to the appropriate value.

H911 IMPACT

Eighteen scalers are presently in service. Diagnosticians recognized this anomaly as a system problem quite some time ago, and have the

ability through a software switch to compensate for double pulses. Changing the resistor value would be transparent to the system where they are presently used.

H908 AND H3232 DIGITIZER

The External Clock and trigger inputs of the H908 and H3232 digitizer use the same optical isolated input device. The trigger input has been determined to not be of concern, because of the nature of the internal logic of the digitizer. However, the External Clock input was shown that if driven by the 904 and 412 timing and sequencing modules, that the same double pulsing occurs. The present circuit could be driven by as much as 68 ma I_F, which exceeds the 20 ma absolute maximum rating (see Attachment A). Replacing the 51 Ω terminating resistor with a nominal value of 390 Ω was verified to correct the problem (see Attachment C) at a nominal I_F of 10 ma.

Because only a few applications use the configuration that requires the External Clock input, I would suggest that a series external terminating resistor be inserted at the digitizer end of the External Clock signal cable (possible in a Pamona box).

WR:vz
Attachments
Distribution
N. Arnold
W. Bergin
H. Feng
S. Hosein
G. Kolinchak
J. Montague
P. Sichta
J. Wertenbaker

cc: G. Oliaro
N. Sauthoff
K. Young

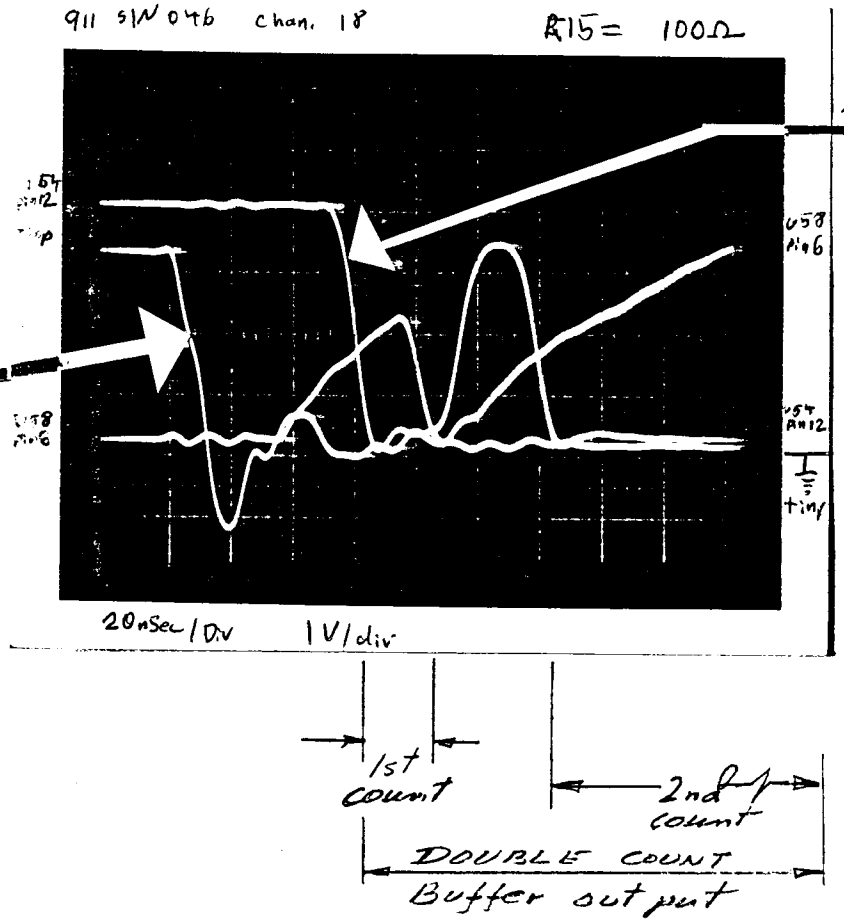


Figure 1

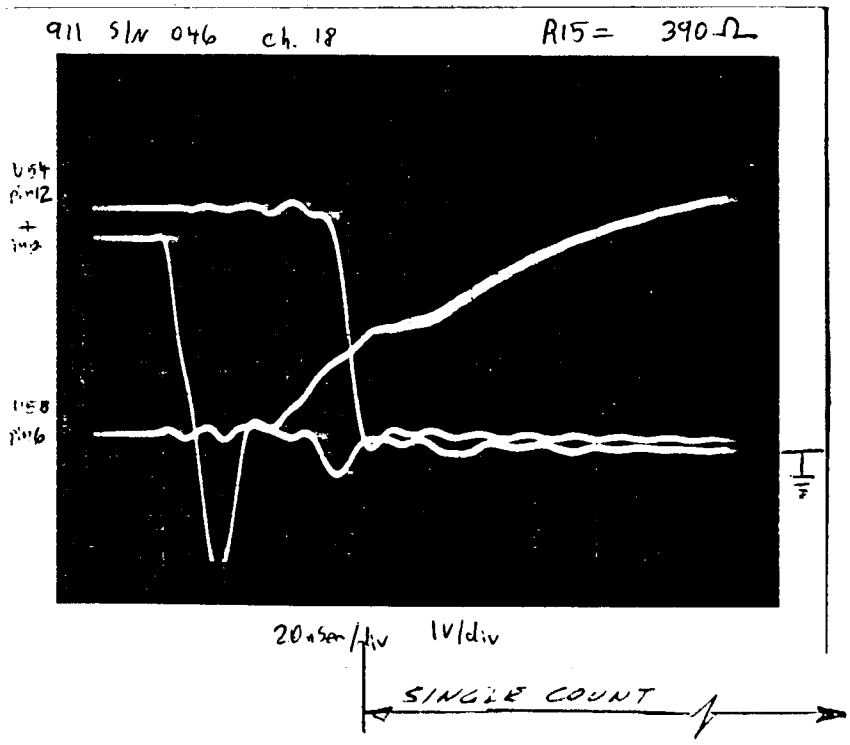


Figure 2

2601 opto Isolator Specs

Input Forward Voltage $V_{F_{TYP}} = 1.5V$, $V_{max} = 1.75V$ } $I_F = 10ma$

Recommended $I_F = 6.3ma$ at $V_{cc} = 5 \pm .5V$

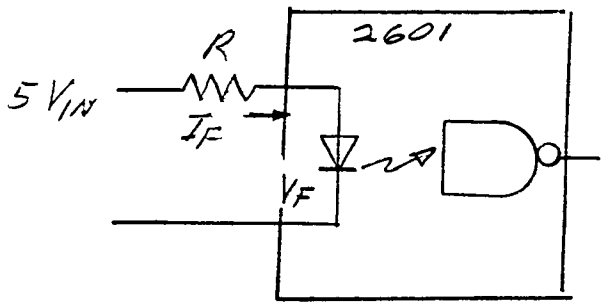
Absolute Max $I_F = 20ma$

Input diode Temperature coefficient

$$\frac{\Delta V_F}{\Delta T_A} = -1.6 \text{ mV}/^{\circ}C \text{ at } I_F = 10ma$$

H911, $R = 100\Omega$

$$I_F = \frac{V_{IN} - V_F}{100} = \frac{5 - 1.5}{100} = 35ma$$



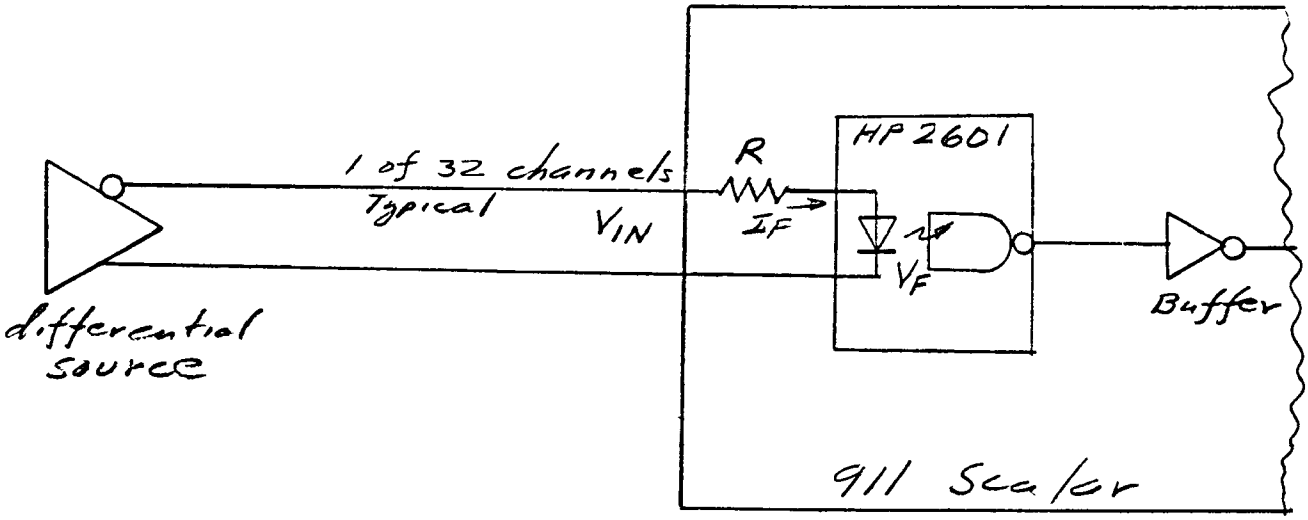
H908 and 3232 EXT CLK, $R = 51\Omega$

$$I_F = \frac{V_{IN} - V_F}{51} = \frac{5 - 1.5}{51} = 68ma$$

ATTACHMENT A

H911 Multi-channel latching scalar

$V_{IN_{MIN}} = 3V$
$V_{IN_{MAX}} = 5V$ differential (per 911 spec)



$I_F = 6.3ma$ recommended by mfg.

$$R_{MIN} = \frac{V_{IN_{MIN}} - V_{F_{MAX}}}{I_F} = \frac{3 - 1.75}{6.3\,ma} = \frac{1.25}{6.3ma} = 198\,\Omega$$

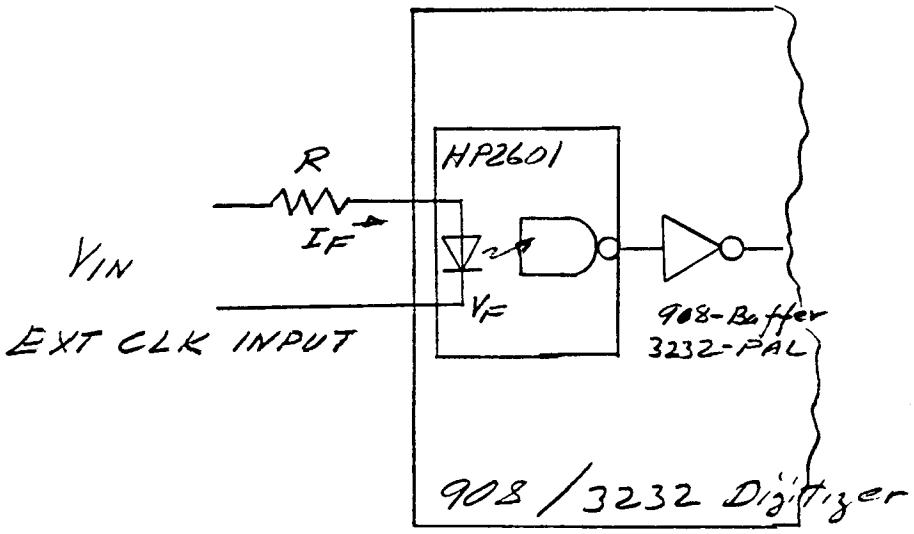
$$R_{max} = \frac{V_{IN_{MAX}} - V_{TYP}}{I_F} = \frac{5 - 1.5}{6.3ma} = \frac{3.5}{6.3ma} = 555\,\Omega$$

$$R_{NOM} = \frac{V_{NOM} - V_{TYP}}{I_{F_{NOM}}} = \frac{4 - 1.5}{6.3\,ma} = 396\,\Omega$$

ATTACHMENT B

H908 & 3232 Transient Digitizer

EXT CLK $V_{IN} = 5V \pm 20\%$ (per TFTR-10A2-H57)
$= 5V \pm 1V$



use $I_F = 10$ ma

$$R_{MIN} = \frac{V_{IN_{MIN}} - V_{F_{MAX}}}{I_F} = \frac{4 - 1.75}{10\text{ ma}} = 225\ \Omega$$

$$R_{MAX} = \frac{V_{IN_{MAX}} - V_{TYP}}{I_F} = \frac{6 - 1.5}{10\text{ ma}} = 450\ \Omega$$

$$R_{NOM} = \frac{V_{IN_{NOM}} - V_{TYP}}{I_{F_{NOM}}} = \frac{5 - 1.5}{10\text{ ma}} = 350\Omega \quad \text{use } 390\Omega$$

ATTACHMENT C

908 Transient Digitizer Invalid Setups

John Wertenbaker
4/20/2004

An anomaly was recently found in the 908 transient digitizer. It is stated in the 908 specification in Section 4.1 that the maximum number of channels for the 40Khz sampling rate is 4. However, there is nothing to prevent someone from programming it to digitize at 40Khz with 32 channels. There are other invalid setups, too. Below is a chart describing what happens with these invalid setups:

# of Ch.	Programmed Sample Rate	Actual Sample Rate
8	40Khz	20Khz
16	20Khz	10Khz
16	40Khz	13.3Khz
32	10Khz	5Khz
32	20Khz	6.67Khz
32	40Khz	8Khz

It should be noted that, although these sampling rates were tested on 2 908's, there is no guarantee that all 908's will function properly at these sampling rates. Also, the software will graph the wrong time scale if any of these setups are used.

908 Transient Digitizer Self-Test Modification

John Wertenbaker

9/16/2010

It was discovered that some 908 Transient Digitizers were going into self-test mode while digitizing. This happens when there is a plasma disruption and during CHI operations. It turns out that the 908 allows the F(25) A(1) Self-Test command to be executed even after a trigger is received. Although the crate controller isn't invoking this command during the plasma shot, there is enough of a glitch on the dataway lines to fool the 908 into thinking it is receiving an F(25) A(1) command during the disruption.

There was a simple modification that was thought to fix the problem. This modification prevented the 908 from going into self-test mode while it was actively digitizing. However, one of the digitizers with this modification was still going into self-test mode.

It was then decided to design a modification that completely disables the self-test mode. This is a simple 2-jumper modification. One jumper connects U17 pin 3 to U17 pin 6. The second jumper connects U17 pin 11 to U17 pin 14. No traces need to be cut, and this jumper can be on the component side of the board. This modification grounds both “CLR” inputs of the self-test one-shot, which completely disables the self-test function.

After a 908 module is modified, a sticker that says "Self Test Disabled" needs to be attached

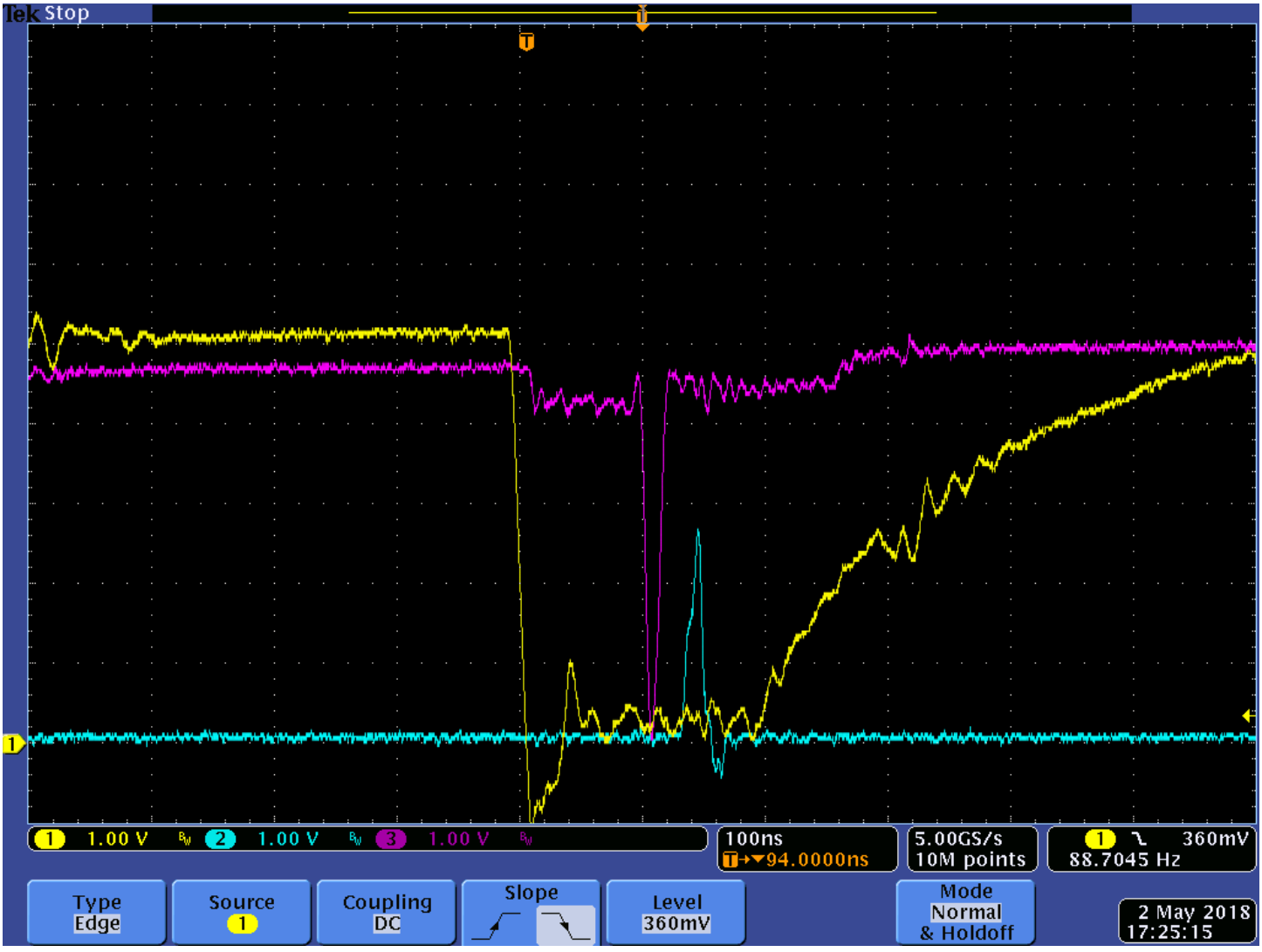
908 Transient Digitizer U16 Pin 19 Modification

John Wertenbaker

05/09/2018

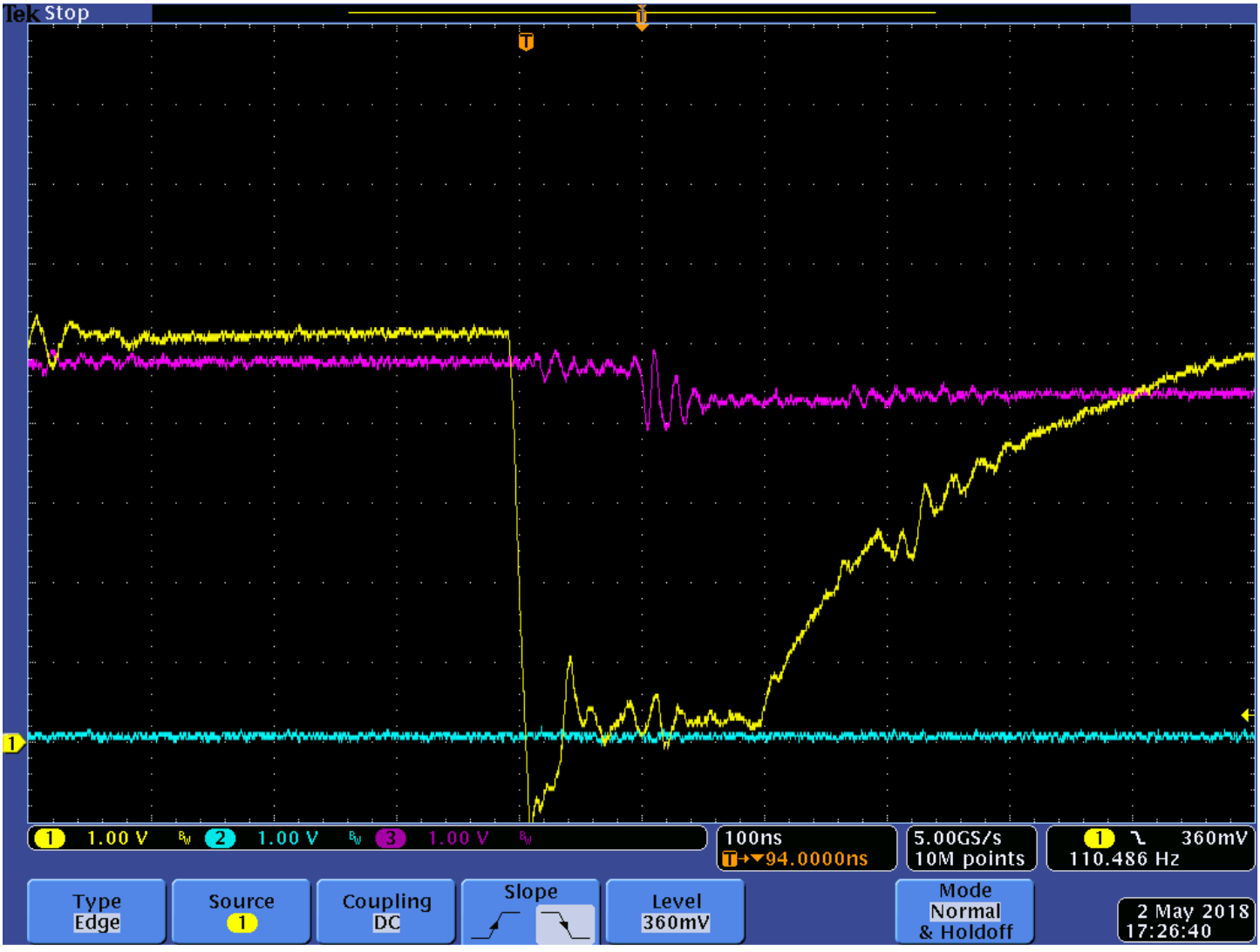
It was discovered that, after the U16 PROM was replaced on the left board, the 908 would occasionally fail to trigger. The new 74S472AN PROM is much faster than the old 82S147N. On some 908 modules, a glitch will be present on the "A>B" line during the ARM command, generated by the center board. The old PROM never propagated this glitch, but the new ones do. The glitch is generated during an F(16) A(0) ARM command when the number of active channels is being changed. On the center board, U3 and U10 act as a 2-4 decoder/demultiplexer. When the input data is changed, the propagation delay of U10 causes a race condition to the "A" inputs of U4. This causes U4 to output the glitch. The glitch is then sent to the PROM, U16, left board. This glitch goes through U16 pin 19 to U16 pin 12. From there, it is sent to U17 pin 2 on the center board.

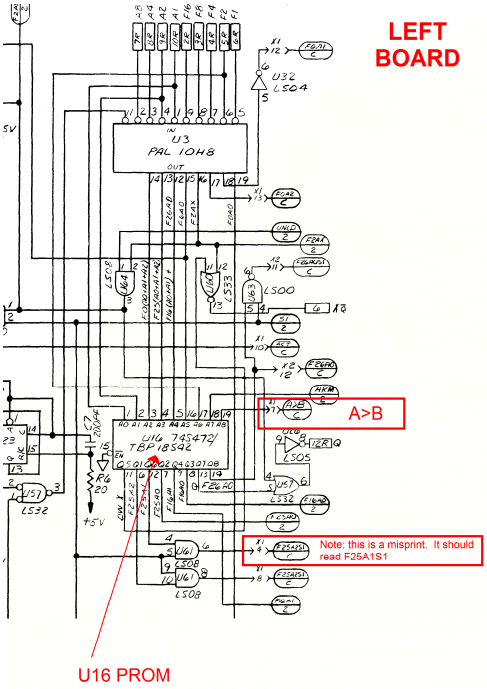
The glitch triggers U17 pin 2 on the center board, which triggers some, but not all of the Self Test trigger logic. The Self Test cycle inhibits a real trigger for at least 1 second, and it makes the module fail the functional test. At this time, it is not known if this behavior causes any other problems. The “A>B” signal (U16, pin 19, left board) is shown below in magenta, the CAMAC S1 line is yellow, and the F25 A1 S1 line (U61 pin 6) is blue. This glitch can easily be generated by running test #1 in NEWERCAL.EXE.

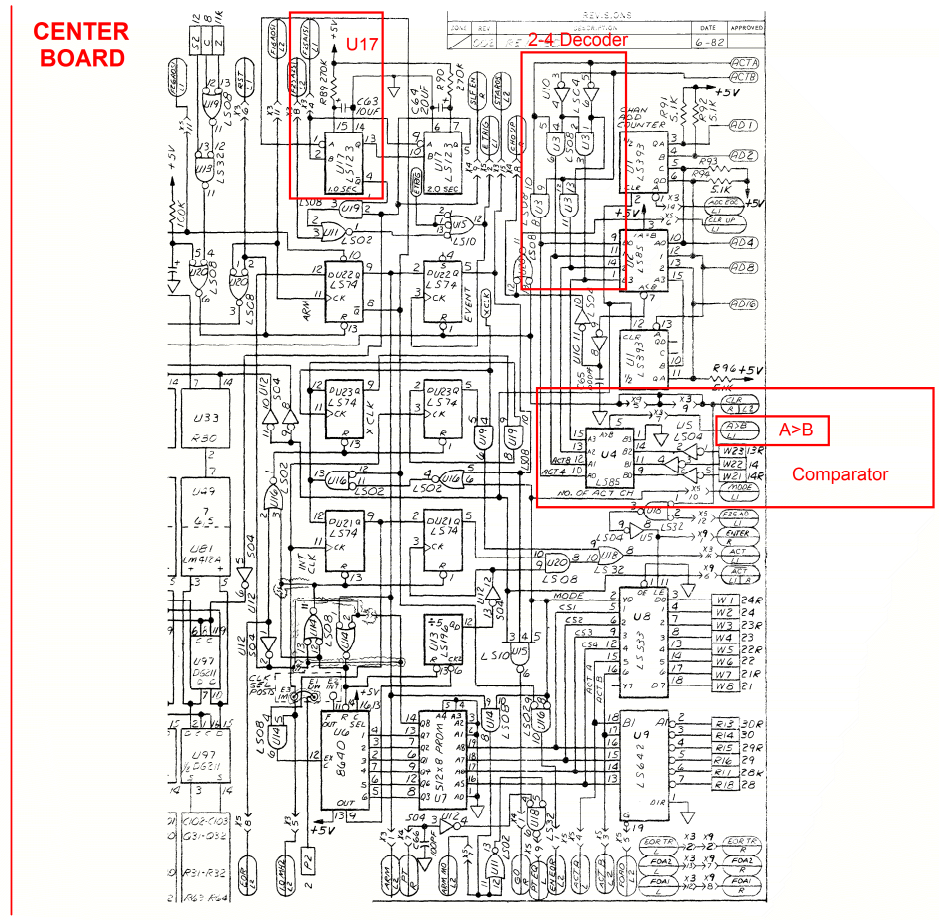


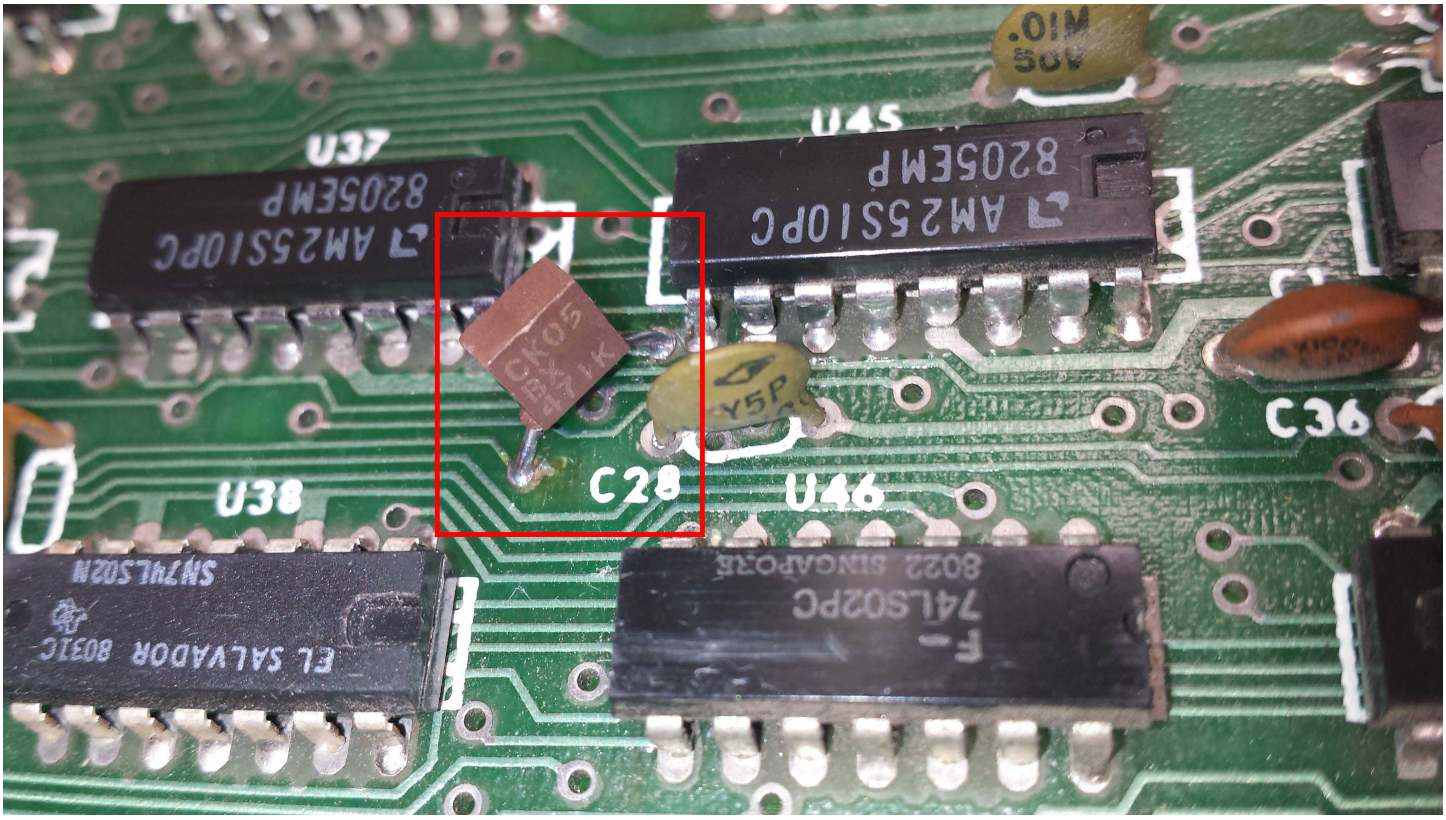
When a 470pf capacitor is placed between U16 pin 19 and ground of the left board, this glitch is filtered out, and is no longer seen by the PROM. Ground is available next to U45 pin 9, and a feed-thru that connects to U16 pin 19 is in between U37 pin 16 and U38 pin 1. This is where the 470pf capacitor should be soldered to. The capacitor completely filters out the glitch, as shown below. It is recommended that all 908 Transient Digitizer modules receive this modification.

The purpose of the magnitude comparator is to disable the F(16) A(1) Enable Unload command and return NOT Q if the user attempts to read back a channel that was not digitized since the last ARM command. If the channel number that is requested to be unloaded is higher than the number of channels specified in the last ARM command, the magnitude comparator has nearly 350nS to disable F(16) A(1) before S1 activates. The 470pf capacitor delays the "A>B" line by only 60nSec, so it's still ready in plenty of time to do its job. It should be noted, however, that the 908 will still read back data, even though F(16) A(1) was disabled. The NOT Q that is returned upon the F(16) A(1) command is the indicator that the data is invalid.




LEFT BOARD
U3 PAL 10H8
U32 LS04
U16 74S472/ TBP18S42
A>B
Note: this is a misprint. It should read F26A1S1
U16 PROM


CENTER BOARD
U17
2-4 Decoder
A>B
Comparator


U37
U45
U38
U46
C28
C36
AM2510PC
74LS02PC
SN74LS02N

908 Transient Digitizer A1-6 Capacitor Mod

John Wertenbaker

05/28/2019

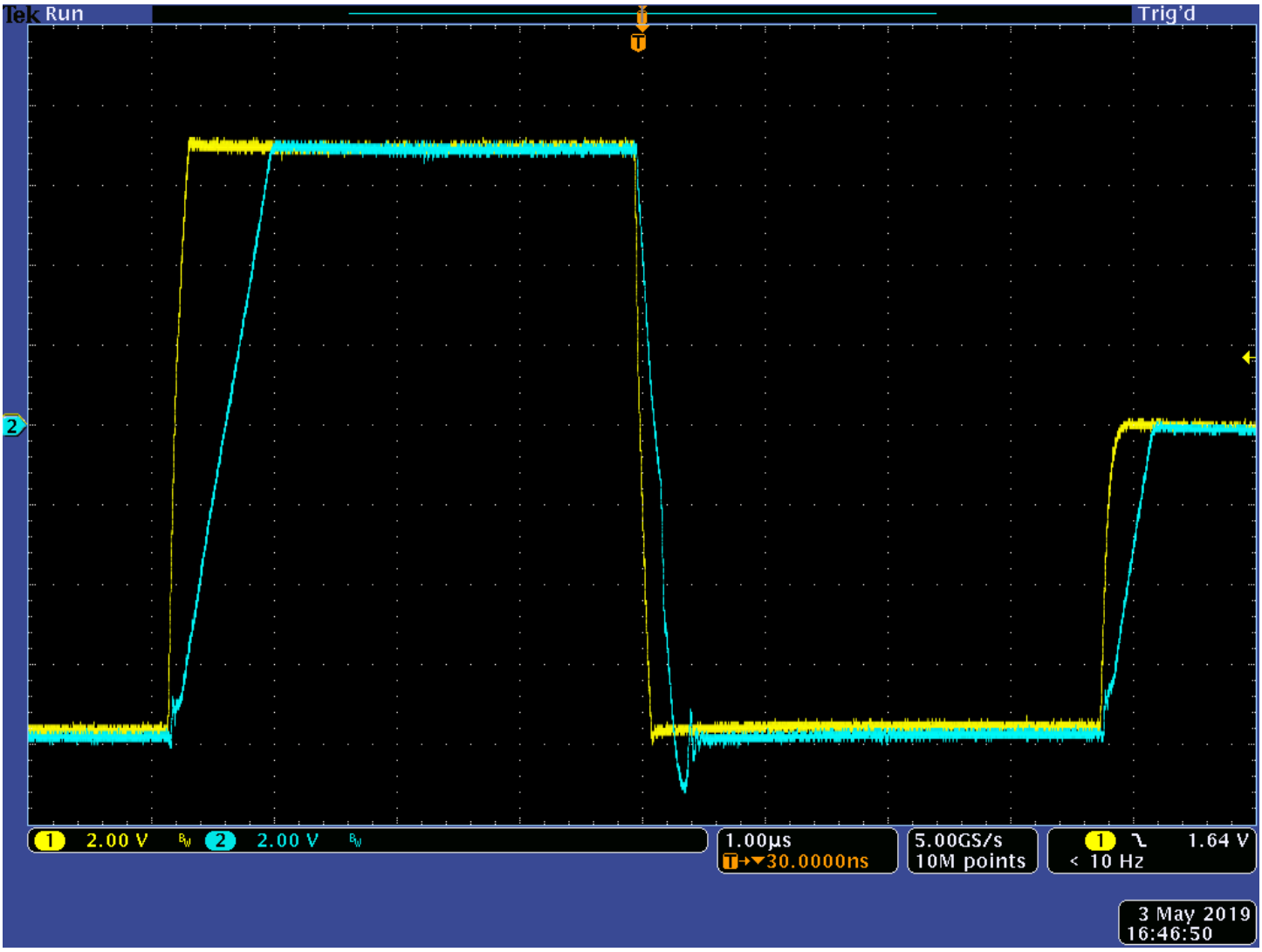
Many 908 Transient Digitizers have missing bits at the zero crossing, usually just into the negative voltages. This problem seems to be more common as the 908's age. In the past, the problem was alleviated by changing the ADC module. After a few swaps, it became apparent that some ADC's would work in some modules but not in other modules. A cause had to be found to really fix this problem.

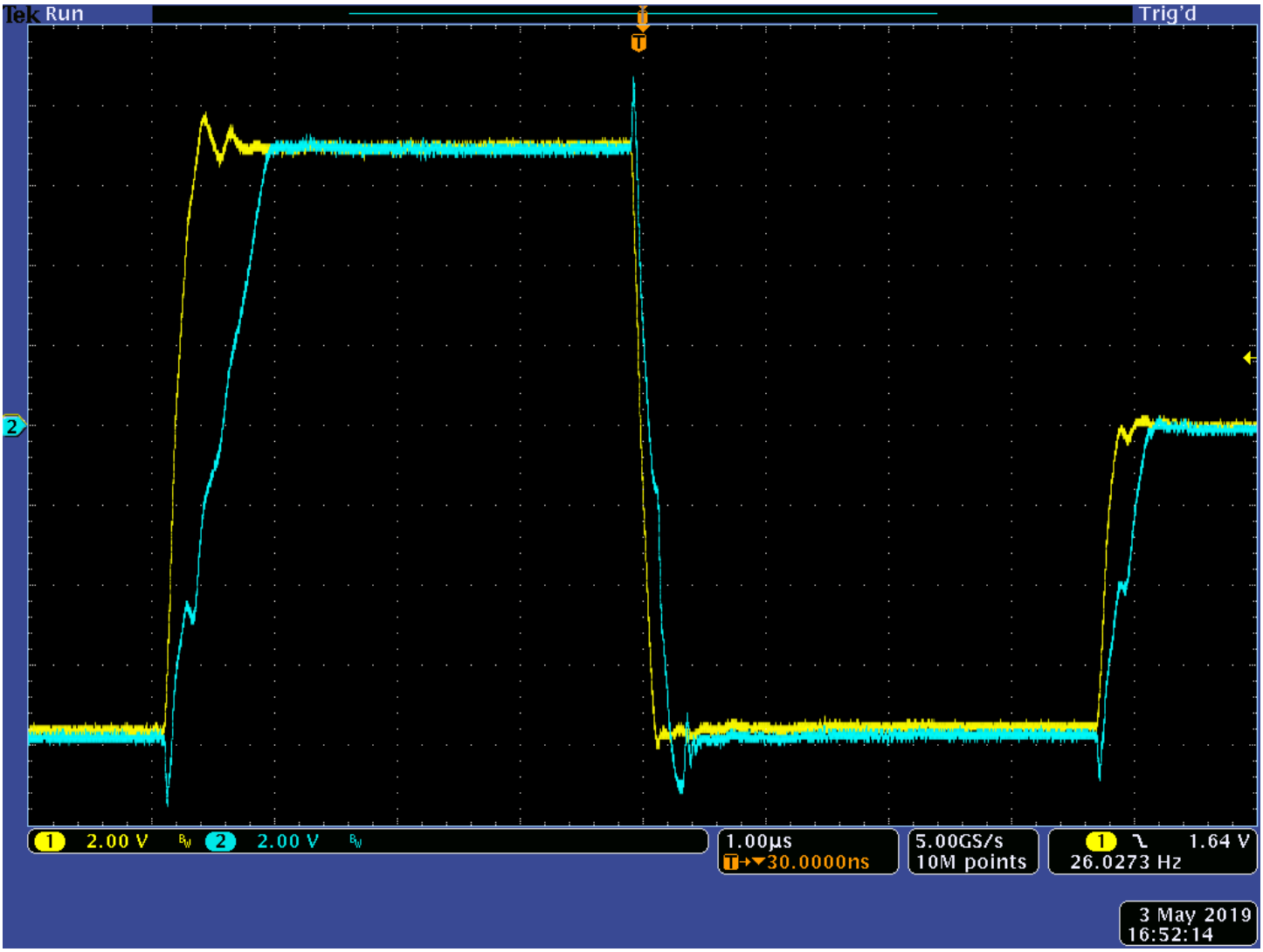
Timing of all the one-shots on the left board was investigated between a "good" and a "bad" board, but this ended in failure, as both boards had nearly identical timing. Replacing bypass capacitors near the 15V regulators was tried, but this didn't work either. Replacing one of the 15V regulators to make the +15V more closely match the -15V didn't work. Installing a filter module in a nearby slot cleaned up most of the bit noise in the 908, but it did nothing to fix the missing bit problem.

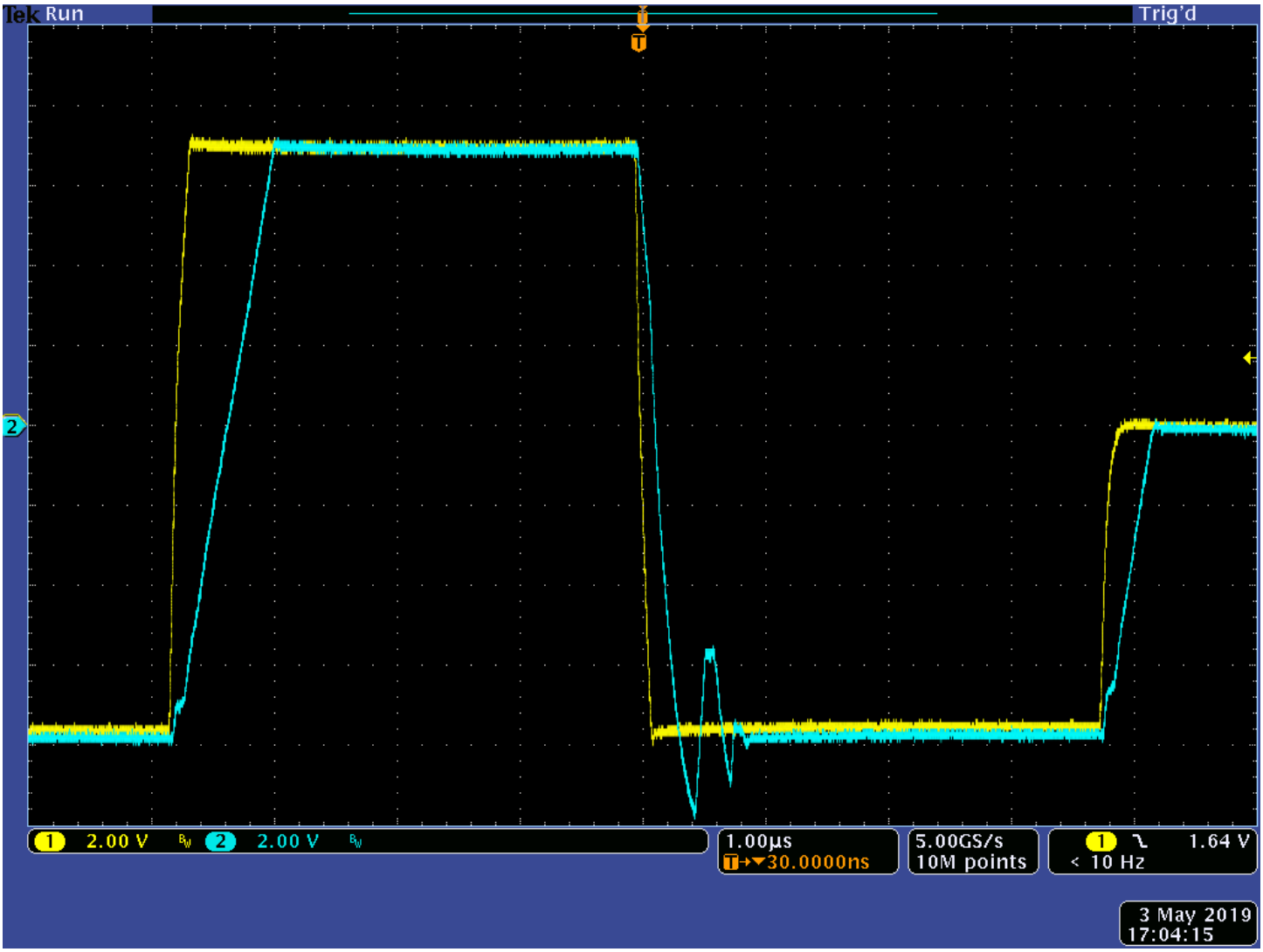
So far, the only thing found that works is a 100pf capacitor placed on the output of the op-amp A1 on the left board. The capacitor was tried on the input of the A1 op amp, but this didn't help the problem. Curiously, though, larger capacitor values on the output don't fix the problem as well as the 100pf capacitor. The capacitor is filtering noise on the input of the ADC. This noise just may be coming from inside the ADC, but this has not been proven.

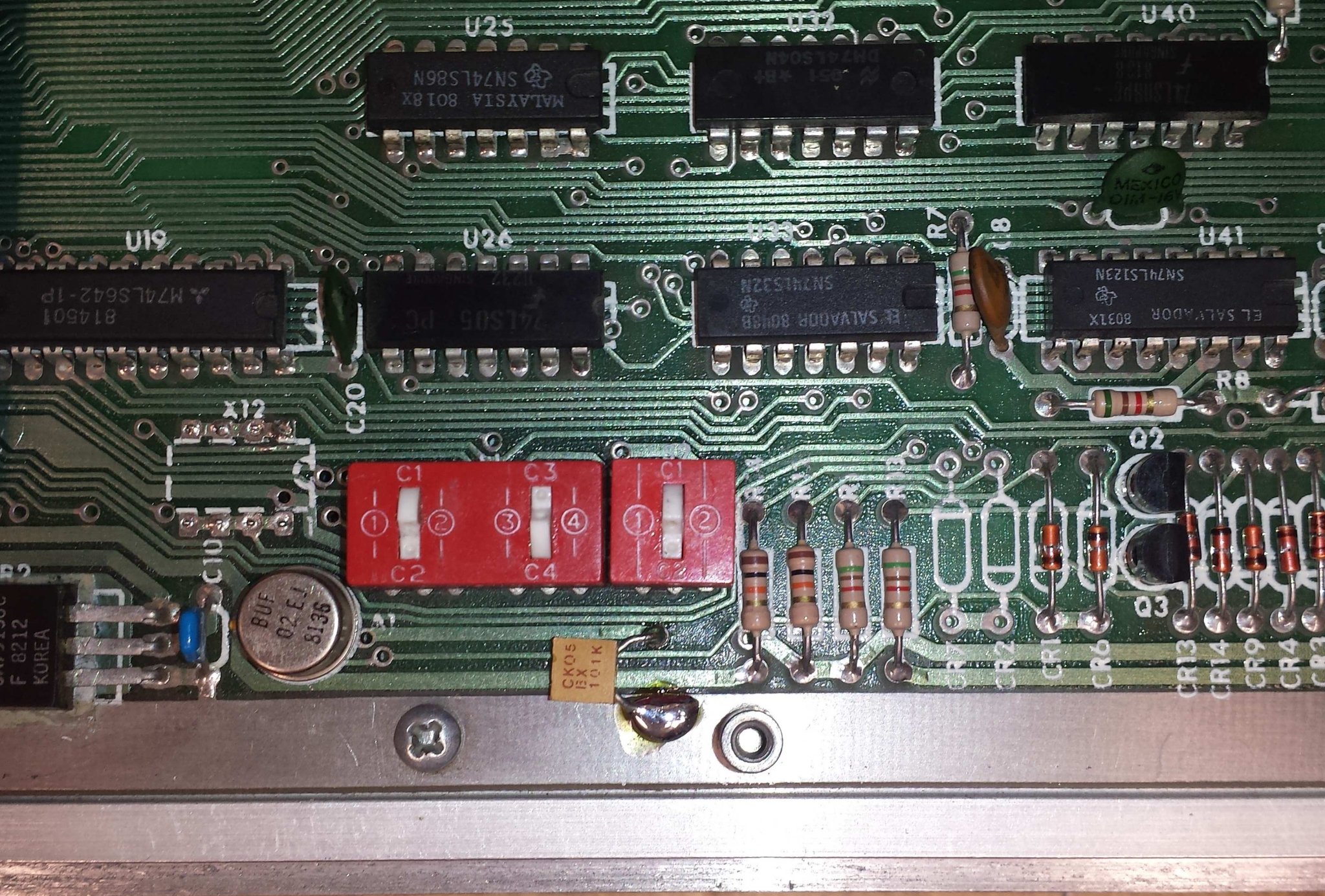
After this capacitor mod, the 908 was tested for the channel crosstalk problem, but the mod did not significantly affect it.

The first picture is with no capacitor. The yellow trace is the input of A1, and aqua is the output of A1. The second picture is with the capacitor on the input of A1. The third picture is with the capacitor on the output of A1.


Tek Run
Trig'd
2
1 2.00 V
2 2.00 V
1.00µs
30.0000ns
5.00GS/s
10M points
1 1.64 V
< 10 Hz
3 May 2019
16:46:50


Tek Run
Trig'd
2
1 2.00 V
2 2.00 V
1.00µs
30.0000ns
5.00GS/s
10M points
1 1.64 V
26.0273 Hz
3 May 2019
16:52:14


Tek Run
Trig'd
2
1 2.00 V
2 2.00 V
1.00µs
30.0000ns
5.00GS/s
10M points
1 1.64 V
< 10 Hz
3 May 2019
17:04:15


U25
U19
U26
U33
U41
U40
X12
C20
C1
C3
C2
C4
C1
C2
R7
R8
Q2
Q3
BUF
Q2 E.J
8136
CR7
CR2
CR1
CR6
CR13
CR14
CR9
CR4