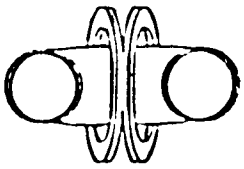

CICADA SYSTEM
SPECIFICATION

DOCUMENT NO.
TFTR-10C6-H910A

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DATE - 03/14/84

SUBJECT FUNCTION GENERATOR MODULE

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REVISIONS

DATE	DESCRIPTION
03/15/84	Revision to Section 6.12.3 (page 15) Revision to Section 6.12.8 (page 19)

Function Generator Module

1. Abstract.

This specification, in conjunction with referenced documents, sets forth all characteristics of subject module. The intended use of this document is to provide a minimum design goal for the module as well as a working document for subsequent users.

NOTE: Revisions from the previous issue of this document are identified by a vertical bar in the outer margin of the page.

2. Reference Documents.

2.1. IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Std. 583-1975

2.2. Printed Circuit Board Fabrication and Assembly CICADA Handbook Volume I, TFTR-10A2-H54B

2.3. Electronic Schematic, CICADA Handbook Volume I, TFTR-10A2-H55

2.4. Printed Circuit Artwork, CICADA Handbook Volume I, TFTR-10A2-H53A

2.5. Reliability, Quality Control, and Temperature Cycling, CICADA Handbook Volume I, TFTR-10A2-H58

2.6. Standard Timing Pulse, CICADA Handbook Volume I, TFTR-10A2-H57

2.7. Remote Memory Module, CICADA Handbook Volume I, TFTR-10C6-H903

3. Introduction.

The CAMAC module specified will be used as an interface between elements of the Tokamak Fusion Test Reactor (TFTR) and the Central Instrumentation Control and Data Acquisition (CICADA) computer system. The module will be housed in a CAMAC crate (see Reference 2.1). The module will function as a four (4) channel digital to analog converter to be used as a function generator.

4. Basic Features.

The module shall be a single width CAMAC module and shall house four (4) high speed digital to analog converters and necessary

circuitry to load and unload an external memory module with 32 K (32,768) twelve (12) bit words.

The module shall provide the circuitry for loading the external memory with data transferred from the CAMAC Dataway and upon command, unload the memory to either its internal digital to analog converters (DAC) or to the Dataway for write verification. Clocking of the data to the DAC's may make use of either an internal clock derived from a 1 MHz clock on Dataway line P2 or an externally supplied clock. All four (4) channels shall utilize the same clock signal. The module may be commanded to free run or to run through its assigned memory some preprogrammed number of times (15 maximum).

Through CAMAC command, the module shall be capable of being configured to cycle through a desired number of memory words (32 K maximum total). A fifteen (15) bit register shall be used to indicate the number of memory words to be used for each active channel. Upon outputting the desired number of memory words for each active channel, the memory control logic shall recycle to the zero location word.

It should be noted that the number stored in this register is the number of words for each channel and must be multiplied by the number of active channels to ascertain the total amount of memory used. If this total quantity exceeds 32 K words, each memory partition will recycle through its own zero location (see table on page 13) after address $7FFF_H$ is reached. Arming and starting of the execution through memory may be accomplished through CAMAC command or through use of an external trigger pulse. The use of the assigned memory shall be partitoned equally among active channels. The number of active channels (1, 2, or 4) shall be set by CAMAC command. Inactive channels shall have their DAC set for zero output. The module analog outputs (4), clock input, buffered clock output, start input, arm input, "active" output, and "recycle" output shall be interfaced through the front panel. The module memory interface shall be interfaced through the rear auxiliary connector.

5. Mechanical Characteristics.

5.1. The module shall conform to mechanical specifications as indicated in Reference 2.1.

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5.2. The module shall be a single (1x) width CAMAC module.

5.3. The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA type FR-4 or equivalent. The circuit board shall be either a "two-sided" printed circuit board with etched conductors or a "two-sided" board using Multiwire technology. The fabrication of the circuit board shall be in compliance to Reference Specification 2.2.

5.4. This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate (see Reference Specification 2.1). In addition, the module shall be equipped with aluminum side covers for both the component and foil side of the circuit board. Covers shall be insulated in a manner to preclude shorting of conductors on printed circuit board and top covers shall have cutouts to expose all switches and fuses on the module.

5.5. All components are to be identified with a standard manufacturer's part number or standard method of marking (e.g., resistor color coding) and shall have an exact replacement available from a second source manufacturer.

5.6. All electrical components are to be mounted on only one side of the board.

5.7. The condition of this module is to be monitored by LED's located on the module front panel. See Figure 11.1 for the suggested front panel layout. All lettering on the front panel shall be either engraved or silkscreened. The front panel material shall be aluminum with an iridite finish with contrasting colored lettering.

5.8. All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part number on the electronic schematic associated with this module. See Reference Specification 2.3.

5.9. External connections to the module shall be accomplished through use of ten (10) front panel connectors as well as the rear edge "auxiliary" connector. Front panel connectors shall be utilized as follows:

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J1 - External start pulse input (Start)

J2 - External arm pulse input (Arm)

J3 - External clock input (Clk in)

J4 - Buffered clock output (Clk out)

J5 - "Module Active" output (ACT)

J6 - "Recycle" output (RECY)

J7 - Analog output CH0

J8 - Analog output CH1

J9 - Analog output CH2

J10 - Analog output CH3

The rear auxiliary connector shall be used for connection to the external memory module. Pin asignments for all connectors shall conform to Table 11.2.

5.10. Circuit board layout shall be designed physically to separate analog components from the CAMAC dataway connector and from other digital components. It is suggested that the DAC components and any analog drivers required, be mounted toward the front of the circuit board utilizing as much copper clad ground plane as possible. In addition, it is suggested that analog and digital ground connections be isolated from each other except at a single ground point.

6. Electrical Characteristics.

6.1. Dataway Interface shall conform to specification as indicated in Reference 2.1.

6.2. Input Power shall be derived from the satndard +/- 6 volt and +/- 24 volt CAMAC supply voltages. Whenever possible, low power circuitry (such as the 74 LS series) shall be used.

6.3. The + 6 and - 6 supply voltages used must be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The + 24 and - 24 volt supply voltages used must be bypassed with electrolytic capacitors of at least 6.8

microfarads. In addition, at least half the integrated circuits must contain a ceramic bypass capacitor of at least .01 microfarads on their supply voltage lines. The .01 microfarad capacitors should be distributed on the circuit board and be located as close as possible to noise sensitive components.

6.4. All components on this module must have an MTBF rating as specified in Reference 2.5.

6.5. Analog Output Characteristics.

The module shall have four (4) identical output channels available on the front panel connectors. Each output shall utilize IC current drivers such as the LH0002 (National) or HA2630 (Harris) in a closed loop configuration.

Output Type: Differential, balanced to ground

Common Mode Offset: +/- 10×10^{-3} volts worst case as measured from each output to ground, with DAC commanded to zero at 25^{0}C (Trimmable to zero)

Drive Capability: +/- 10 milliamp (minimum)

Resolution: 12 bits (2.5 millivolts (MV) for 10 volt range)

Nonlinearity +/- 1/2 LSB (maximum) from 0 to 50^{0}C The method of testing this parameter shall extend a straight line between the actual minimum and maximum output values. The deviation from this line for all points on the D/A output curve shall be 1/2 LSB maximum. (Integral nonlinearity using end point linearity.)

Output Range: Each channel shall have a selectable output range determined by the position of circuit board mounted switches (one set of switches per channel). Selectable ranges:

+10.235 volt to -10.240 volt (5 MV/bit)
+ 5.117 volt to - 5.120 volt (2.5 MV/bit)
0.000 volt to +10.237 volt (2.5 MV/bit)
0.000 volt to + 5.118 volt (1.25 MV/bit)

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Absolute accuracy measured at 25^0C with line to line (differential output) load values of from 120 ohms to an open circuit.

Line to Line (differential) +/- .03% of Full Scale
Line to Ground (each output) +/- .03% of Full Scale

Setting Time for a full scale change over all ranges (maximum) with a 120 ohm load resistor shunted with 5000pf.

2 microseconds to 0.5% of FS +/- 1.2 LSB
6 microseconds to .03% of FS +/- 1.2 LSB

Temperature coefficient of both gain and offset: 50 PPM/^{0}C of full scale (maximum total).

Glitch Energy: The maximum allowable glitch for any change of output value shall be 250 x 10^{-12} volt sec as measured across a 120 ohm load resistor.

The output stage shall be capable of withstanding a line-to-line and/or a line-to-ground short indefinitely without sustaining any permanent damage.

The module shall be monotonic throughout the temperature range of 0 to 50^0C.

6.6. Status Outputs.

The module shall have two (2) TTL level outputs buffered by an SN74128 line driver available on front panel connectors.

6.6.1. The "Active" output shall be true (output high) within 100ns of the receipt of a valid module trigger (as defined in Section 6.6.2) and false within 100ns of the last clock cycle which ends the DAC sequence (module stopped). In addition, this output shall also be driven false within 100ns of receipt of a module "stop" command (from Dataway).

6.6.2. The "Recycle" output shall be a positive going pulse of from 1.0 musec to 1.5 musec that shall occur whenever the memory address counter(s) recycle through the zero location and whenever a valid "Start" command is received (logical OR of the two conditions). The valid start command is defined as a start command received from either the Dataway or the front panel connector when the module is armed but not yet active (see paragraph 6.11.5). The leading edge of this output shall occur within 100nsec of the triggering source (loading of zero location data or valid "Start" command).

6.7. Memory Interface.

The module shall interface to an external memory module through use of the thirty-six (36) pin rear auxiliary connector. Signal (data, address, and strobes) interfaces shall be implemented with tri-state "bus drivers" to drive the required interconnecting cable. The signal levels and timing shall be compatible with the TFTR Remote Memory Module Type 903 (Reference Specification 2.7) as indicated by Figure 11.3 and Figure 11.4.

6.8. Throughput.

The module memory control shall have a minimum throughput (Dataway/memory or DAC/memory) of 1 MHz. To accommodate the simultaneous updating of up to four (4) DAC's, each DAC must be equipped with two (2) data registers. Upon receipt of a DAC update clock, data shall be transferred from register to register in a "pipeline" fashion. After the output register is updated from the input register, the input register for each DAC shall in turn be updated with the next data word from the external memory. In addition, a separate data register (Dataway buffer) shall be used for communication between the CAMAC Dataway and the external memory. When the module is in the process of transferring data from memory to the Dataway, the Dataway buffer shall queue the next word in memory after each unload command. To preclude problems that would occur if Dataway reconfigure commands are received while the module is armed and/or active (armed and triggered) all such commands shall be ignored during these periods. If the user desires to reconfigure a module (i.e., issue Command #7, Set Module Status), the user must either ascertain that the module is in the Dataway mode by using Command #2 or must issue Command #9 to force the module into the Dataway mode. The commands "Arm Module," "Stop Scan," "Read Status," "Read Module Number," "Read Samples/Channel," and the signals Z+C, will, however, be accepted and executed during all operating states and

modes of the modules.

6.9. DAC Clocking.

All active DAC output registers shall be updated by the same clock signal. The selected of the desired clock shall be accomplished through use of CAMAC commands. In addition, the selected clock (buffered) shall be available on a front panel connector for use by external devices.

The clock divider circuits shall be designed to utilize the low to high transition of either P2 clock or the external clock to toggle internal counters. DAC updates shall occur - 0ns to + 100ns from a low to high transition of the source clock. In addition, the divider circuits shall be designed to issue the first DAC update signal within one source clock period after receipt of a valid trigger. The second and subsequent DAC clock signals shall then be timed to the period of the selected clock.

6.9.1. The internal clock shall be derived from a one megahertz (1 MHz) clock signal available at CAMAC Dataway line P2. The clock signal supplied to the module on P2 shall be TTL level compatible, with a duty cycle of 50% +/- 20%. The module shall impose a maximum of one standard TTL load on this clock input.

The module shall have clock frequency divider circuits counting down from this supplied clock to allow for the selection of various DAC clocking rates through use of CAMAC commands.

Selectable rates:
200 Hz
500 Hz
1000 Hz
2000 Hz
5000 Hz
10,000 Hz
20,000 Hz
50,000 Hz

6.9.2. The external clock shall be interfaced through a front panel connector. Electrical connection to the external clock shall make use of a Type 2601 (Hewlett Packard Corp.) optoisolator, impedance matched for 120 ohm transmission line (see Figure 11.5). The DAC register update shall respond to the low to high transition of the incoming signal. The external clock shall have a nominal pulse width of 1 microsecond with a maximum fre-

quency of 250 KHz. When the use of this clock is selected through CAMAC command, clock divider circuits shall not be available.

6.9.3. The clock output signal shall be interfaced through a front panel connector and shall be a differential output compatible with the external clock input (see Figure 11.6). The clock output shall be synchronized with the internal DAC update clock (either internally derived or externally supplied) and shall have a nominal pulse width of 1 microsecond with the low to high transition being the active edge. The maximum delay between the active edge of the external clock input and clock output shall be 50 nanoseconds as measured at the 2.5 volt point with 120 ohm load on the output clock.

6.10. Memory Control.

The remote memory module connected to the Function Generator shall be under full control of the Function Generator module. Each transfer to or from memory must be accompanied by the appropriate memory address and an appropriate "read" or "write" strobe signal. Data transfers between the Dataway and memory shall make use of a memory address pointer that is initialized by CAMAC command and then incremented as memory accesses occur.

Through CAMAC command the module may be configured to cycle through memory using less than the full 32 K words. This feature shall be used by loading a fifteen (15) bit register with the number of memory words to be used for each channel. The register may be loaded and read through CAMAC commands. The default value which shall exist after Z+C power up shall be zero. The memory control circuit shall have two (2) distinct modes of operation to accommodate either Dataway transfers or DAC transfers. The determination of the operating mode is accomplished by CAMAC commands.

6.10.1. The Dataway operating mode shall exist after power up, after receipt of Z+C, or after receipt of the appropriate CAMAC command (Command #6 Load Address Pointer). When in this mode, the module shall ignore all input signals ("start," "stop," and "clock") with the exception of the CAMAC Dataway. When this mode is initiated by power up or reset (Z+C), the address pointer shall be set to the zero location and the module shall be set to transfer data from the Dataway to the remote memory. When this mode is initiated by the CAMAC command, "Load Address Pointer," the address pointer as well as the data direction (Dataway to Memory/Memory to Dataway) must be set in response to the command. When the command indicates that transfers of data from memory to

the Dataway will follow, the memory control circuit shall fetch and queue up the first requested word for subsequent transfer. If the DAC mode is active when a transfer to Dataway mode is sensed, this Dataway command shall be ignored and the DAC update continued.

6.10.2. The DAC operating mode shall exist after receipt of a module arm command. Upon entering this mode, the memory control circuit shall transfer the first DAC word for each active channel to the DAC to output the voltage corresponding to that data word. The first data word for each active DAC will be loaded after receipt of the arm command and will be held until the first update clock is received (internal or external sourced). The DAC will proceed to update its output value in response to clock pulses. When operating in multiple scan mode, the update will continue until the required number of updates (memory words) is satisfied. At the conclusion of the sequence, all active DAC's will hold the last commanded voltage and the "Module Active" output signal will be driven to the false state.

6.11. Operating Modes and Procedure.

6.11.1. Active Channels.

The number of active channels may be selected by CAMAC command to be 1, 2, or 4 channels. All inactive channels shall have their output DAC set for zero volt output. When the entire 32 K words of memory are used, the utilization of memory shall be as follows:

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NUMBER OF CHANNELS ACTIVE	CHANNEL USED	MEMORY SIZE	MEMORY ADDRESS
1	CH0	32 K	$0000\text{-}7FFF_H$
2	CH0	16 K	$0000\text{-}3FFF_H$
	CH1	16 K	$4000_H\text{-}7FFF_H$
4	CH0	8 K	$0000\text{-}1FFF_H$
	CH1	8 K	$2000_H\text{-}3FFF_H$
	CH2	8 K	$4000_H\text{-}5FFF_H$
	CH3	8 K	$6000_H\text{-}7FFF_H$

When less than 32 K words are being used, each channel will have its first location the same as indicated above and extend to the commanded end point.

6.11.2. Clock Selection.

The clock selection for the module is accomplished through CAMAC command as delineated in Section 6.9 and Section 6.12.7.

6.11.3. Mode Selection.

The module shall be capable of a continuous scan mode or a multiple scan mode. The operating mode shall be set by CAMAC command. All output channels of the module shall operate in the same mode and shall be started by the same "start" signal.

Upon receipt of the "mode select" command, all channels will be stopped, the output DAC's set to hold the last commanded voltage, and the first word from memory will be queued to be outputted after the module is armed.

When operating in multiple scan mode, once started, each active channel will cycle through its dedicated memory partition from one (1) to fifteen (15) times. After the commanded number of cycles are complete, the next clock pulse shall be used to stop the

module scan and shall set all output channels to hold the last commanded voltage. Subsequent "start" signals received while the module is scanning shall be ignored.

Stop command received while the module is scanning shall asynchronously stop the scan and set all outputs to hold the last value and disarm the module. Stop commands received while the module is "armed" but not yet started will also "disarm" the module.

When operating in continuous scan, once started, each active channel will cycle through its dedicated memory partition continuously, switching back to the first location after the last word is read. The module will continue the scan until such time as a stop signal is received or a new "arm" command is received. Subsequent "start" signals received while the module is cycling shall be ignored by the module. As stated in paragraph 6.11.1, the memory area for each channel will have a dedicated starting location. The block length, however, is loaded by CAMAC command for application needing less than the available memory.

6.11.4. Arm Command Function.

The arm function is a decoded CAMAC command or external pulse. The receipt of this command is required before a DAC sequence may commence. Once "armed" the module will remain in the armed state until such time as one of the following conditions occur:

a. Receipt of a "stop"command

b. Receipt of start followed by the commanded number of iterations through memory complete

6.11.5. Start Command Function.

The module will respond to this command whenever the module is armed. The module start command can originate at any time from either the front panel connector or from a decoded CAMAC command. When the start command is received, the address control circuitry is forced to the zero location for each channel and the memory scan is started. Start commands received while the module is either unarmed or while the module is active will be ignored. The command may be issued by CAMAC command or external pulse. Both the external "Arm" and "Start" pulses shall be optically isolated and comply with the characteristics of a CICADA Standard Timing

Pulse (see Reference Specification 2.6).

6.11.6. Stop Command Function.

The stop command may originate any time from two sources as does the start command. When the stop command is received, the module will stop the memory scan and set all channel outputs to zero volts and disarm the module. The stop pulse characteristics shall be a Standard Timing Pulse as is the start pulse.

6.12. CAMAC Commands.

6.12.1. Command #1 Read Memory [F(0).A(0)] (Read Data Returned).

This command gates the contents of the Dataway data buffer onto the CAMAC Dataway read lines R1 through R12 with the LSB on R1 (R13 through R24 always zero). The module circuitry will reload the buffer with the next memory word after the CAMAC transfer is complete. The module will respond to this command (Return Q=1) only if it was previously set up by Command #6 for data transfers from Memory to the Dataway and the module is not in the process of scanning. If the command is received while the module is not able to respond, the module will return X=1, Q=0, and a data field of all zeros.

6.12.2. Command #2 Read Channel Status F(1).A(n) Read Data Returned.

This command gates the operating status of channel n (n=0,3) onto the dataway read lines. The data returned shall be formatted as follows:

R1-R3 Number of channels active

1 = 1 Channel active

2 = 2 Channels active

4 = 4 Channels active

OtherNot assigned

R4-R5 Channel output range

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(Settable by hardware switches)

0 = +10.235 volt to -10.240 volt (5MV/bit)

1 = + 5.117 volt to - 5.120 volt (2.5MV/bit)

2 = 0.000 volt to +10.237 volt (2.5MV/bit)

3 = 0.000 volt to + 5.118 volt (1.25MV/bit)

R6-R8 Module Status

0 = Unarmed

1 = Armed not active

2 = Active

3 = Dataway mode

R9-R11 Clock Selected (internal)

0 = 200 Hz

1 = 500 Hz

2 = 1,000 Hz

3 = 2,000 Hz

4 = 5,000 Hz

5 = 10,000 Hz

6 = 20,000 Hz

7 = 50,000 Hz

R12

0 = Internal Clock

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1 = External clock

R13-R16 Scan Iterations

0 = Continuous scan

1 = 1 Scan iternation

. .
. .
. .

15 =15 Scan iterations

R17-R24 Always Zero

The module will respond (Q=1, X=1) to this command during all modes of operation.

6.12.3. Command #3 Read Samples/Channel F(0).A(2) Read Data Returned.

This command gates the binary contents of the register used to set the number of memory words to be used during scan onto the Dataway read lines R1 through R15 with the LSB on R1 (R16 through R24 aways zero). All values from 0 to 7FFF are valid indications of the quantity previously loaded into this register by Command #8. The module will respond (q=1, X=1) to this command during all modes of operation.

6.12.4. Command #4 Read Module Number F(6).A(0) Read Data Returned.

This command gates the module identification number (decimal 910, hexadecimal 38E) onto the Dataway read lines R1 through R12 (R13 through R24 always zero). The module will respond (Q=1, X=1) to this command during all modes of operation.

6.12.5. Command #5 Load Memory [F(16).A(0).D(YYYYYY)].

This comamnd loads the twelve (12) LSB's (W1-W12) of the dataway write lines into the module Dataway buffer register. The received data will subsequently be loaded into the remote memory location

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indicated by the dataway memory address register. The dataway memory address register shall be incremented after the memory transfer is complete. The data loaded for subsequent conversion shall be presented as straight binary for unipolar operation and two's complement for bipolar operation as determined by the board mounted switches.

The module will respond to this command (Q=1, X=1) only if it was previously set up by Command #6 for data transfers from the Dataway to Memory. If the command is received under any other condition, the command will be ignored (Q=0, X=1).

Examples of Data Coding

Unipolar Settng 0.000 volt to +10.238 volt (2.5MV/bit)

Voltage	Code
0.000 V	0000 0000 0000
+ 2.560 V	0100 0000 0000
+ 5.120 V	1000 0000 0000
+10.237 V	1111 1111 1111

Bi-Polar Setting +5.117 volt to -5.120 volt (2.5MV/bit)

Voltage	Code
+ 5.117 V	0111 1111 1111
+ 2.560 V	0100 0000 0000
0.000 V	0000 0000 0000
- 2.560 V	1100 0000 0000
- 5.120 V	1000 0000 0000

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6.12.6. Command #6 Load Address Pointer [F(16).A(1).D(YYYYYY)].

This command transfers the sixteen (16) LSB's (W1-W16) to the Dataway write lines to the module for use as follows:

Bits W1-W15

This field contains the absolute memory address from which the next Dataway cycle shall either read from or write to.

Bit 16

1 = Memory reads to follow

0 = Memory writes to follow

The module will not respond to this command if the command is received while the module is armed or active (Q=0, X=1) otherwise Q=1, X=1 shall be returned.

See note 1 on Page 28

6.12.7. Command #7 Set Module Status [F(17).A(0).D(XXXXXX)].

This command utilizes the CAMAC write lines to set up the module DAC mode of operation. The CAMAC wirte lines are utilized as follows:

W1-W3 Active channels

1 = 1 Channel active

2 = 2 Channels active

4 = 4 Channels active

Other values not assigned and if used will result in the entire command being ignored

W4-W8 Not used

W9-W11 Set Internal Clock Rate

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0 = 200 Hz

1 = 500 Hz

2 = 1,000 Hz

3 = 2,000 Hz

4 = 5,000 Hz

5 = 10,000 Hz

6 = 20,000 Hz

7 = 50,000 Hz

W12 Select Clock

0 = Internal clock

1 = External clock

W13-W16 Set Scan Iterations

This field sets the number of times that the module memory will be scanned through before automatically stopping and setting all channels outputs to zero. Note that the scan may be stopped before the programmed number of scans is complete by a CAMAC stop command.

0 = Continuous

1 = 1 Scan iterations

2 = 2 Scan iterations

. .
. .
. .

14 =14 Scan interations

15 =15 Scan iterations

The module shall not respond to this command if the command is received while the module is armed or active or if unassigned data is transmitted on W1-W3 (Q=0, X=1), otherwise, Q=1, X=1 shall be returned.

6.12.8. Command #8 Set Samples/Channel F(16).A(2).

This command utilizes the CAMAC write lines W1 through W15 to set the number of samples (memory words) to be scanned before the module restarts at the zero location. Any quantity from 1 to $7FFF_H$ (corresponding to quantitites 2 to 32768;N+1) may be loaded and shall represent the number of updates each channel will be loaded with before recycling to its respective starting point.
See Note 2 on Page 28
The module shall not respond to this command if the command is received while the module is armed or active (Q=0, X=1), otherwise Q=1, X=1 shall be returned.

6.12.9. Command #9 Stop Scan [F(24).A(0)].

This command stops the module scan if it is active and forces the module into the unarmed state. Upon receipt of this command all DAC outputs will be set to zero volts and the module will then be able to respond to new configure commands. This command may be used to terminate a continuous scan or to abort an arm set up for subsequent reconfiguration. The module shall respond to this command (Q=1, X=1) during all modes of operation.

6.12.10. Command #10 Start Scan [F(25).A(0)].

This command performs the same function as would a start pulse received on the external "Start" input connector. If the module is armed and has not yet started scanning, then the scan will be started.

The module will respond (Q=1, X=1) to this command only if the module is in the armed state. If the command is received at any other time (i.e., not armed, dataway mode, scanning), the command will be ignored (Q=0, X=1).

See Note 3 on Page 28

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6.12.11. Command #11 Arm Module [F(26).A(0)].

This command as well as the external "Arm" pulse will arm the module to enable DAC scan after receipt of the start command or start pulse and clock signal. After receipt of this command subsequent reconfigure commands will be ignored until such time as either the scan sequence is complete or the module is given a stop command or stop pulse input. The module shall respond to this command (Q=1, X=1) during all modes of operation.

6.12.12. Initialize or Clear Z+C.

The module will respond to Z or to C or to power on by setting up the following conditions:

Samples/channel - full utilization (32 K total)

All clock selection internal 50,000 Hz

Scan mode, continuous

Status, unarmed

Channels active - 4

DAC output - zero

6.13. Front Panel LED's.

The module shall provide four (4) LED indicators for visibility from the front panel.

LED #1 (N) shall illuminate for approximately 100 milliseconds whenever N is received.

LED #2 (Active) shall illuminate whenever the module active output is true.

LED #3 (Recycle) shall illuminate for a minimum time of 100 milliseconds whenever the memory address counters recycle.

LED #4 (XCLK) shall illuminate whenever the external clock source is selected.

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7. Environmental Data.

7.1. The module shall operate, as defined, over an ambient temperature range of 0 to $+50^{0}$C.

7.2. The module shall operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3. The module shall operate, as defined, in the presence of an external magnetic field changing at a maximum rate of 200 gauss per second with a peak magnitude of 100 gauss in any direction.

7.4. The module must operate, as defined, in a radiation environment as follows:

Neutrons	2×10^{7} n/cm^2/sec
Rad-Dose	5×10^{-2} rad (Si)/sec
Integrated Dose	200 rad (Si)

8. Safety.

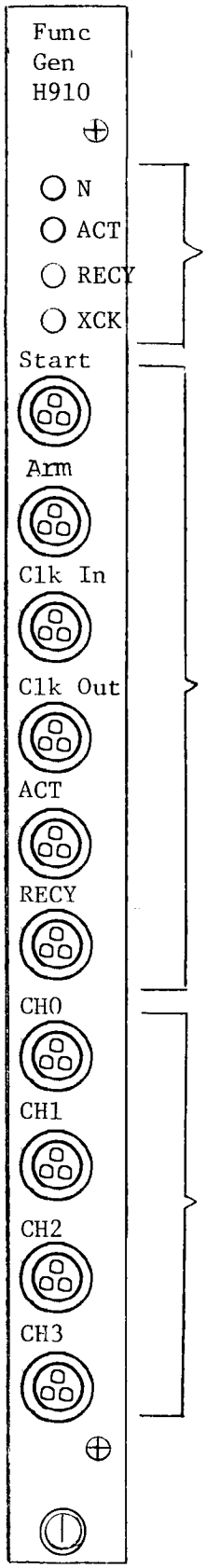
All components of this module must be of flame redardant material.

9. Testing.

All modules shall be subjected to a temperature cycling period followed by a functional test prior to shipment. A description of the tests to be performed shall be submitted by the bidder for incorporation into this specification.

10. Reliabiilty and Quality Control.

The module must meet all applicable requirements specified in Reference 2.6.



Status LED's

J1-J6 for
Timing Interfaces
LEMO Bulkhead Connector (3 pin)
Part Number RGOB303CA222

J7-J10 for
Analog Output
LEMO Bulkhead Connector (3 pin)
Part Number RGOB303CA222

Front Panel Layout

Figure 11.1

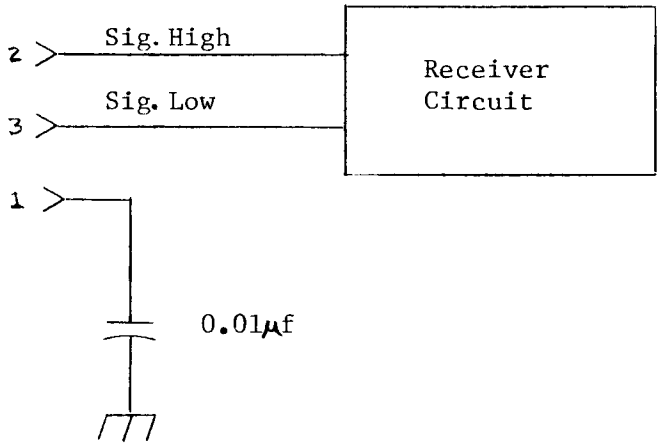
Pin	Function	Pin	Function
1B	MAB 19*	1A	MAB 1
2B	MAB 18*	2A	MAB 0
3B	MAB 17*	3A	GND
4B	MAB 16*	4A	DB 11
5B	MAB 15*	5A	DB 10
6B	MAB 14	6A	DB 9
7B	MAB 13	7A	DB 8
8B	MAB 12	8A	DB 7
9B	MAB 11	9A	DB 6
10B	MAB 10	10A	DB 5
11B	MAB 9	11A	DB 4
12B	MAB 8	12A	DB 3
13B	MAB 7	13A	DB 2
14B	MAB 6	14A	DB 1
15B	MAB 5	15A	DB 0
16B	MAB 4	16A	GND
17B	MAB 3	17A	Write Strobe
18B	MAB 2	18A	Read Strobe

*reference only

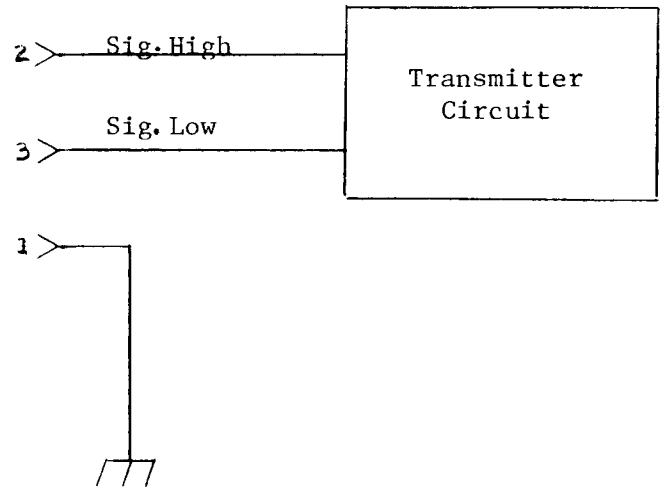
Auxiliary Connector

Pin Assignment

Table 11.2

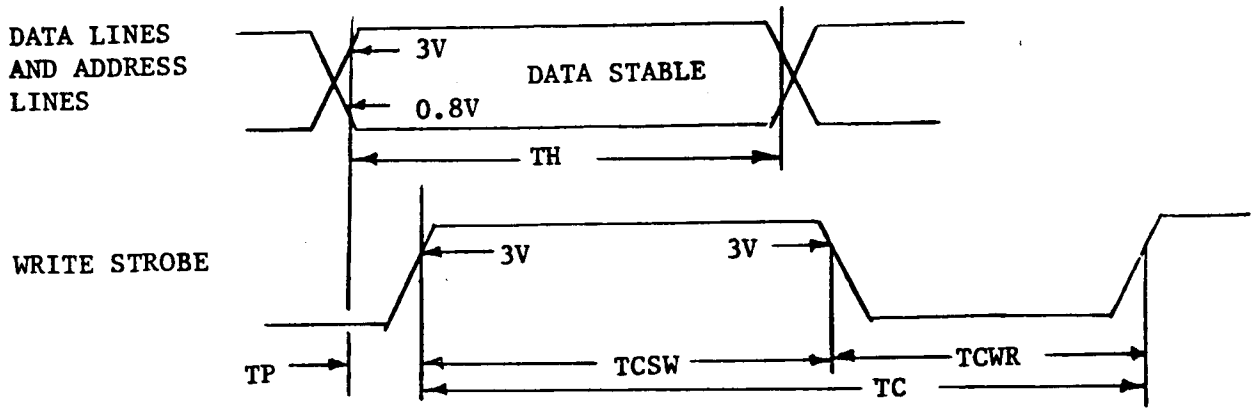


J1,J2 and J3
"LEMO" Type Connectors

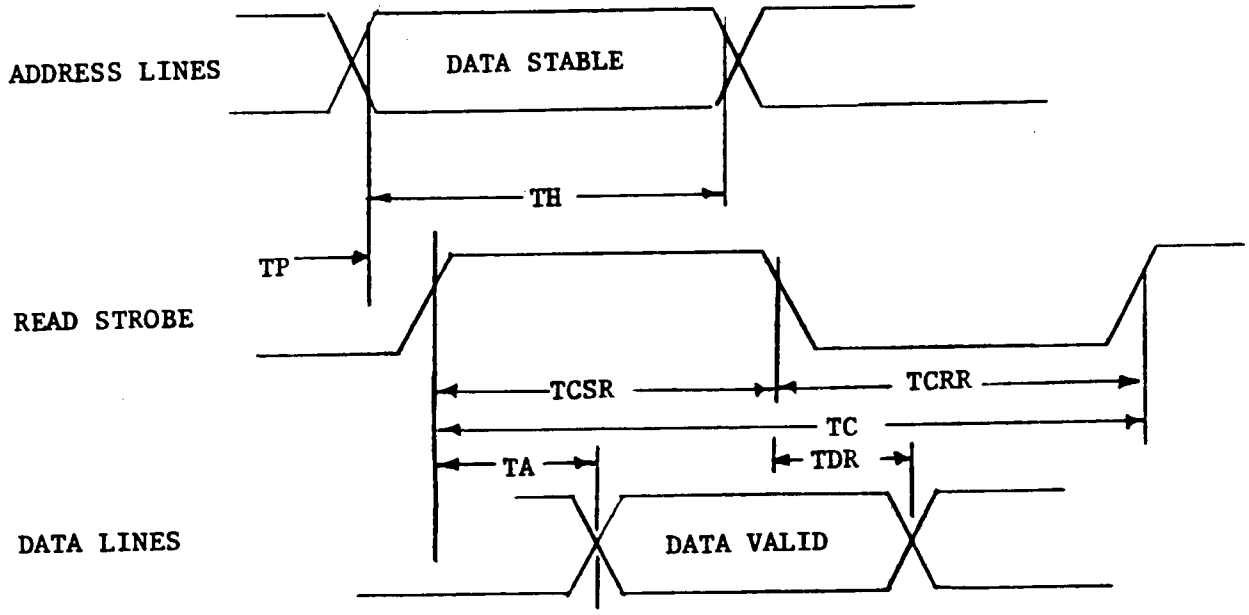


J4-J10 "LEMO"
Type Connectors

Table 11.2



WRITE CYCLE



READ CYCLE

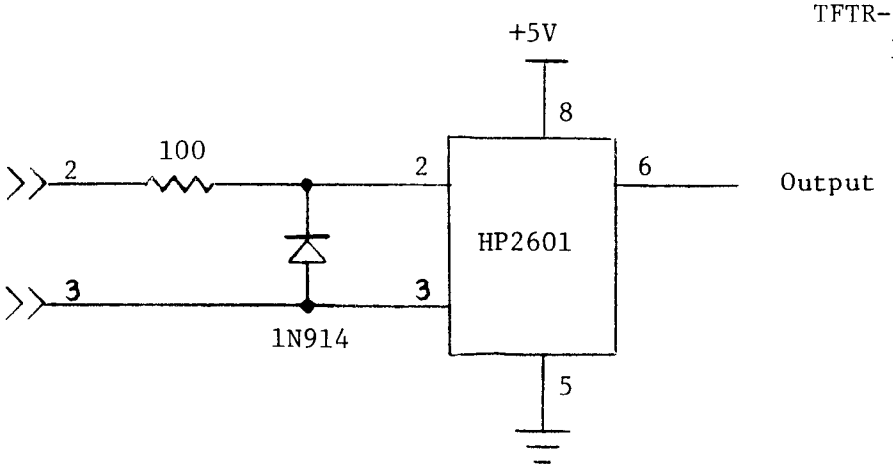
Typical Timing Diagrams

Figure 11.3

Characteristic	Symbol	Min	Max	Unit
Data Hold Time	TH	200	---	ns
Set Up Time	TP	0	---	--
Write Strobe Pulse Width	TCSW	25		ns
Write Recovery Time	TCWR	150	---	ns
Cycle Time	TC	450		ns
Read Strobe Pulse Width	TCSR	250		ns
Read Recovery Time	TCRR	150	---	ns
Access Time	TA	---	250	ns
Output Recovery Time	TDR	10	---	ns

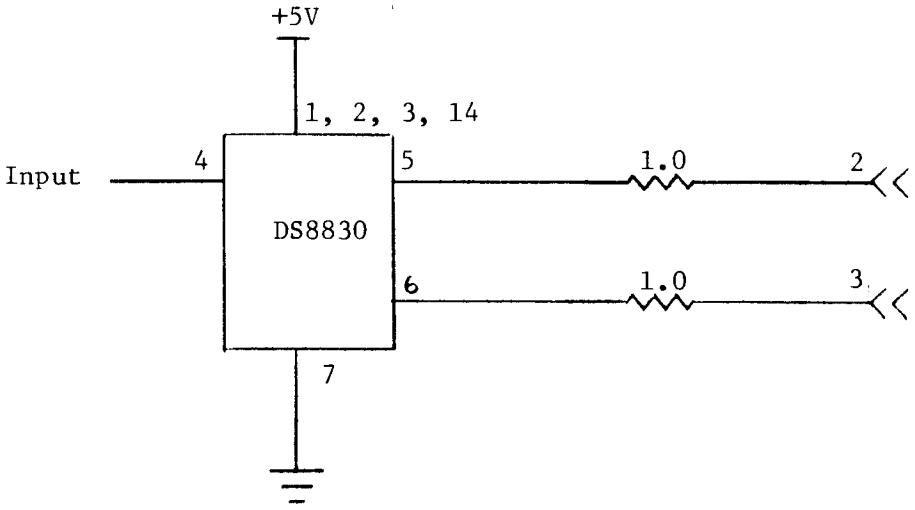
Typical Timing Parameters

Table 11.4



External Clock Input Circuit

Figure 11.5



Clock Output Circuit

Figure 11.6

Anomalies of the BiRa 910 Function Generator Module

Paul Sichta and John Wertenbaker
4/11/00

1) CAMAC Command #6 Load Address Pointer F(16).A(1).D(YYYYYY)
Prior to using the Load Address Pointer command (F16.A1), you must perform a STOP-ARM-STOP sequence (F24,F26,F24).

2) CAMAC Command #8 Set Samples/Channel F(16).A(2)
Do not use one sample/channel (data=0) with F16.A2. Minimum value should be 2 samples (data=1).

3) CAMAC Command #10 Start Scan F(25).A(0)
The trigger command F25.A0 does not always return Q, but X is always returned. The trigger action always occurs, even when Q is not returned.