CICADA ENGINEERING SPECIFICATION

DOCUMENT NO. TFTR-10C6-H911

DATE - 2/24/81

SUBJECT

Multi-Channel Latching Scaler

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DATE	DESCRIPTION

Multi-Channel Latching Scaler

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V 2.0

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1.0 Abstract

This document specifies a multi-channel latching scaler with memory interface.

2.0 Reference Documents

2.1 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Std. 583-1975.

2.2 Printed Circuit Board Fabrication and Assembly Specification, Document No. TFTR-10A2-H54B.

2.3 Electronic Schematic Specification, Document No. TFTR-10A2-H55.

2.4 Printed Circuit Artwork Specification, Document No. TFTR-10A2-H53A.

2.5 Reliability, Quality Control and Temperature Cycling. Document No. TFTR-10A2-H58.

2.6 Remote Memory Module, Document No. TFTR-10C6-H903.

3.0 Introduction

The CAMAC module defined by this specification will be used as an interface between elements of the Tokamak Fusion Test Reactor (TFTR) and the Central Instrumentation Control and Data Acquistion (CICADA) computer system. The subject module is a 32 channel latching scaler with memory interface. A suggested front-panel layout is given by Figure 1.

Figure 2 is the system block diagram of a typical input into one scaler channel, associated memory, and timing connections.

4.0 Performance Specifications

4.1 Scaler Signal Inputs

4.1.1 Each scaler input shall be optically isolated. The Hewlett-Packard HCPL-2601 optical coupler, or equivalent, shall be used as the input device.

The signal-input cable termination shall be as shown by Figure 2.

4.1.2 Each scaler shall respond to inputs which cover the frequency range from 1 Hz to at least 4×10^6 Hz. The minimum count pulse width will be 160 nanoseconds as shown by the worst case waveshape in figure 3.

4.1.3 The scaler signal input connector shall be the KINGS K-LOC 1904-1 or equivalent.

4.1.4 The signal shield connection shall be brought into the scaler through one of the connector pins. Provisions shall be made internally, close to the bulkhead connector, to optionally: (1) AC ground the pin using a 0.01μf, 100V ceramic capacitor, /RA or (2) not connect to ground. As delivered, the module will be supplied with option (1).

4.2 Count Enable

4.2.1 The externally generated (non CAMAC-dataway) count-enable (CE) signal is the "sample window" for all 32 scaler channels. CE shall have no effect unless the subject scaler is in the Armed Mode (see paragraph 4.5.2).

4.2.2 The CE signal source will have the following characteristics:

(a) Balanced differential signal

(b) Enable is active low (on non-inverting input)

(c) Active width of 50 μ sec or greater

(d) The interval between CE events will be greater than or equal to 1 μ sec (CE timing is given by figure 4).

4.2.3 The CE input receiver circuitry shall use a DS8820A line receiver or equivalent.

4.2.4 The CE signal shall enter the scaler module through a KINGS K-LOC 1904-1 type connector, or equivalent.

The CE output signal shall also be the KINGS K-LOC 1904-1.

The CE and signal connector pin assignment shall be:

Pin 1 Non-inverting input

Pin 2 Inverting input

Pin 3 Shield

Pin 4 Shield

Pin 1 of both CE connectors and Pin 2 of both CE connectors shall be wired together using twisted pair shielded cable as shown in Figure 2.

4.2.5 For large scaler arrays one CE source will drive a number of "daisy-chained" scaler modules. The last module in the chain will have its output connector externally terminated with a 120 ohm load resistor.

4.3 Scaler Counters

4.3.1 Each scaler "counter" shall have the capacity of 12 binary bits.

4.3.2 Each counter shall have the data format and overflow indication given below.

SCALER

	MSB											LSB
Zero Counts	0	0	0	0	0	0	0	0	0	0	0	0
4094 Counts	1	1	1	1	1	1	1	1	1	1	1	0
Overflow*	1	1	1	1	1	1	1	1	1	1	1	1

*All "ones" indicates count of 4095 or greater.

4.3.3 An internal circuit-board dip switch connection shall be provided to allow the scaler to reset from all "ones" to all zeros at input pulse 4096, and to count normally thereafter. The single overflow connection shall be common to all counters in the module. The overflow switch state shall be a component of the scaler status word. See paragraph 4.6.5.

4.4 Scaler/Memory Interface Requirements

4.4.1 External CAMAC-resident memory modules will be used in conjunction with this specified Scaler Module. See "Remote Memory Module", Reference 2.6. The Scaler Module shall accommodate the referenced memory modules to achieve parallel expandability to 32 modules (1 megaword by 12 bits wide). Logical adaptation to memory expansion shall be dip switch controlled. The memory expansion dip switch shall be contained on the Scaler Module and shall be a component of the Scaler Status Word. See paragraph 4.6.5. The memory available to each Scaler channel shall be determined by the number of active channels. See paragraph 4.5.2 and Table 1.

4.4.2 The Scaler Module shall interface to the Memory Module(s) by means of a thirty-six (36) pin rear edge card connector. Pin-outs and corresponding signal functions are given in Figure 5. Auxiliary memory bus-driving circuitry shall be implemented using TTL tri-state devices. The bus-drivers shall have the capability of driving as many as thirty-two auxiliary memory modules. The memory module will not load any interface point with more than one standard TTL load.

4.5 Scaler Operating Modes

The scaler module can be placed in one of three operating modes:

(a) Standby Mode

(b) Armed Mode

(c) Readback Mode

The three modes are described below.

4.5.1 Standby Mode

The module shall be in this mode when first powered-up, upon receipt of a CAMAC clear or initialize command and upon receiving the appropriate command (see paragraph 4.6.1). In this mode, the module shall ignore count inputs and will not accept a memory readback command. If a memory readback command is attempted when in standby mode a Q = 0 signal will be returned.

4.5.2 Armed Mode

In this mode, the module shall accept count inputs during the active count enable time. The module shall go into the armed mode when it receives the appropriate CAMAC command (see

paragraph 4.6.2). The Scaler Module shall always put the first count word from channel 1 into the first memory location. The first count word from channel 2 shall be placed into the second memory location and so on. The organization of count data in memory is shown in detail in Table 1.

When in this mode, and only this mode, count enable (CE) input pulses shall be counted by a 20 bit counter and saved for reading on the Dataway. See paragraph 4.6.6. The CE counter shall be cleared when the Scaler is in Standby Mode or when the Scaler is commanded to go into the Armed Mode. (paragraph 4.6.1 and 4.6.2). The CE counter shall be incremented on the low-to-high transition of the CE signal. (See Figure 4).

The Scaler shall ignore count inputs and the count enable input if the end of external memory is reached. If external memory is full, it shall not be allowed to "wrap around" and the count enable counter shall not be incremented. If the memory is full a bit shall be set in the status register (see paragraph 4.6.5). If the attached memory is not an integral multiple of the active channels the last memory segment will contain only a partial data set.

If memory readback is attempted while the Scaler is in this mode a value of Q = 0 shall be returned.

4.5.3 Readback Mode

In this mode, the Scaler Module shall allow data to be read back from the external memory modules on to the CAMAC Dataway. The Scaler module shall go into Readback mode when it receives the appropriate command (see paragraph 4.6.3). The data field of this command will contain the memory address of the first word to be read back and the memory address increment for subsequent words to be read back. The memory address of the first word read back can take on the values 0 to 1,048,576. See Table 1. After the first word is read back, the Scaler module shall automatically increment the memory address by a value from 1 to 256 as specified in paragraph 4.6.3. A value of Q = 0 shall be returned if an attempt is made to read beyond the end of memory (i.e., 32K for 1 external memory module, 64K for 2 external modules, etc.). It shall be possible to read the memory back at the standard Dataway rate. The Scaler shall ignore count inputs when in readback mode.

4.6 CAMAC Commands

4.6.1 Standby Mode F(24) • A(0) /RA

This command shall put the Scaler into Standby Mode. See paragraph 4.5.1. In this mode the count enable counter and the memory full bit in the status register (R4) shall be cleared. Q = 1 and X = 1 will be returned in response to this command. This command shall be accepted at any time.

4.6.2 Armed Mode F(26) • A(0) /RA

This command shall put the Scaler into the Armed Mode. See paragraph 4.5.2. This command shall clear the count enable counter and the memory full bit (R4) in the status register. Q = 1 and X = 1 shall be returned in response to this command. This command shall be accepted at any time.

4.6.3 Readback Mode F(17) • A(n) • Write Data Field

This command shall put the Scaler into the Readback Mode. See paragraph 4.5.3. Q = 1 and X = 1 shall be returned in response to this command. This command shall be accepted at any time.

The value of n in the subaddress A(n) shall set the memory readback increment as defined below:

n	Memory Increment
0	1
1	Number of active channels (1 to 32)
2	2 times the number of active channels (2 to 64)
3	3 times the number of active channels (3 to 96)
4	4 times the number of active channels (4 to 128)
5	5 times the number of active channels (5 to 160)

6	6 times the number of active chanels (6 to 192)
7	7 times the number of active channels (7 to 224)
8	8 times the number of active channels (8 to 256)

Values of n from 9 to 15 shall be ignored and treated like a value of n = 1.

The bits in the write data field are defined as:

W1 - W20 = Encoded memory address of first word to be read back, from 1 to 1,048,576 with the LSB on W1.

W21 - W24 = 0.

4.6.4 Readback Data F (0) • A(0) • Read Data Field

This command shall place the 12 bits of memory data at the current memory address on Dataway read lines R1 to R12 with the LSB on R1 and then increment the memory address by the value specified in paragraph 4.6.3.

The Scaler shall set bits R13 to R24 to 0. Q = 1 and X = 1 shall be returned in response to this command when the Scaler is in Readback Mode, except if the current memory address exceeds the memory address of the external memory modules, in which case Q = 0, X = 1 will be returned and bits R1 to R24 will be set to 0. Also, this command shall only be accepted when the Scaler is in Readback Mode; at any other time a

value of Q = 0, X = 1 shall be returned and bits R1 - R24 shall be set to 0.

4.6.5 Read Status

These commands shall put the contents of status register on to the Dataway read lines. Q = 1 and X = 1 shall be returned in response to these commands. These commands shall be accepted at any time.

4.6.5.1 General Status F(0) • A(2) • Read Data Field /RA

The bit assignments for the read data lines shall be as follows.

R2	R1	
0	0	Standby Mode
0	1	Armed Mode
1	0	Readback Mode

R3	
1	Counter can overflow
0	Counter cannot overflow

R4	
1	Memory full
0	Memory not full

R5 - R24 = 0

4.6.5.2 Memory F(0) • A(3) • Read Data Field

The bit assignments for the read data lines shall be as follows.

R1 - R5 = Encoded value of external 32k memory modules with LSB on R1.

R6 - R24 = 0.

4.6.5.3 Active Channels F(0) • A(4) • Read Data Field

The bit assignments for the read data lines shall be as follows:

R1 - R5 = Encoded number of active scaler channels with LSB on R1.

R6 - R24 = 0

4.6.6 Read Count Enable Counter F(0) • A(1) • Read Data Field /RA

This command shall put the contents of the count enable counter in binary format on to Dataway read lines R1 to R20 with the LSB on R1. Q = 1 and X = 1 shall be returned in response to this command. This command shall be accepted at any time.

4.6.7 Read Module Identification F(6) • A(0) • Read Data Field

This command puts the module I.D., decimal 911, binary 00000000000000111000111 1 on the Dataway read lines with the LSB on R1. Q = 1 and X = 1 shall be returned in response to this command. This command shall be accepted at any time.

4.6.8 Clear or Initialize C + Z

These Dataway signals shall be accepted at any time and shall put the Scaler into Standby Mode.

4.7 LED Indicators

The LED's defined below shall be visible from the Scaler front panel (see Figure 1):

4.7.1 A red LED (N) shall flash for 100 milliseconds (±20%) whenever the module is addressed.

4.7.2 A red LED (Q) shall flash for 100 milliseconds (±20%) whenever the module is addressed and Q=1 is returned.

4.7.3 A green LED (A) shall be lit when the module is in Armed Mode.

4.7.4 A green LED (R) shall be lit when the module is in Readback Mode.

4.7.5 A red LED (RB) shall be lit when the module is reading back data or for 100 milliseconds (±20%), whichever is greater.

4.7.6 Five green LED's (C) shall be lit to indicate the number of active channels.

4.7.7 Five green LED's (M) shall be lit to indicate the number of attached external memory modules.

4.8 Memory Increment

The memory increment sent to the Scaler depends on two factors: the desired method of reading data back and the number of active channels.

If it is desired to have contiguous words read back from the external memory represent the same event time in contiguous channels, then the memory increment sent to the Scaler will be 1. (The appropriate CAMAC set-up command is F(17) • A(0), see paragraph 4.6.3). When the data from the first event in

all active channels has been read the Scaler shall automatically continue with the data from the second event and so on.

If it is desired to have contiguous words read back from memory represent the data from a selected channel, then the memory increment sent to the Scaler will be a multiple of the number of active channels. For example, if the number of active channels is 24 and it is desired to read back every word from channel 3, then the starting memory address will be 3 and the increment of 24 corresponds to a CAMAC set-up command of F(17) • A(1). If every second word is to be read back from channel 3, then the starting memory 9, address will be 3 and the increment of 48 corresponds to a CAMAC set-up command of F(17) • A(2). In the channel readout mode, the Scaler shall increment by a value which takes into account the number of active channels and the subaddress A(n) in the F(17) A(n) command.

5.0 Mechanical Characteristics

5.1 This module shall conform to the mechanical requirements outlined in reference specification 2.1.

5.2 The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA type FR-4 or equivalent. See reference specification 2.2.

5.3 This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate. See reference

specification 2.1.

5.4 All components are to be identified with a standard manufacturer's part number or standard method of marking (e.g., resistor color coding).

5.5 All electrical components are to be mounted on only one side of the board. There shall be no hardwired connections between boards.

5.6 The condition of this module is to be monitored by LED's which can be viewed from the module front panel. See Figure 1 for the suggested front panel layout. The front panel shall be of aluminum and both sides are to have an iridite (conducting) finish. The color of the letters shall be chosen to contrast with the iridite finish and may be engraved or silk screened.

5.7 The 36 pin card edge connector shall mate with a Viking 3V18 connector (or equivalent). The card edge connector shall be marked with pin 1 on top and pin 18 on the bottom on each side of the card. It is not necessary to mark each pin.

5.8 All components are to be asigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part number on the electrical schematic associated with this module. See reference specification 2.3.

6.0 Electrical Characteristics

6.1 This module shall conform to the electrical requirements outlined in reference specifications 2.0.

6.2 Whenever possible, low power circuitry (such as the 74LS series) shall be used to minimize power dissipation.

6.3 The module shall derive its input power from the standard ±24 volt and ±6 volt CAMAC supply voltages.

6.4 The +6 and -6 volt supply voltages shall be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages shall be bypassed with electrolytic capacitors of at least 6.8 microfarads. In addition, at least half the integrated circuits shall contain a ceramic bypass capacitor of at least .01 microfarads on their supply voltage lines. The .01 microfarad capacitors should be located as close as possible to the integrated circuits and distributed equally across the board.

7.0 Environmental Data

7.1 The module shall operate as defined over an ambient temperature range of 0 to +50°C.

7.2 The module shall operate as defined over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module shall operate as defined in the presence of an external magnetic field changing at a maximum rate of 200 gauss per second with a peak magnitude of 100 gauss in any direction.

7.4 The module shall operate, as defined, in a radiation environment as follows:

Neutrons	2×10^7 n/CM^2/sec
Rad-dose	5×10^{-2} rad (Si)/sec
Integrated Dose	200 rad (Si)

8.0 Safety

All components of this module shall be of flame retardant material.

9.0 Testing

The module shall undergo all tests normally performed by the Seller. A description of the tests performed on this module and the results obtained shall be furnished by the Seller. Successful performance of the tests does not relieve the Seller of the responsibility of certifying that all requirements specified herein are met. The vendor shall provide a test procedure and, with PPL approval, it will be incorporated in this specification as paragraph 11.0.

10.0 Quality Control

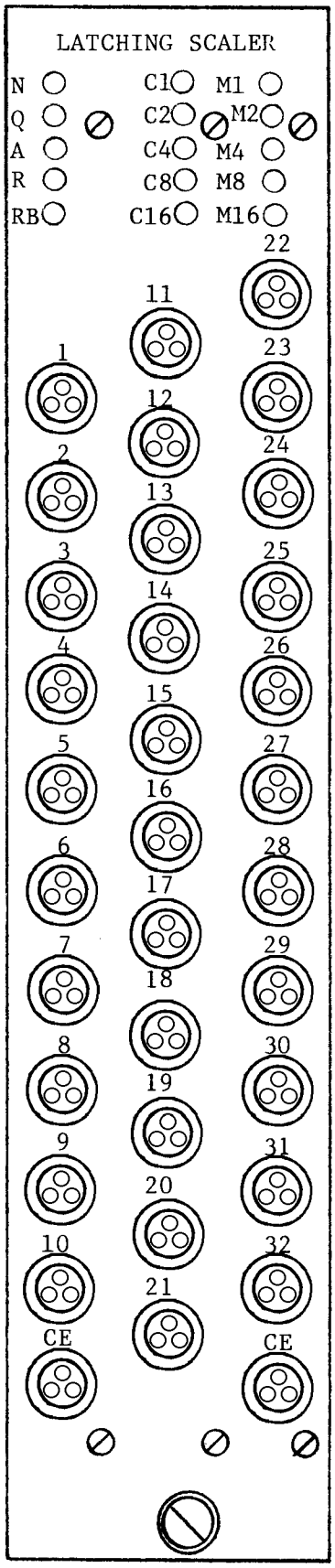
This equipment shall meet all applicable requirements specified in reference 2.5.

11.0 Test Procedure

Table 1

MEMORY ORGANIZATION

Physical Memory Address	Data From Count Enable Number	Data From Channel Number
0	1	1
1	1	2
2	1	3
3	1	4
.	.	.
.	.	.
.	.	.
Last Active Channel (L.A.C)-1		Last Active Channel (L.A.C.)
L.A.C.	2	1
L.A.C. + 1	2	2
L.A.C. + 2	2	3
.		
.		
.		
2 L.A.C. - 1	2	L.A.C.
2 L.A.C.	3	1
2 L.A.C. + 1	3	2
2 L.A.C. + 2	3	3
.		
.		
.		

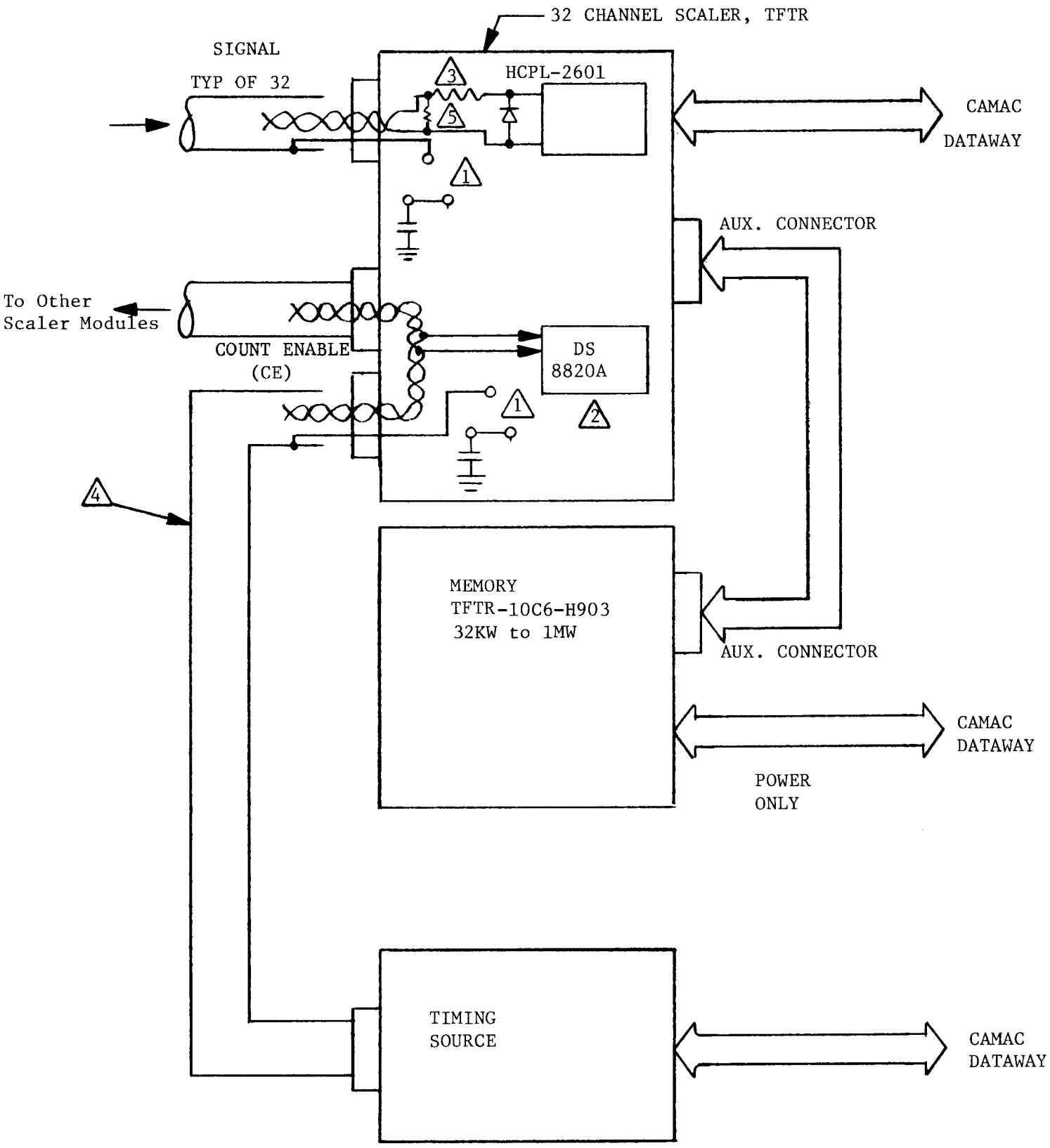


Suggested front panel layout

Figure 1

FIG. 2

System Block Diagram



NOTES

1. Optional shield grounding by jumper
2. Line terminations not used
3. Terminate HCPL with a 390 OHM +5% resistor as shown and Shunt Diode Schottky type HP-5082-2835
4. Cable type, Trompeter TWC-124-1A or equivalent
5. Vendor shall provide pads for ¼ W. Resistor

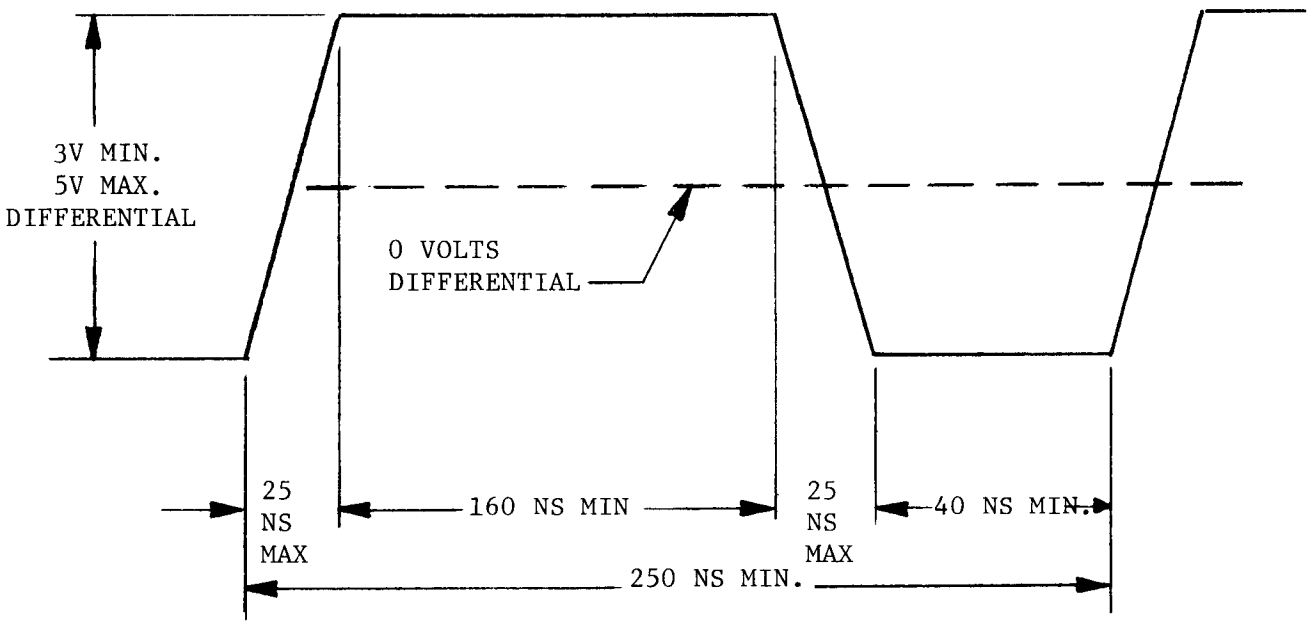


FIGURE 3

INPUT SIGNAL WAVESHAPE INTO TERMINATED LINE (SEE FIG. 2) FROM BALANCED DIFFERENTIAL LINE DRIVER

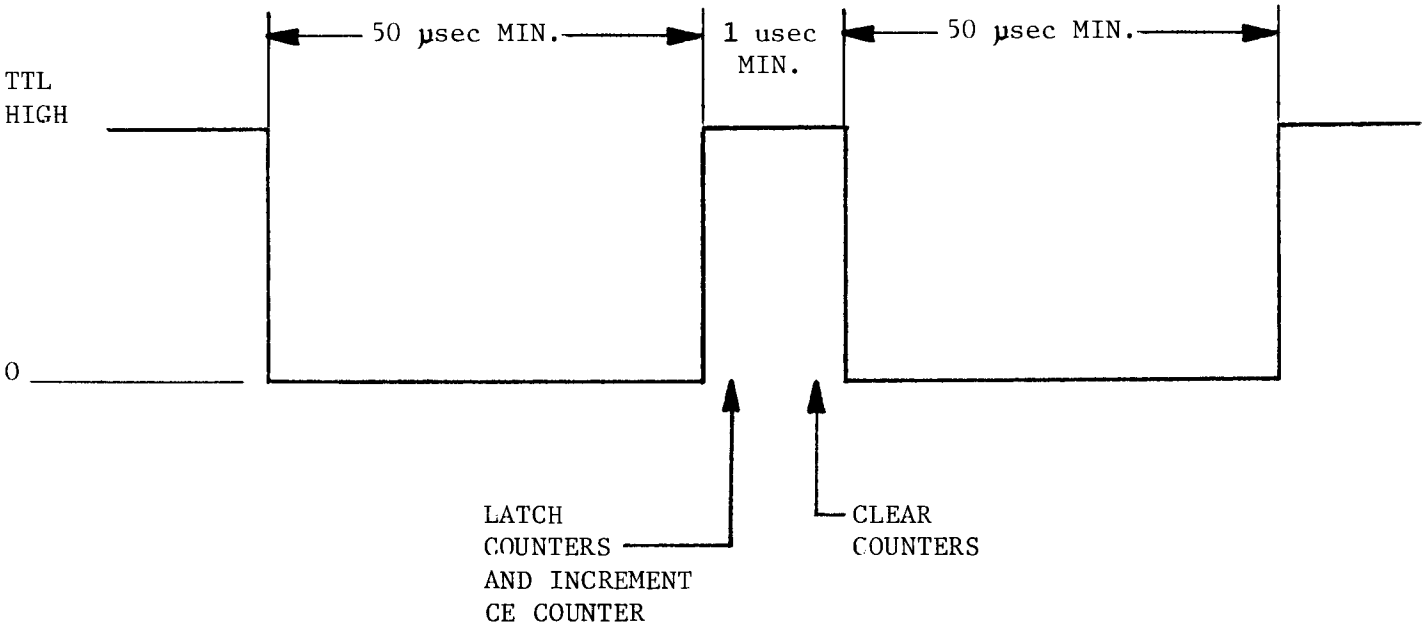


FIG. 4

COUNT ENABLE TIMING

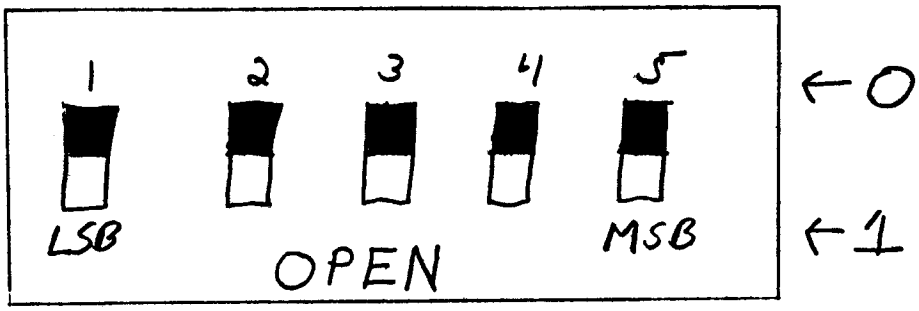
Figure 5 Auxiliary Connector Pin Assignments

Pin	Function	Pin	Function
1B	MAB 19	1A	MAB 1
2B	MAB 18	2A	MAB 0
3B	MAB 17	3A	GND
4B	MAB 16	4A	DB 11
5B	MAB 15	5A	DB 10
6B	MAB 14	6A	DB 9
7B	MAB 13	7A	DB 8
8B	MAB 12	8A	DB 7
9B	MAB 11	9A	DB 6
10B	MAB 10	10A	DB 5
11B	MAB 9	11A	DB 4
12B	MAB 8	12A	DB 3
13B	MAB 7	13A	DB 2
14B	MAB 6	14A	DB 1
15B	MAB 5	15A	DB 0
16B	MAB 4	16A	GND
17B	MAB 3	17A	Write Strobe
18B	MAB 2	18A	Read Strobe

MEM Modules (F0, A3)

SW2

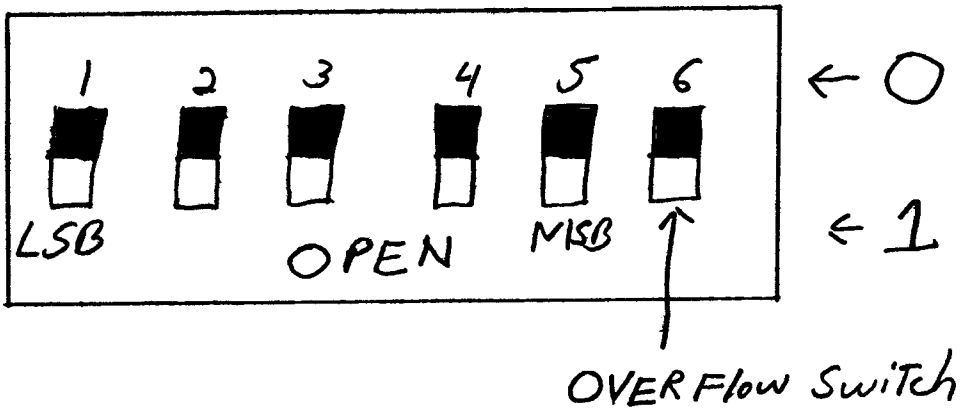
0-31 (IF)



Active channels (F0, A4)

SW1

0-31 (IF)



POST E_1 E_2 - Strapped Together, Terminates Clock Enable (CE) In ≈ 154 Ω Load

Posts E_3 E_4 - Strapped Together provide addition ground For shield on (CE)

Gating a 911 with a 412 using Mode 2

John Wertenbaker 9/11/2000

When a 911 Latching Scaler module is gated by a 412 Timing and Sequencing module, it was found that the first and last sample in the 911 need to be thrown away. The first sample needs to be thrown away because of the indeterminate time between arming of the 911 and the first trigger of the 412. The last sample needs to be thrown away because of the indeterminate time between last sample and the Readback Mode command.

There is a hardware fix for this problem. Switch the 412 to Mode 2. Invert the polarity of the Lemo cable that connects the Output of the 412 to the Count Enable input of the 911. (Connect pin 2 of the 412 output to pin 3 of the 911 input, and connect pin 3 of the 412 output to pin 2 of the 911 input.) Then program the 412 to output a high during the times the 911 should be counting data, and a low of at least 1 microsecond for each Count Enable pulse. Since the 412 starts and finishes its cycle with a low output, this will prevent the Scaler from counting input pulses before the first trigger and between the last Count Enable pulse and the Readback Mode command.

See Figure 7 below for details.

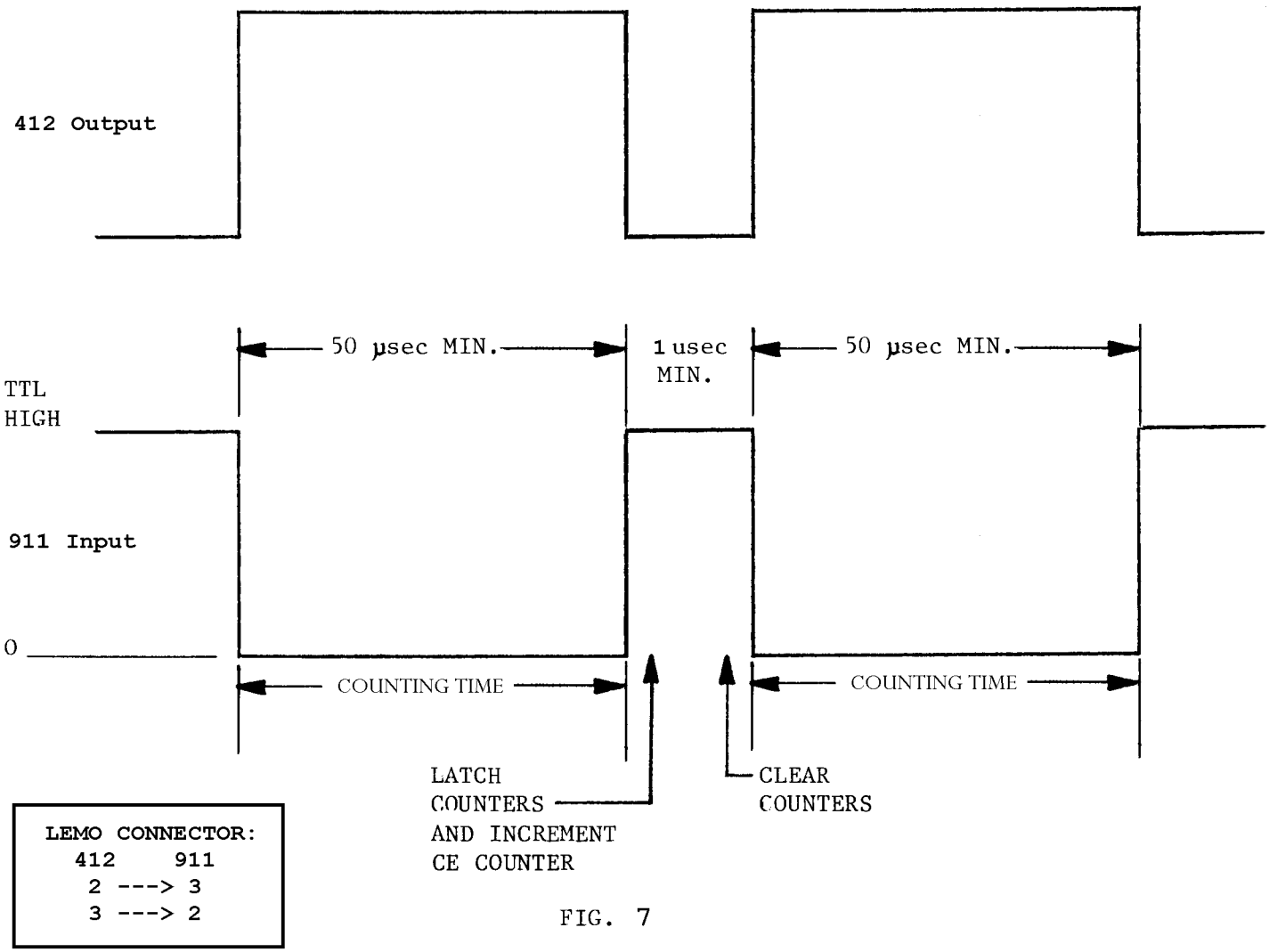


FIG. 7

COUNT ENABLE TIMING

Gating A 911 with a 412 using Mode 1 in Recycle Mode

John Wertenbaker 5/8/07

The Recycle Mode of a 412 presents special problems for a 911 Latching Scaler Module, unless certain conditions are met. Refer to the following example:

Address	Value	Should use
0	0	95
1	100	195
2	200	295
3	300	395
4	400	495
5	16,777,215	16,777,215

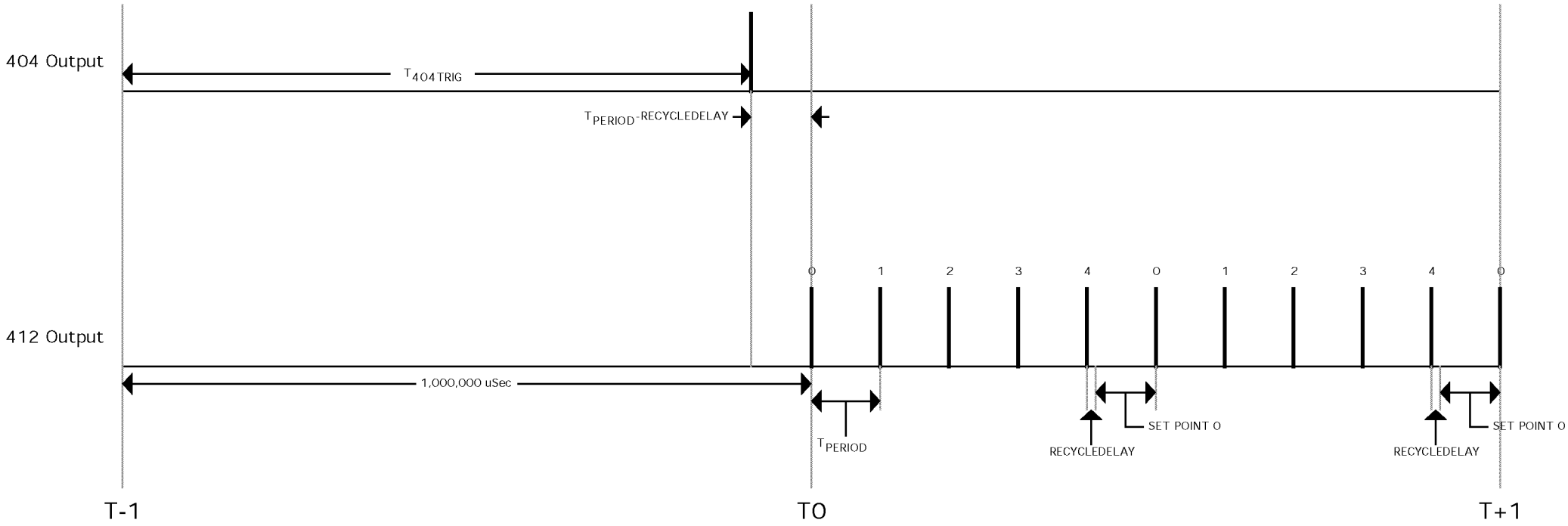
Let's assume that the recycle counter is set to 5, the 412 clock divider is set to 1, and the 412 is in Mode 1. The intent of this is to output 25 pulses, 100uSec apart. In reality, though, there will be a 5uSec interval between the pulse at address 4 and the next pulse at address 0. Not only does this introduce an inaccuracy in the timing, but it also causes missed CE pulses for the 911. The 911 requires an interval between CE pulses of at least 50uSec. If it is clocked any faster than that, it will ignore the second CE pulse. The "Should use" column provides 25 pulses, evenly spaced at 100uSec. In order to make the first sample happen at T=0, the 404 Timing Module could be triggered off of T-1, with a delay of 999,905uSec. This is 1,000,000 + recycle delay - T_{period}.

This example assumes that the user is already aware of the problem whereby the first and last samples need to be disregarded. That problem, and its solution, are detailed on another page. Please note that the same recycle problem also exists for Mode 2. If Mode 2 is to be used in clocking a 911 Scaler, the same technique mentioned on this page should be used. However, the example mentioned on this page won't work in Mode 2 because Mode 2 requires an even number of set points.

The following page is a graphic example of this, with formulas for programming both modules. The time period between pulses is different in order to make it fit on one page. The above example uses a period of 100uSec, while the diagram uses a period of 100,000uSec.

Gating a 911 with a 412 using Mode 1 in Recycle Mode

John Wertenbaker 5/8/07



(All times are in microseconds.)

$$T_{SETPOINT\ 0} = \frac{T_{PERIOD} - RECYCLEDELAY}{DIVIDER}$$

$$T_{SETPOINT\ 1} = \frac{T_{SETPOINT\ 0} + T_{PERIOD}}{DIVIDER}$$

$$T_{SETPOINT\ Last} = FFFFFF$$

$$T_{404TRIG} = 1{,}000{,}000 + RECYCLEDELAY - T_{PERIOD}$$

RECYCLEDELAY = 5us for 1us divider
20us for 10us divider
200us for 100us divider