Transient Digitizer Controller Module (Type 2)

1.0 Abstract

This specification in conjunction with referenced documents sets forth all characteristics of subject module. This specification shall take precedence where areas of overlap with referenced documents occur. The intended use of this document is to provide a minimum design goal for the module as well as a working document for subsequent users.

NOTE: Revisions from the previous issue of this document are identified by a vertical bar in the outer margin of the page.

2.0 Reference Documents

2.1 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Std. 583-1975

2.2 Printed Circuit Board and Assembly Specification, CICADA Handbook Volume I, TFTR-H54B

2.3 Electronic Schematic Specification, CICADA Handbook Volume I, TFTR-H55

2.4 Printed Circuit Artwork Specification, CICADA Handbook Volume I, TFTR-H53A

2.5 Reliability, Quality Control, and Temperature Cycling, CICADA Handbook Volume I, TFTR-H58

2.6 Standard Timing Pulse, CICADA Handbook Volume I, TFTR-H57

2.7 Facility Clock Subsystem, CICADA Handbook Volume I, TFTR-H401

2.8 Remote Memory Module, CICADA Handbook Volume I, TFTR-H903

2.9 Transient Digitizer Module, CICADA Handbook Volume I, TFTR-H907

3.0 Introduction

The CAMAC module specified will be used as part of the Central Instrumentation Control and Data Acquisition (CICADA) system. The initial use of the module shall be to facilitate data acquisition for the Tokamak Fusion Test Reactor (TFTR). The module shall be used to control high speed transient digitizers and their associated memory modules.

4.0 Basic Features

The module shall be a single width CAMAC module. The module shall interface to the CAMAC Dataway, to Transient Digitizers, and to Remote Memory modules. The Transient Digitizer Controller (Controller) module shall control the system memory address as well as initiate convert and unload sequences for all digitizers connected to it.

A digitizer system shall be made up of one controller module with up to fifteen (15) Digitizer modules. Each Digitizer module shall contain a high speed ADC system capable of a throughput of up to 500 KHz. In response to a "Convert" pulse signal, the Digitizer performs a 12 bit ADC, presents the data to its associated memory array, and then generates a write strobe. The Digitizer module shall not have control of the memory address bus. The Controller module shall control the address lines for all memory arrays attached to the system. All Digitizers will be equipped with a dedicated memory array with a dedicated data bus. All Digitizers, however, will share a common address bus. "Convert" pulses will be issued from the controller module, in parallel, to all the Digitizer modules in the system. All Digitizers will, therefore, write into the same absolute address location of their respective memory arrays at the same sample time. The function of the controller shall be to set up all addresses for both writing to and reading from system memories as well as to issue "Convert" and "Unload" pulses to system Digitizer modules. In addition, the Controller shall have a control line bussed to all Digitizer modules that will cause Digitizer modules to switch to self test input waveform.

The Controller module shall provide memory control and ADC "Convert" pulses to allow the recording of multiple transients. Prior to the start of a data acquisition sequence, the controller shall be set up for recording of 1, 2, 4, 8, or 16 such transients. Each transient shall be allocated to an equal number of memory locations (memory block). The starting and the sequencing of the Controller shall be accomplished through use of trigger pulses interfaced to the Controller through the front panel. The memory blocks may be set up for post- and pre-trigger recording with each block having the same number of post-/pre-trigger sample counts as all other blocks.

The Controller module shall have clock dividing circuits for establishing the digitizing rate for the system. The divider circuit shall use a clock signal on dataway line P2 for its source frequency. The clock dividers shall be set up by CAMAC command. In addition, the module may be configured to use a clock signal available from its panel in lieu of the P2 clock. This front panel clock input shall be used for applications that require clock synchronization between different Controller systems. When this external clock is selected, the internal dividers circuits shall not be available to the system.

The Controller module shall include circuitry to support a "self test" feature for a Controller/Digitizer system. In response to a CAMAC command, the module will cause the self test command line on its front panel command connector to go to its "true" state and impose a self test signal on the self test output pins of the command connector.

5.0 Mechanical Characteristics

5.1 The module will conform to mechanical specifications as indicated in Reference 2.1.

5.2 The module shall be a single width CAMAC module.

5.3 The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA Type FR-4 or equivalent. The circuit board shall be a two sided printed circuit board

with etched conductors. The fabrication of the circuit board shall be in compliance with Reference 2.2.

5.4 All components are to be identified with a standard manufacturer's part number or standard method of marking (e.g., resistor color coding) and shall have an exact replacement available from a second source manufacturer whenever possible.

5.5 This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate. (See Reference 2.1)

5.6 All electrical components are to be mounted on only one side of the board.

5.7 The condition of this module is to be monitored by LED's located on the module front panel. See Figure 11.1 for the suggested front panel layout. All lettering on the front panel shall be either engraved or silkscreened. The front panel material shall be aluminum with an iridite finish with contrasting colored lettering.

5.8 All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part number on the electronic schematic associated with this module. (See References 2.3 and 2.4)

5.9 The module shall have five (5) three pin LEMO connectors and one (1) twenty pin header connector mounted on the front panel. The front panel LEMO connectors shall be used for clock and trigger pulses in/out and the header connector shall be used for system control bus connections to Digitizer modules. The module shall use the rear 36 pin auxiliary connector for connections to the address and data bus for Digitizer and Auxiliary Memory Modules. The pin assignments for the connectors shall conform to Figures 11.2, 11.3, and 11.4.

The LEMO connector shall be a LEMO type RGOB303, CA22, or equal; the 20 pin header shall be a double row right angle header with locking hooks such as Robinson Nugent R221-ND; the 36 pin auxiliary connector shall be a standard card edge connector (0.1 inch centers).

6.0 Electrical Characteristics

6.1 Dataway Interface shall conform to specification as indicated in Reference 2.1.

6.2 Input Power shall be derived from the standard +/- 6 volt and +/- 24 volt CAMAC supply voltages. Whenever possible, low power circuit (such as the 74LS series) shall be used.

6.3 The +6 and -6 supply voltages must be bypassed on the module with electrolytic capacitors of at least 33 microfarads. The +24 and -24 volt supply voltages must be bypassed with electrolytic capacitors of at least 6.8 microfarads. In addition, at least half the integrated circuits must contain a ceramic bypass capacitor of at least .01 microfarads on their voltage lines. The .01 microfarad capacitors should be distributed on the

circuit board and be located as close as possible to noise sensitive components.

6.4 Address Control

6.4.1 Timing

The module shall be in control of the address lines for all Digitizer modules on its system. The timing for both loading and unloading memory is given by Figure 11.8.

6.4.2 Data Acquisition

During data acquisition, the Controller module shall provide timing control as well as address control for all Digitizer modules. All Digitizer modules will, therefore, be connected to the same address lines and to the same "Convert" signal line. All Digitizer modules must be equipped with the same amount of private memory. Essentially, the Controller module issues a "Convert" pulse and then posts the address for the sample to be acquired to all Digitizers on the system bus. A block diagram is given by Figure 11.9.

Prior to a digitizing sequence the Controller module must be set up and then armed. The set up commands shall be used by the Controller to determine the digitizing sequence.

6.4.3 Memory Blocks

The system memories may be divided into a number of equally sized blocks. The blocks shall be used for recording multiple transient events. Prior to a digitizing sequence, a CAMAC "set up" command shall be used to cause the memory to be divided into 1, 2, 4, 8, or 16 blocks (partitions). The module shall use the trigger input signal to initiate advance from block to block. The block size shall be a function of the amount of memory the system is equipped with. All available memory shall be used.

6.4.4 Memory Address Size

The Controller module shall be capable of utilizing up to a total of 128K words of memory for each channel. All channels must be equipped with an equal amount of memory.

Allowed memory sizes shall be 8K, 32K, 64K, or 128K words. Switch assemblies mounted on the module printed circuit board shall be used by the module circuitry to ascertain the amount of memory present. The status of the switch settings shall be available for read out by CAMAC command.

6.4.5 Address Sequence

The Controller module shall be set up to operate in either post-trigger or pre-trigger mode. When in the post-trigger mode, all the data acquired for each commanded block shall be data acquired after receipt

of trigger. When in the pre-trigger mode, data acquired for each commanded block may contain both pre-trigger and post-trigger data.

6.4.5.1 Post-Trigger Mode

After being set up in the post-trigger mode and after being armed by CAMAC command, the system shall not commence acquisition of data (loading of memory) until such time as a trigger input signal is received. Upon receipt of the first trigger signal, the module will commence data acquisition. The Controller module will control the memory address and the "Convert" pulse command so that the first memory block may be filled with data acquired after the trigger. Upon filling the first block with data, the controller will cease data acquisition and await a second trigger which will then result in the acquisition of the second block of data in a similar fashion. The controller will move from block to block until the last memory block is filled with data or until the sequence is terminated by CAMAC command. At the end of the sequence (blocks complete or CAMAC terminate), an internal "end of record" (EOR) flag shall be set. After the EOR flag is set, the module will not respond to any subsequent trigger signals until it is again armed by CAMAC command.

6.4.5.2 Pre-Trigger Mode

When the module is configured for pre-trigger mode, system memory blocks may be configured to contain both pre-trigger and post-trigger sample data. The quantity of post-trigger samples is loaded by CAMAC command prior to issuing its CAMAC "Arm" command. The number of post-trigger samples may be set up to be any integer value from 0 to 131,071 (1FFFF Hex). The number of pre-trigger samples for each block is, therefore, the block size minus the post-trigger sample count loaded by CAMAC command. The number of post-trigger samples loaded may exceed the block size, which will cause all the data to be post-trigger data and delayed in time from the trigger signal. When the number of post-trigger samples exceeds the block size, the system will continue writing (round-robin) within the block until the required number of samples have been acquired. The number of samples available shall, therefore, be limited to the block size.

When the Controller is "Armed" and is set up in pre-trigger mode, the module will immediately commence issuing "convert" pulses and begin writing data into the first memory block of its system memories. The system will continue to write into the first block in a "round robin" fashion until such time as a trigger signal is received. Upon receipt of a trigger signal, the module shall commence a count of post-trigger samples which may be any integer from 0 to 131,071. After satisfying the required number of post-trigger samples, the module will then advance to the next memory block and commence loading data into the next block a similar fashion. Each memory block shall be

configured with the same quantity of post-trigger samples and shall require that a trigger signal be received in order to commence post-trigger sample count. As trigger signals are received and post-trigger sample counts are satisfied, the controller will advance from block to block until the last memory block is satisfied or until the sequence is terminated by CAMAC command. The EOR flag shall be set at the end of the sequence in the same way as it is during post-trigger operation.

6.5 Clock Selection and Source

The module shall be capable of using an internally derived clock signal or an externally supplied clock signal for the source of its "convert" pulse command. The selection of internal or external clock source shall be accomplished through a CAMAC command. The current clock selection shall be readable by CAMAC command.

When the module is set for internal clock, the clock signal will be derived from a 1MHz clock signal available on Dataway line P2. The "P2" clock shall be a TTL level signal with a nominal duty cycle of 60/40. When the P2 clock is used, the modules internal clock dividers shall be available. The divider circuit shall use the high to low transition of the P2 clock signal as its active edge.

When the external clock source is selected, the "convert" output pulse shall be synchronized to the clock signal available through the front panel "CLK IN" LEMO connector. The "convert" pulse shall be a gated pulse that shall be triggered by the leading edge (low to high) of the clock input signal. When the external clock is selected, the internal clock divider circuits shall not be available.

Clock dividers shall allow the following convert frequencies:

DIVIDER NUMBER	NOMINAL FREQUENCY
0	500 KHz
1	200 KHz
2	100 KHz
3	50 KHz
4	20 KHz
5	10 KHz
6	5 KHz
7	2 KHz
8	1 KHz
9	500 Hz
10	200 Hz

6.6 Module Triggering

The module may be triggered from either a front panel LEMO connector or from a decoded CAMAC command. Incoming trigger signals will be typically asynchronous with the module sample clock, therefore, the module shall provide circuitry to establish predictable time relationships between the data acquisition clock and incoming trigger signals. In cases where

multiple Controller modules are to be used in a system requiring simultaneity of sampling between systems, one of the Controllers (master) will be used to establish the timing for all other (slave) Controllers.

Typically, the master Controller will be configured to use its internal clock and be interfaced to the external (asynchronous) trigger signal. Other Controllers will be configured for external clock utilization and have their external clock input and trigger input connected to the respective outputs of the master unit. The selection between master and slave operation will be made by CAMAC command.

6.6.1 Trigger/Clock Timing Post-Trigger Mode

When the module is configured for internal clock and used in the post-trigger mode, the module will synchronize its internal clock as well as its clock output signal to the sensed trigger signal input. This capability shall be implemented by clearing the module clock divider circuits such that the time of the first acquisition of data as well as the first clock output (active edge) shall occur on clock period (selected clock) after the receipt of the trigger signal. The trigger output signal, however, shall be designed to occur within 50 nonoseconds (50 x 10 -9 sec) of the sensed trigger input. The time relationship for the trigger and clock for post-trigger mode is given by Figure 11.5.

When the module is configured for external clock and used in post-trigger mode, the synchronization of the module clock shall not be available since the clock divider circuit is not used. The acquisition of the first data word will, therefore, be timed to the first input clock following the sensed trigger input signal. The synchronization circuit of the master digitizer controller will normally be used to ensure some delay between the trigger pulse and the first clock signal. This delay (2 microseconds minimum) will insure that all slaved digitizers will start acquiring data with the same clock signal.

6.6.2 Trigger/Clock Timing Pre-Trigger Mode

The module will use the incoming trigger pulses to start its count of post-trigger samples. A potential problem that will occur with multiple digitizers responding to the same asynchronous clock and trigger signals will be the simultaneity of acquisition of the post-trigger samples when the trigger and clock signals (active edges) are sensed at the "same" time. This problem will be addressed by using one (master) providing trigger outputs for slave controller trigger inputs. The trigger output of the master controller will be a signal delayed from the sensed input trigger to insure that down stream digitizers will start their post-trigger sample count with the same clock edge as does the master controller. This feature shall be implemented by the module circuitry establishing a trigger output permissive "window" that shall fall between clock signal edges. This circuit shall insure sufficient time between its trigger output and the first clock output that follows to insure simultaneity of the start of post-trigger sample count for all controller modules using

this clock and trigger output. All modules will be equipped with the circuitry to accomplish this "delay trigger" feature. This circuit, however, may be disabled through a CAMAC command. The status of the "delay trigger" feature shall be readable by CAMAC command.

When the "delay trigger" circuit is disabled, the trigger output signal shall be a buffered equivalent to the trigger input signal with minimum delay. The required time relationships between the input and output signals for this configuration is given by Figure 11.6.

6.6.3 Extraneous or Untimely Triggers

Because of the experimental environment in which the subject module is to be used, some trigger pulses may occur at unanticipated times. The module will respond to these triggers as follows:

6.6.3.1 Post-Trigger Mode

If extra pulses are received while the module is controlling digitizing of a given block, the first such extra trigger shall be stored by the module. This second trigger will effect the module in the same way as if this second trigger were received just as the module entered the next block. Third and subsequent triggers will have no effect on the module. As an example, if the module were configured in post-trigger mode and two or more trigger pulses were received before the first block is complete, then the first two blocks will be written consecutively. There will, however, be up to two microseconds of time discontinuity between blocks to allow the module time to reset its internal counters and to store the block pointer.

6.6.3.2 Pre-Trigger Mode

If a trigger signal is received by the module before the module has completed a sufficient number of pre-trigger samples, the module will continue loading that block with post-trigger samples until the entire block is loaded with new data. The user must use the module output "EOB" pulse together with an external time logging device to ascertain the occurrence of early trigger signals.

The second potential trigger problem for pre-trigger mode is the occurrence of multiple triggers within a given block. The module will respond to these extra triggers in this mode as it does in the post-trigger mode. The second trigger received will be stored and will effect the module in the same way as if this second trigger were received just as the module entered the next block. Third and subsequent triggers will be ignored. As an example, if the module were configured for pre-trigger mode and received a second (or more) trigger(s) before completing its post-trigger sample count, it will complete its current block and then advance to the next block. Upon entering the next

block, the module shall clear the trigger flag set during the last block and immediately start a count of its post-trigger samples. As stated above, the module will always, as a minimum, fill this block with new data before advancing to the next block. If the number of post-trigger samples requested exceeds the block size, the controller will continue incrementing memory address in a round robin fashion until the requested number of post-trigger samples have been acquired before a block advance. If while loading this second block a trigger signal is received, then this trigger will not effect this (second) block but it will cause the next (third) block to behave as if it were triggered immediately upon starting in the same way as did block number two.

6.7 Memory Unloading

Memory unloading shall be accomplished through a series of CAMAC commands to the Controller Module. In order to allow memory unloading to the CAMAC Dataway, an intermediate queuing of data must be maintained within the system Digitizer modules.

Unloading shall be accomplished by first placing the system into the unload mode and subsequently issuing read memory data commands. The command initiating the unload mode (Enable Unload) shall provide a data field indicating the channel number, the desired block number, and the relative starting point for the requested data. The relative starting point (offset) shall be an integer that the module will add to the oldest available data for the requested block.

In response to receipt of the CAMAC "Enable Unload" command, the module will post the address of the requested data on the system address bus and the address of the requested channel onto the system control (front panel) bus. The Digitizer module that recognizes its address on the control bus will then queue up the corresponding data word for subsequent transfer onto the Dataway. The memory unload commands that follow shall cause the Controller to issue an "Unload" pulse to its control bus and then cause the address bus data to be updated. The Unload pulse imposed on the command bus shall be equivalent to the decoded CAMAC command N.F(2) as received by the Controller. The addressed digitizer shall have the next data word loaded into a Dataway queuing register ready for the Dataway cycle. The address of the next word will be a function of the subaddress (A) of the previous unload command. Increments of 1, 2, 4, 8, or 16 will be accommodated such that the user may choose or read every N'th word (N=1, 2, 4, 8, or 16) if a gross waveform is desired.

It should be noted that the base address to which the initial offset is added must be the oldest available data for the requested block. The address of this data is simply one (1) greater than the address of the last word loaded within the block. The determination of the address of the oldest available data shall be accomplished within the module hardware and shall be "transparent" to the user. The address update shall occur after the Dataway cycle is complete as shown by Figure 11.8.

After the module has been configured in the unload mode, the addressed

Digitizer module (channel) shall load the first requested data word into an internal register that may be subsequently unloaded to the CAMAC Dataway. As unload commands are received, the Controller module shall increment its memory address through data contained within the commanded block. When data for a specific block is exhausted, the module shall advance to the next block and start with the oldest available memory data from the next block. The intended use of this feature is to support complete memory readout. In the case where complete memory is desired, the unload mode command shall request the oldest word from the first block. Unload commands that follow will, thus, continue until all available blocks are unloaded from the requested channel (Digitizer Module).

Three potential problems that may be encountered when the unload mode is exercised are the use of excessive offset (offset greater than block length), unloading from block to block with increments other than one (1), and read requests beyond the last valid block (last block loaded during the previous sequence).

In the case where the commanded offset exceeds the block length, then the first word unloaded shall be the oldest available data for the next block.

In the case of consecutive "read data" commands that cause a transfer from one block to the next block, the first word read from the next block will always be the oldest available data (OAD) from that block. This feature will be operational for all read out increments. In the hypothetical case where every sixteenth word is being read out, using the internal 3K memory, with a block size of 512 (16 blocks active), then the word read out will be as follows:

READ DATA COMMAND #	WORD #	BLOCK #
1	1(OAD)	1
2	17	1
3	33	1
4	49	1
.	.	
.	.	
.	.	
32	497	1
33	1(OAD)	2
34	17	2
35	33	2
36	49	2

In the case where an unload request is made to a memory area that either is non-existent or is an area not overwritten during the last sequence, then the module will return a data field of all zeros along with CAMAC Q of zero. Such requests for invalid data may be caused by excessive offset when requesting data from the last block or by issuance of read commands beyond the last "digitized block". A digitized block is one that had been completed and had caused an issuance of End of Block (EOB) pulse.

6.8 Memory Interface

The module shall interface to external memory modules through use of the thirty-six (36) pin rear auxiliary connector. Signals on the memory connector shall be implemented through use of tristate TTL level devices. The output signals shall utilize "Bus Drivers" to allow the use of as many as four (4) auxiliary memory modules (see Reference 2.8). The data convention shall be high-true with timing compatible with companion memory modules (see Reference 2.8).

6.9 External Clock Input

The module shall interface to an external clock signal through use of the three (3) pin front panel connector. The clock input circuit shall utilize a high impedance differential line receiver, such as an AM26LS32AC or equivalent (12K OHM input impedance) with pads for a 1/4 watt terminating resistor as shown in Figure 11.7. The module shall use the low to high transition on pin 2 (see Figure 11.2) as the active edge.

6.10 Clock Output

The module shall provide a clock output signal that shall be interfaced through a front panel connector and shall be a differential output compatible with the external clock input. The clock output shall be synchronized with the convert output signal (either internally or externally sourced) and shall be nominally a square wave (maximum asymmetry 70/30) with the low to high transition being the active edge. This output shall be a buffered equivalent to the internal convert signal. This output shall be capable of driving a 100 ohm resistive load to +5V +0, -1V (line to line) with a maximum rise time of 50 nanosecond. This clock output shall be present whenever the system is actively acquiring data.

As stated in Section 6.6.1, this output shall be synchronized to the incoming trigger signal (as is the "Convert" clock) whenever the module is triggered to start a block in the post-trigger mode. Examples of the time relationship between the clock output and asynchronous trigger input signals is given in Figure 11.5. When the module is operating in the pre-trigger mode, this signal shall not be affected by trigger inputs.

6.11 Synchronization of Multi-Controller Configurations

The clock and trigger input/output signals may be used to synchronize several controller/digitizer systems. For such applications, one of the controllers shall be set up as a "master" controller. The master controller will be used to provide trigger and clock signals for all slave controllers.

Slave controllers shall be set up for the use of the external clock input. Clock and trigger inputs for slave controllers shall originate from the master controller. Connections between slave controllers and the master controller may be accomplished in either a parallel or serial mode.

In order that slave controllers may be configured with reasonable simultaneity between the "convert" output pulses, a multi-tapped delay line shall be used. A diagram of the delay line utilization is provided in FIgure 11.10.

6.11.1 Parallel Mode Configuration

This configuration is suitable for applications in which the various slave controllers are located in close proximity to each other (i.e., less than 10 feet apart). The clock and trigger outputs of the master controller shall be connected to the clock and trigger inputs of the various slave controllers. Connection between modules may be accomplished through use of "T" type connectors or through use of fanout type cable assemblies.

The terminating resistor for the clock and trigger input circuit should be either installed on only one of the slave controllers, or be installed as part of the interconnecting cable assembly.

Propagation differences between modules will cause a time shift of the various output "convert" signals as referenced from the "convert" signal of the master controller. Calibration of the delay lines for the various slave controllers and the master controller shall be set for best fit synchronization, with the "worst case" slave controller. Ideally, all slave controllers will be set for minimum delay and the master controller will be set for sufficient delay to compensate for cable delay and for line receiver and gate delays of the slave units.

6.11.2 Serial Mode Configuration

This configuration is suitable for applications in which the various slave controllers are located at distances greater than 10 feet apart. The clock and trigger outputs of the Master controller shall be connected to one of the slave controllers, which in turn shall be connected to the next controller through use of the slave controller's clock and trigger outputs. The serial configuration allows each controller to be equipped with impedance matching resistors which will minimize line reflections caused by impedance mismatches. Propagation delays between the various slave controllers are additive for this configuration, requiring that each controller have its delay tap set individually. All controllers must be set up for sufficient delay for synchronization with the last (worst case) slave controller on the link.

It should be noted that the trigger input/output system does not employ a settable delay feature. If more than three (3) slave controllers are used in this mode, then the trigger time displacement feature as delineated in Section 6.6.2 may be defeated.

6.11.3 Delay Parameters

CLK IN/CLK OUT: 100ns +/- 20ns

DELAY LINE: 50ns/tap, +/- 2ns +/- 5 percent of delay

6.12 Trigger Input

The module shall receive event trigger pulses through use of the front panel LEMO connector. The event trigger input shall utilize an opto-isolator

circuit, such as an HCPL-2601 or equivalent. The module shall use the low to high transition on pin 2 of the LEMO as the active edge. The trigger input shall be compatible with a "TFTR standard timing pulse" as defined in Reference 2.6.

6.13 Trigger Output

The module shall provide a trigger output signal that may be used for time tagging or for triggering other controllers. This output shall be a differential pulse signal capable of driving a 100 ohm resistive load to +5V +0, -1V with a maximum rise time of 50 nanoseconds. The output pulse width shall be 1.0 microseconds +/- 10% (measured at the 2 volt level).

The trigger output port may be a configured function in one of two ways through use of the "delay trigger" selection. When the "delay trigger" feature is disabled, the trigger output port will pulse in response to all trigger input signals (pulse or Dataway) and shall have a maximum delay of 100 nanoseconds from the source input trigger.

When the "delay trigger" feature is enabled, the trigger output signal shall be used to signify an internal trigger signal that was "used" by the module. Trigger signals received that are not immediately acted upon, such as stored trigger signals or trigger signals that are ignored by the module, will not result in trigger output pulses. Trigger output pulses for modules configured with trigger delay enabled will be generated under the following conditions:

(1) The module is in post-trigger mode and is about to start acquiring a new block of data. When the internal clock is used, this trigger output will precede the following clock signal by a minimum of 2 microseconds.

(2) The module is in pre-trigger mode and is about to start a count of post-trigger samples. This trigger output will be displaced in time to occur between clock output pulse edges.

(3) All other trigger input signals that may be sensed by the module will not result in trigger output signals. Examples of time relationships between the trigger output and trigger input is given in Figure 11.6.

6.14 End of Block Output

The module shall provide a pulse output to be used to signify the end of each digitized block. This pulse shall have the same electrical characteristics as the trigger output and shall normally be used to trigger an external time recording device. The pulse shall occur within 1 microsecond of the conversion of the last valid data sample for each block.

6.15 Memory Partitioning

The memory may be partitioned into 1, 2, 4, 8, or 16 partitions or blocks. The block size (number of data words per block) for an 8K configuration is as follows:

NUMBER OF BLOCKS	BLOCK SIZE
1	8192
2	4096
4	2048
8	1024
16	512

Memory configuration of 32K, 64K, or 128K shall cause the block sizes to increase by a factor of 4, 8, or 16, respectively.

6.16 Self Test Capability

The Controller/Digitizer system shall have a self test feature. The CAMAC command to initiate the self test shall be sent to the Controller Module. In response to this command, the controller module shall set its self test command line to the true (low) state and impose an analog signal upon the self test output pins. Digitizer modules connected to the Control Command bus will respond to the self test command by switching their respective analog input port to the self test input pins of the command bus.

The analog signal that shall be provided by the Controller shall be a periodic monotonically increasing and decreasing signal varying from -5 volts (+ or - 100 millivolts) to +5 volts (+ or - 100 millivolts). This output shall be capable of driving a 50 ohm load to specified voltage and shall be capable of withstanding a line-to-line or line-to-ground short indefinitely without sustaining damage.

The frequency of this output shall be settable through use of board monitored switches to be 200Hz, 2KHz, 20KHz, or 200KHz. The position of these switches may be ascertained through the use of the "Read Status" CAMAC command.

6.17 CAMAC Commands

The module shall accept commands from the CAMAC dataway in compliance with Reference 2.1.

6.17.1 Command #1 Read Status 1 [F(0).A(0).(Data Returned)]

This command gates the module Status Register 1 onto the dataway read lines. The data returned shall be interpreted as follows:

Bits R1-R3 Operating Mode
- 0 = Unload Mode
- 1 = Post-Trigger Mode
- 2 = Pre-Trigger Mode
- 3 = Not used

Bits R4-R5 Operating State
- 0 = Digitizing Sequence Complete
- 1 = Armed (not triggered)
- 2 = Armed and Triggered (digitizing in progress)

3 = Not used

Bits R6-R7 Available Memory
0 = 8K
1 = 32K
2 = 64K
3 = 128K

Bits R8-R10 Not Used

Bits R11-R13 Number of Memory Blocks
0 = 1 Block
1 = 2 Blocks
2 = 4 Blocks
3 = 8 Blocks
4 = 16 Blocks
5-7 = 16 Blocks

Bit R14 Undefined

Bits R15-R18 Clock Selected
0 = 500 KHz
1 = 200 KHz
2 = 100 KHz
3 = 50 KHz
4 = 20 KHz
5 = 10 KHz
6 = 5 KHz
7 = 2 KHz
8 = 1 KHz
9 = 500 Hz
10 = 200 Hz
11 = Not allowed
12-15 = External Clock

Bit R19
1 = External Clock Selected
0 = Internal CLock Selected

Bit 20
0 = Trigger Delay Disabled
1 = Trigger Delay Enabled

Bits R21-R22 Self Test Signal
0 = 20Hz Self Test Selected
1 = 200Hz Self Test Selected
2 = 2KHz Self test Selected
3 = 20KHz Self Test Selected

Bits R23-R24 Always Zero

The module will respond to this command and return Q=1 and X=1 during all modes of operation. It should be noted that when the external

clock is selected through use of on board jumpers, bit R18 will be set and bits R15-R17 have no significance.

6.17.2 Command #2 Read Post-Trigger Sample Count [F(0).A(1).(Data Returned)]

This command gates the contents of the post-trigger sample count register onto the CAMAC read lines R1 through R17 (R18-R24 always zero). The quantity returned (pre-set by command F(16).A(1) represents the number of post-trigger samples commanded for each block.

The module will respond to this command and return Q=1 and X=1 during all modes of operation.

6.17.3 Command #3 Read Status 2 [F(0).A(2).(Data Returned)]

This command gates the contents of the Status Register 2 onto the Dataway read lines R1 through R17 (R18-R24 always zero). Bits R1 through R16 shall correspond to memory block 1 through memory block 16. A logical one ("1") for a given bit will indicate that the corresponding block was used during the last digitizing sequence (the entire block contains new data). A logical zero ("0") will be returned if either the block was not commanded to be used during the last sequence or, if the block was commanded to be used, was not fully utilized (module stopped by CAMAC command before EOB or not triggered during last sequence). Bit R17 shall be used to indicate whether the digitizing sequence is still in progress or whether the module internal end of record flag is set. A logic one ("1") will, thus, indicate that the sequence is complete and a logic zero ("0") will indicate that the digitizing sequence is still in progress.

The module design shall clear (set to all zeros) this register upon receipt of an ARM command. Individual bits of this register will then be set by the module as the appropriate condition occurs.

The module will respond to this command and return Q=1 and X=1 during all modes of operation.

6.17.4 Command #4 Read Memory Buffer [F(2).A(x).(Data Returned)]

This command causes the module to issue an "Unload" pulse to its front panel "command" bus which in turn shall cause the Digitizer module addressed (set up by Enable unload) to impose its memory data onto the Dataway. After completing the Dataway cycle, the module will increment its internal memory address register by a sufficient quantity to obtain the next desired word for the block unloading. The absolute increment shall be determined by the module circuitry dependent upon the subaddress A(x) of the unload command. The intent of this command is to read every xth word for a given channel. Subaddress values of 0, 1, 2, 3, and 4 are supported and correspond to increments of 1, 2, 4, 8, and 16 respectively. The data transfer to the Dataway read lines shall be right justified with the sign extended to sixteen (16) bits (R17 to R24 always zero). The module will respond to this command only after the module has successfully been put into the data unload mode by CAMAC Command #8. Attempts to read the memory buffer prior to setting up the

unload will result in a CAMAC response of Q=0, X=1, and a CAMAC data return of all zeros. Successful use of this command will result in Q=1 and X=1 being returned.

As delineated by Section 6.7, this command that causes the module address bus to increment within a given block, until the end of the block is reached or until the requested increment would be beyond the last word of the block. When either of these instances occur, the address will then advance to the next block, and start with the oldest available data from that block. Thus, the entire memory may be unloaded if desired, with only one "Enable Unload" command.

6.17.5 Command #5 Read Module Number [F(6).A(0)]

This command gates the module identification number (decimal 912, hexadecimal 390) onto the Dataway read lines R1 through R12 (R13-R24 always zero). The module will respond to this command and return Q=1 and X=1 during all modes of operation.

6.17.6 Command #6 Set Up Module [F(16).A(0).D(YYYYYY H)]

This command sets up the digitizing mode of operation and is required to be issued prior to any digitizing sequence. The command clears the End of Record (EOR) flag if set and sets the module memory address pointer to location zero. This command makes use of the CAMAC data field W1 through W24 as follows:

Bit W1 Set Operating Mode
0 = Post-Trigger Mode
1 = Pre-Trigger Mode

Bits W2-W5 Set Digitizing Clock
0 = 500 KHz
1 = 200 KHz
2 = 100 KHz
3 = 50 KHz
4 = 20 KHz
5 = 10 KHz
6 = 5 KHz
7 = 2 KHz
8 = 1 KHz
9 = 500 Hz
10 = 200 Hz
11 = Not allowed
12-15 = External Clock

Bits W6-W8 Set Number of Blocks
0 = 1 Block
1 = 2 BLocks
2 = 4 Blocks
3 = 8 Blocks
4 = 16 Blocks
5-7 = 16 Blocks

Bit W9 Trigger Delay Select
0 = Disable Trigger Delay
1 = Enable Trigger Delay

Bits W10-W24 Not Used

The module will ignore this command and return Q=0 and X=1 if the command is received while the module is "active" (digitizing and loading memory). The module will accept this command and return Q=1 and X=1 during all other operating states.

6.17.7 Command #7 Set Post-Trigger Sample Count [F(16).A(1).D(XXXXXX)]

This command loads the required number of post-trigger samples into the module from Dataway write lines W1 through W17 (W18-W24 not used). The integer quantity loaded may be from 0 to 131,071 (1FFFF Hex).

The module will ignore this command and return Q=0 and X=1 if the command is received while the module is "active". The module will accept this command and return Q=1 and X=1 during all other operating states.

6.17.8 Command #8 Enable Unload [F(17).A(x).D(YYYYYY)]

This command sets up the memory unloading sequence for block number n (n=x+1). This command utilizes the CAMAC data field as follows:

W1-W17 Starting point or offset of the requested data from the oldest variable data within the requested block.

W18-W24 Channel Address (1 to 15 allowed)

When the entire memory for a given channel is to be read out, this command will be issued as F(17).A(0).D(Y) (Y contains channel address in bits 18-24 followed by zeros) and followed by a sufficient number of F(2).A(0) commands to unload the entire memory, block to block, with each block starting with the oldest data for that block.

The module will respond to this command and return Q=1 and X=1 only if the requested block contains some new data that had been loaded since the last ARM command. If the requested block was either not armed to be active, or was armed but does not contain new data the module will return X=1 and Q=0 and the command will be ignored. Unload commands (Command #4) that may follow the unsuccessful issuance of this command will return Q=0 and data of all zeros.

In addition, the receipt of this command will stop any digitizing sequence that may be in progress.

6.17.9 Command #9 Set "End of Record" [F(25).A(0)]

This command forces the module to stop any digitizing sequence that may be in progress and set the module's internal End of Record Flag (Command #1 will indicate "Digitizing Sequence Complete"). The

potential use of this command is to stop the module sequence through CAMAC command.

The module will respond to this command and return Q=1 and X=1 during all modes of operation. This command will not affect the module in any way other than to stop the digitizing sequence if such is in progress. If the command is received when the EOR is already set, then the module will not be affected.

6.17.10 Command #10 Start Self Test [F(25).A(1)]

This command shall cause the module to drive its "Self Test" command line low (true). This will be switched back to its normal state upon the occurrence of any of the following:

The module "end of record" is reached by virtue of all commanded blocks having been completed (triggered on completed required memory loading).

The receipt of a "Set End of Record" CAMAC command.

The receipt of an "Enable Unload" CAMAC command.

The module will respond to this command and return Q=1 and X=1 if the command is received when the module is not "active". The module will ignore this command and return Q=0 and X=1 if the command is received while the module is active.

6.17.11 Command #11 Trigger Module [F(25).A(2)]

This command triggers the module within its commanded mode. The module will respond to this trigger signal in an identical way as it would respond to an incoming trigger grom its front panel connector.

The module will respond to this command and return Q=1 and X=1 during all modes of operation.

6.17.12 Command #12 Arm Module [F(26).A(0)]

This command "arms" the module within its commanded mode (set up via Command #6 and Command #7). This command is required to start a new digitizing sequence.

The module will respond to this command and return Q=1 and X=1 during all modes of operation. The module will respond to this command by initializing internal counters and registers as follows:

6.17.12.1 The Oldest Data Register for each block will be set to the address corresponding to the beginning of the block. The Oldest Data Registers of blocks not active will be set to zero.

6.17.12.2 Any digitizing or read out sequence that may be in progress will be terminated.

6.17.12.3 All internal flags and counters will be initialized to start the digitizing sequence.

6.17.12.4 When set up for pre-trigger mode of operation, the first block loading will be started.

6.17.13 Dataway Responses Q and X

The module will return X=1 for all addressed commands if it recognizes the command as one it is equipped to perform. The module will return Q=1 conditionally if the module is ready to participate in the commanded function.

6.17.14 Initialize or Clear Z+C

The module will respond to either of these signals by clearing all internal registers and placing the module in an inactive state. After such a clear, the module may be armed to any desired state. Memory data shall not be affected by these clear signals.

6.18 Front Panel Indicators

The module shall provide seven (7) LED indicators mounted for visibility from the front panel. The indicators shall function as follows:

LED #1 "N" shall illuminate for approximately 100 milliseconds whenever N is received.

LED #2 "ARMED" shall illuminate whenever the module is in the armed state (not yet triggered).

LED #3 "TRIG" shall illuminate for approximately 100 milliseconds whenever a trigger is received (pulse or CAMAC).

LED #4 "UNLOAD" shall illuminate for approximately 100 milliseconds whenever an unload (F2) command is received.

LED #5 "SELF TEST" shall illuminate whenever the module is in the self test mode.

LED #6 "EXT CLK" shall illuminate whenever the external (front panel) clock is selected as the clock source.

LED #' "ACT" shall illuminate for approximately 100 milliseconds whenever a "convert" signal is generated.

7.0 Environmental Data

7.1 The module must operate, as defined, over an ambient temperature range of 0 to +50 degrees C.

7.2 The module must operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must operate, as defined, in the presence of an external magnetic field changing at a maximum rate of 200 gauss per second with a peak magnitude of 100 gauss in any direction. No components, such as reed relays, with known susceptibility to such magnetic fields shall be used.

7.4 The module must operate, as defined, in a radiation environment as listed below. No components, such as dynamic RAM, with known susceptibility to such radiation shall be used.

Neutrons:	2 x 10 7 N/CM2/sec
Rad-Dose:	5 x 10 -2 rad (Si)/sec
Integrated Dose:	200 rad (Si)

8.0 Safety

All components of this module must be of flame retardant material.

9.0 Testing

All modules shall be subjected to a temperature cycling period followed by a functional test prior to shipment. A description of the tests performed shall be submitted by the vendor for incorporation into this specification.

10.0 Reliability and Quality Control

The module shall meet all applicable requirements specified in Reference 2.5.

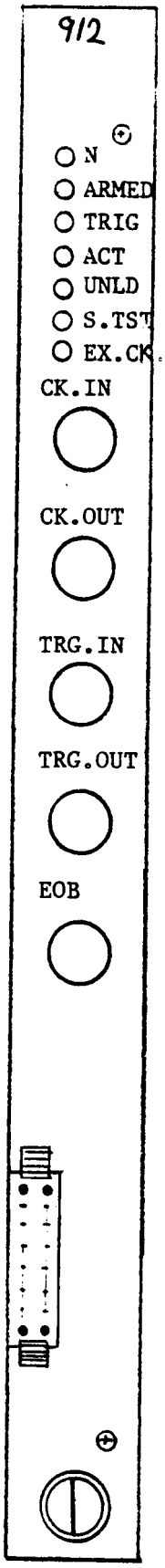
PRINCETON PLASMA PHYSICS LABORATORY
ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT

NAME

DATE | REVISION DATE



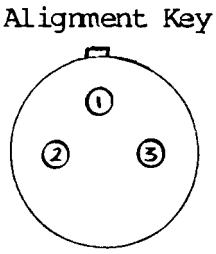
Suggested Front Panel Layout

Figure 11.1

LEMO Type RGOB303 CA22

PIN	TYPE	USE
1	female	*
2	female	signal high
3	female	signal low

View from solder cup (or crimp) side



Typical Connector Circuitry

* Chassis ground for Trigger Output, Clock Output, and End of Block. For other connectors, this pin shall be connected to a printed circuit strap jumper to allow connection to the ground through a series of .01 microfarad capacitor. The module will be initially shipped with the capacitor installed, but with the jumper not connected. See Figure 11.7.

FIGURE 11.2

AUXILIARY CONNECTOR

(Viewed from front of Crate)

PIN	FUNCTION	PIN	FUNCTION
1B	MAB 19 (GND)	1A	MAB 1
2B	MAB 18 (GND)	2A	MAB 0
3B	MAB 17 (GND)	3A	GND
4B	MAB 16	4A	NC
5B	MAB 15	5A	NC
6B	MAB 14	6A	NC
7B	MAB 13	7A	NC
8B	MAB 12	8A	DB 7
9B	MAB 11	9A	DB 6
10B	MAB 10	10A	DB 5
11B	MAB 9	11A	DB 4
12B	MAB 8	12A	DB 3
13B	MAB 7	13A	DB 2
14B	MAB 6	14A	DB 1
15B	MAB 5	15A	DB 0
16B	MAB 4	16A	GND
17B	MAB 3	17A	Write Strobe
18B	MAB 2	18A	Read Strobe

AUXILIARY CONNECTOR

PIN ASSIGNMENTS

FIGURE 11.3

CONTROL PORT

PIN ASSIGNMENT

(Connector as Viewed From Front of Crate)

PIN #	FUNCTION	PIN #	FUNCTION
1	UNLOAD PULSE	2	GROUND
3	SELF TEST COMMAND	4	GROUND
5	CHAN.AD(3) MSB	6	GROUND
7	CHAN.AD(2)	8	GROUND
9	CHAN.AD(1)	10	GROUND
11	CHAN.AD(0) LSB	12	GROUND
13	"CONVERT" PULSE	14	GROUND
15	UNUSED	16	GROUND
17	SELF TEST HIGH	18	GROUND
19	SELF TEST HIGH	20	GROUND

FIGURE 11.4

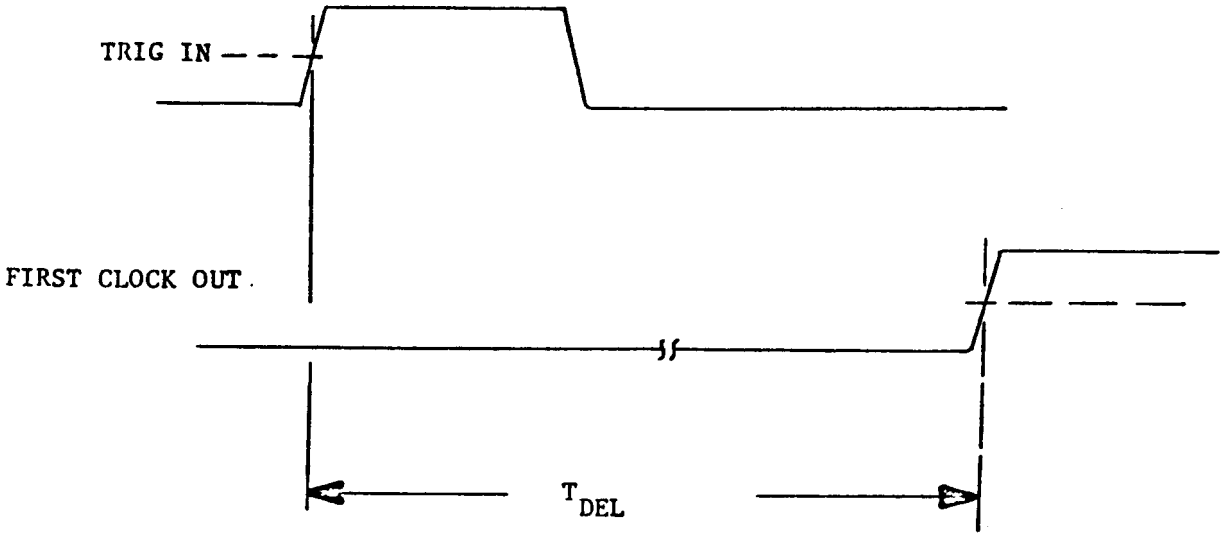
PRINCETON PLASMA PHYSICS LABORATORY
ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT

NAME

DATE | REVISION DATE



T_{DEL} = 1 clock period (2Us minimum) -0, +1Us

FIGURE 11.5

Example of first clock in post-trigger mode, internal clock

PRINCETON PLASMA PHYSICS LABORATORY
ENGINEERING NOTE

PROJECT | SERIAL-CATEGORY | PAGE

SUBJECT | NAME | DATE | REVISION DATE

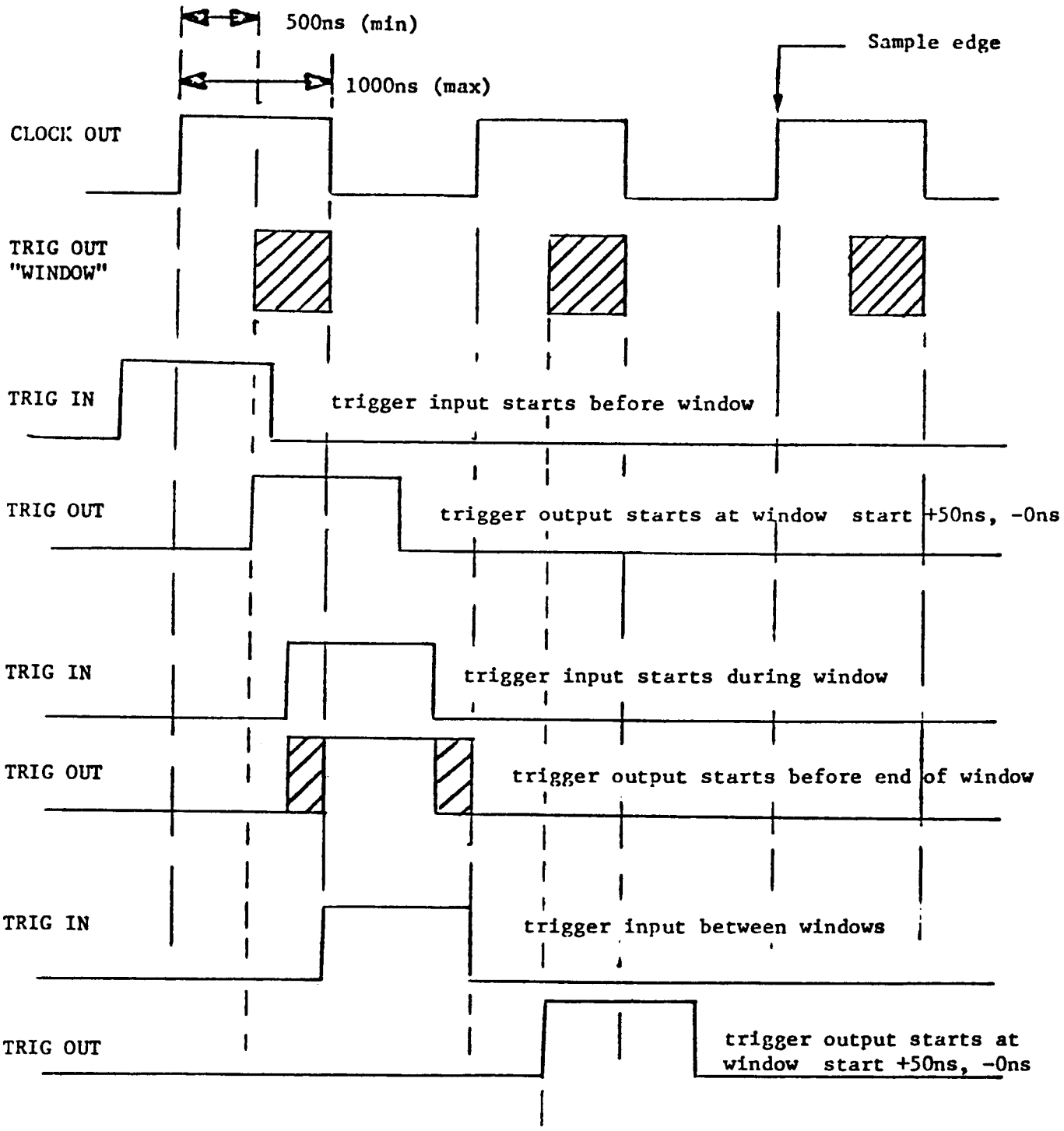


FIGURE 11.6

Examples of "Delay Trigger"

PRINCETON PLASMA PHYSICS LABORATORY
ENGINEERING NOTE

PROJECT | SERIAL-CATEGORY | PAGE

SUBJECT | NAME | DATE | REVISION DATE

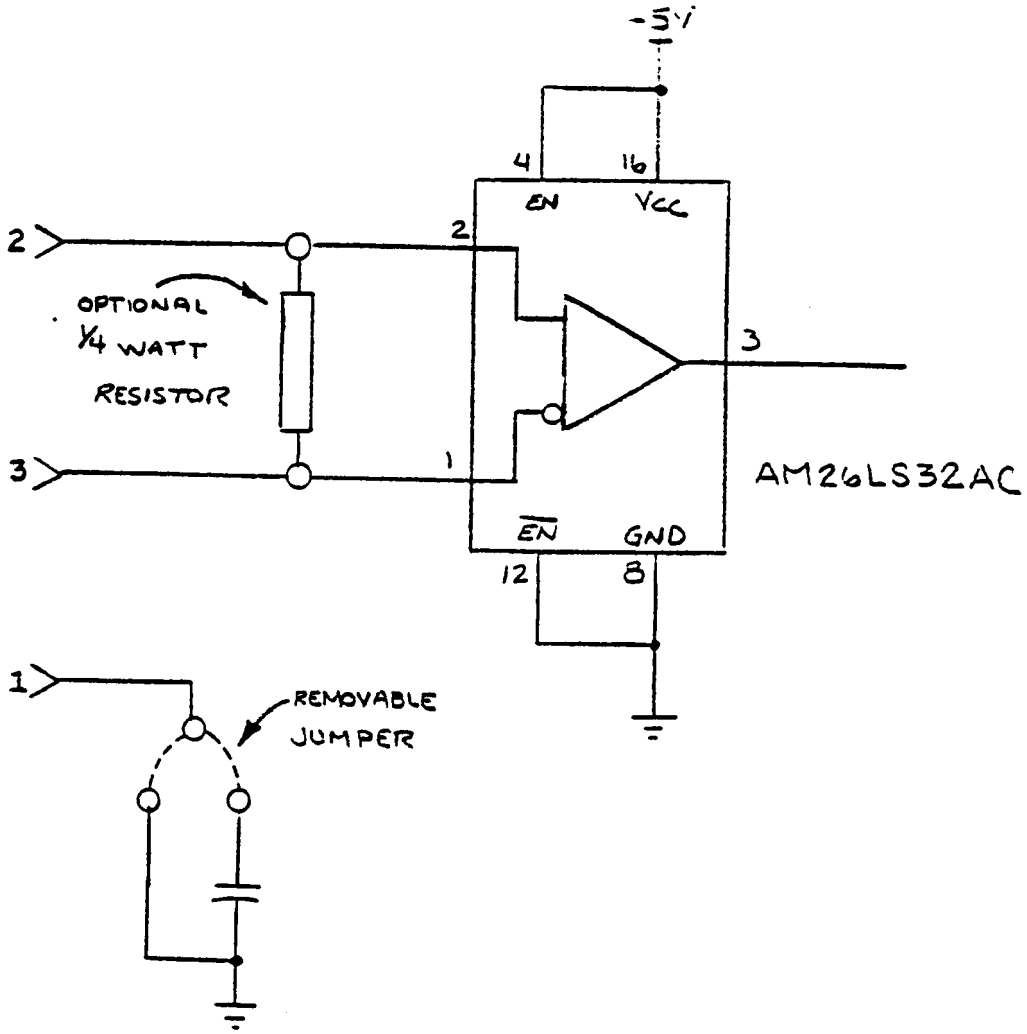


FIGURE 11.7

CLOCK INPUT CIRCUIT

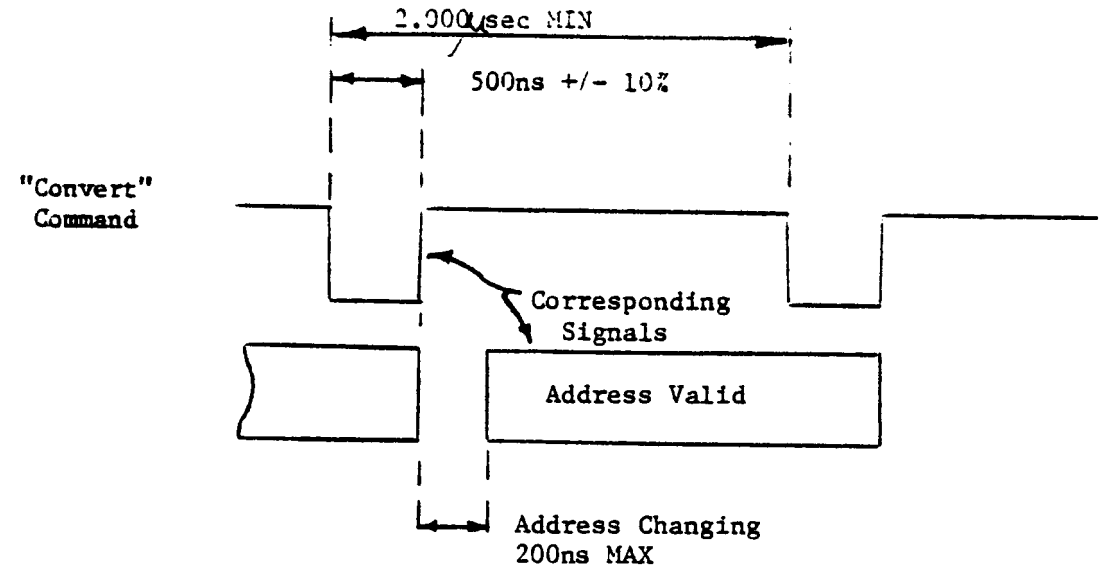
PRINCETON PLASMA PHYSICS LABORATORY
ENGINEERING NOTE

PROJECT | SERIAL - CATEGORY | PAGE

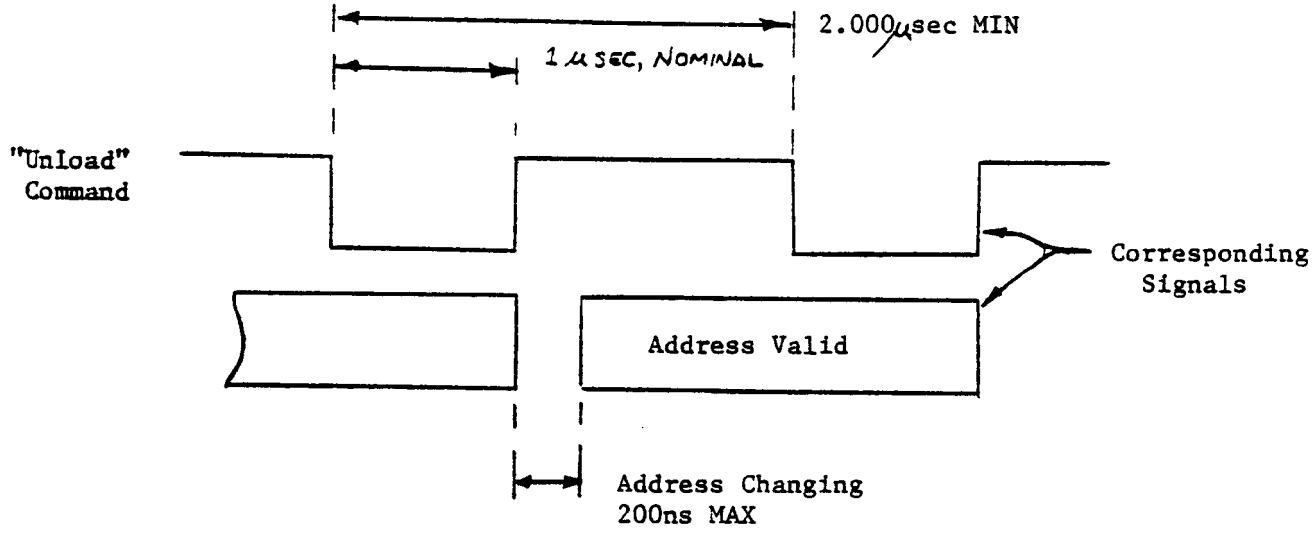
SUBJECT

NAME

DATE | REVISION DATE



Data Acquisition



Data Unloading

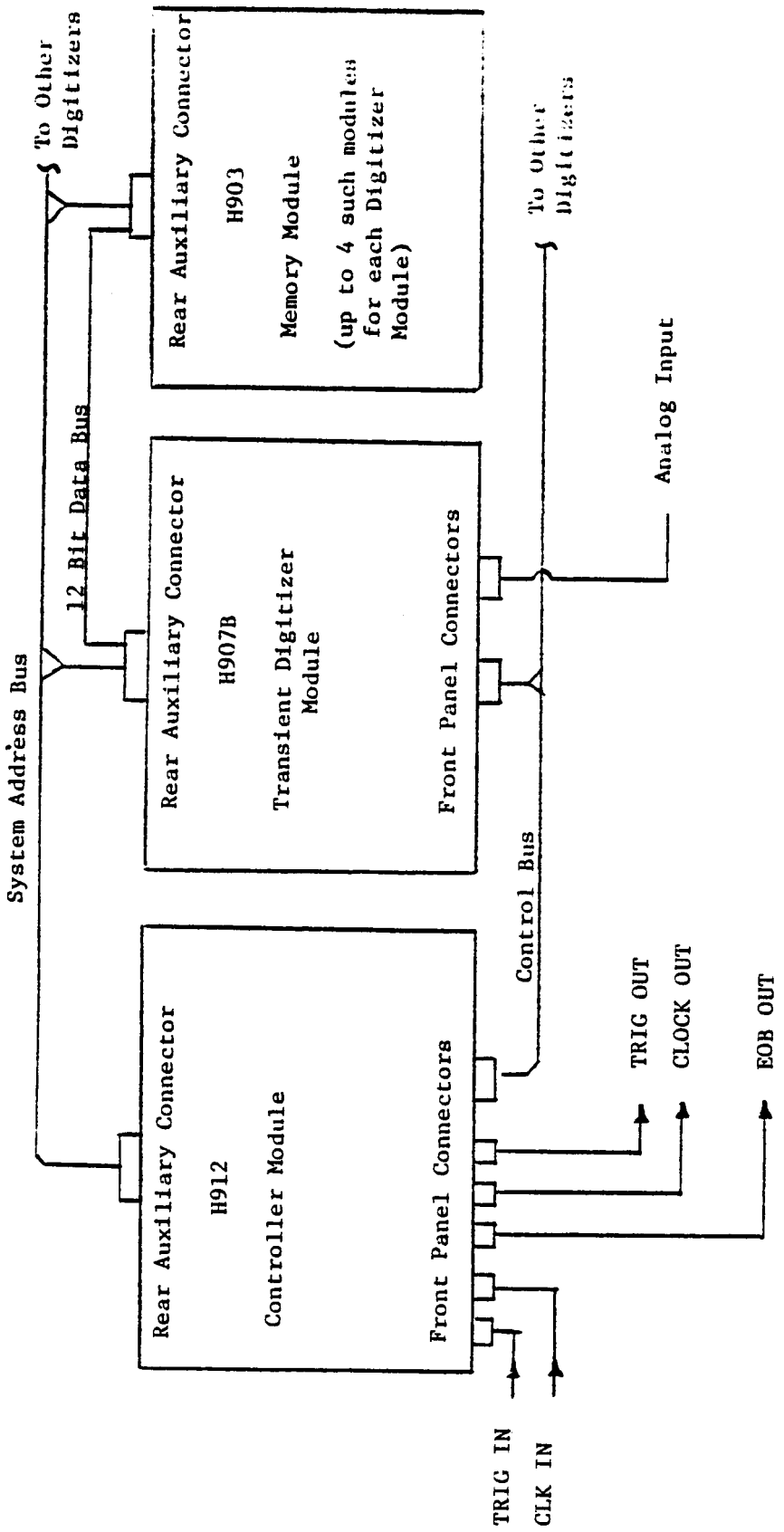
System Timing

Figure 11.8

PRINCETON PLASMA PHYSICS LABORATORY
ENGINEERING NOTE

PROJECT | SERIAL-CATEGORY | PAGE

SUBJECT | NAME | DATE | REVISION DATE



Interconnect Block Diagram

Figure 11.9

PRINCETON PLASMA PHYSICS LABORATORY
ENGINEERING NOTE

PROJECT | SERIAL-CATEGORY | PAGE

SUBJECT | NAME | DATE | REVISION DATE

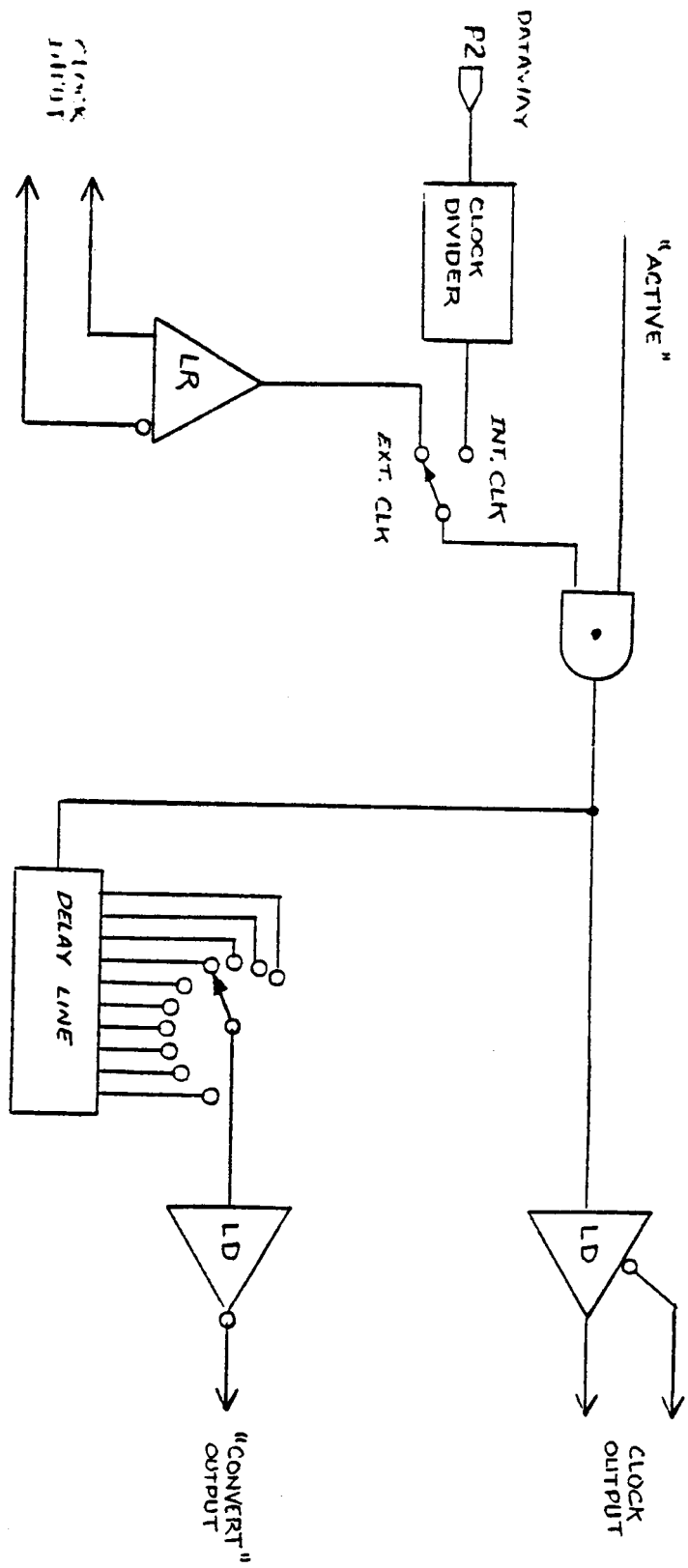


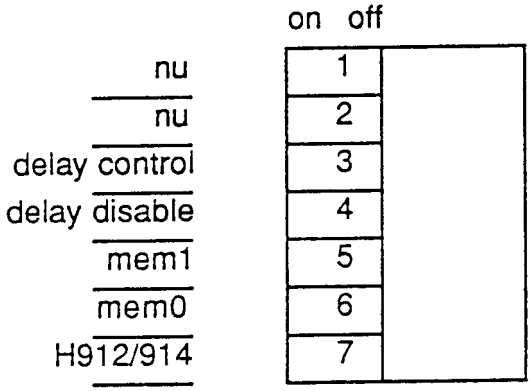
FIGURE 11.10
DELAY LINE CONFIGURATION
FOR MULTI-CONTROLLER SYNCHRONIZATION

10-20-86

appendix B

"YELLOW DOT" SWITCH SETTINGS

912/914
↳ 2 MHz
↳ 500 KHz



BA32

	8k	32k	64k	128k
mem1	on	on	off	off
mem0	on	off	on	off

	912	914
H912/914	on	off

delay control

	sw3	sw4	mode
invalid	on	on	not used
software control	on	off	~~master(1)/slave(0)~~
hardware control	off	on	delay disabled (slave)
harddware control	off	off	delay enabled (master)