2/12/85

USER GUIDE FOR THE 912R DIGITIZER CONTROLLER

This document describes a digitizer controller that supports a subset of those features described in the H912 specification. This 912R digitizer controller may be used instead of the full function 912 as a less expensive alternative if the mode of operation is supported by the 912R.

1. BASIC FEATURES

The 912R is capable of controlling up to fifteen 907/913 digitizer modules in single block post trigger mode. It supports the clock frequencies called out in the 912 spec and can also be configured to accept an external clock. In addition to the 912 specified internal clock frequencies, the 912R can be configured to supply a 2 MHz sample rate to drive 913 type 3 digitizers at their maximum frequency.

As per the 912 spec, the 912R will support 8K, 32K, 64K, or 128K words of memory.

Below is a list of the major 912 functions not supported by the 912R:

- pre-trigger mode is not supported
- multiple blocks is not supported
- no master/slave, trigger out, etc.
- the self test feature is not supported
- unloading every Nth word is not supported

2. CAMAC FUNCTIONS

F(0) A(0) - Read Status

Bits R1-R3 Operating Mode
- 0 = Unload Mode
- 1 = Post-trigger Mode
- 2-7 not used

Bits R4-R5 Operating State
- 0 = Digitizing Sequence Complete
- 1 = Armed (but not triggered)
- 2 = Armed and Triggered
- 3 = not used

Bits R6-R7 Available Memory (per channel)
0 = 8K words
1 = 32K words
2 = 64K words
3 = 128K words

Bits R8-R10 not used

Bits R11-R14 Number of Memory blocks
0 = 1 block

Bits R15-R18 Clock Selected
0 = 500 KHz
1 = 200 KHz
2 = 100 KHz
3 = 50 KHz
4 = 20 KHz
5 = 10 KHz
6 = 5 KHz
7 = 2 KHz
8 = 1 KHz
9 = 500 Hz
10 = 200 Hz
11-15 not used

Bit R19 Internal/External Clock
0 - Module strapped for Internal clock
1 - Module strapped for External clock

Bit R20 External clock source
0 - front panel
1 - on board 2 MHz oscillator

Bits R21-R24 Always 0

F(0) A(2) Read Status 2: R1=1 when EOR, R17=1 when EOR

F(2) A(0) Read Memory Buffer

This CNAF causes the 912R to issue an UNLOAD pulse to the digitizer modules such that the data in the next memory location is read from the previously selected digitizer channel.

F(6) A(0) Read Module ID

This command gates the module ID (decimal 912) onto the dataway.

F(16) A(0) Set Up Module

This command is used to select the desired internal clock frequency as described below:

Bits W2-W5

0 = 500 KHz
1 = 200 KHz
2 = 100 KHz
3 = 50 KHz
4 = 20 KHz
5 = 10 KHz
6 = 5 KHz
7 = 2 KHz
8 = 1 KHz
9 = 500 Hz
10 = 200 Hz
11 - 15 not used

The module will ignore this command (and return Q=0) if it is "active" and presently digitizing.

F(17) A(0) Enable Unload

This command puts the 912R in the unload mode and must be issued before a F(2)A(0) command is attempted. The data field is used as follows:

Bits W1-W17 Starting address for reading data

Bits W18-W24 Channel Address (1 to 15 allowed)

The receipt of this command will stop any digitizing sequence that may be in progress.

F(25) A(0) Set "End of Record"

F(25) A(2) Trigger Module

F(26) A(0) Arm Module

3. MODULE SET UP

The module contains an eight position DIP switch for clock selection (internal or external) and memory size available. Below is a description of the switch positions :

MEMORY SIZE	SW1	SW2
8K	ON	ON
32K	OFF	ON
64K	ON	OFF
128K	OFF	OFF

CLOCK SELECTION	SW3	SW4	SW5
INTERNAL	ON	ON	OFF
EXTERNAL	OFF	ON	OFF*
2 MHz OSC	OFF	OFF	ON

*-If External clock exceeds 500KHz, SW5 should be ON

PRINCETON PLASMA PHYSICS LABORATORY

ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT

912R Controller front panel

NAME

DATE

REVISION DATE

1 cutout 7/16" x 1 1/4", 1 1/4" from lower edge

5 holes 1/8" d, 1/32" from edge

2 holes 3/8" d, 1/32" from edge

engrave all words and letters into panel