JOERGER ENTERPRISES, INC.

STEPPING MOTOR CONTROLLER AND DRIVER, MODEL SMC-L

FEATURES:

- *COMPLETE MOTOR CONTROL AND DRIVE CAPABILITY IN A #1 MODULE*
- *DRIVERS ARE OPTICALLY ISOLATED AND INTERNALLY BIASED*
- *ADJUSTABLE LINEAR ACCELERATION AND DECELERATION TIME*
- *MANUAL MODE OF OPERATION*
- *2's COMPLIMENT LOGIC*
- *LOW POWER IC's FOR IMPROVED RELIABILITY*

OPTIONAL FEATURES:

- *COMPLETE PROGRAMMABLE CONTROL OF ACCELERATION TIME AND MOTOR SPEED*
- *HALF STEP MODE FOR IMPROVED RESOLUTION*
- *HIGH CURRENT DRIVE IN EXCESS OF 6 AMPS*

The Model SMC-L is a self contained stepping motor controller and optically isolated driver packaged in a single width module. Its features provide the ability to satisfy most stepping motor applications. The standard unit has adjustable linear acceleration and deceleration to provide an efficient method of driving high torque loads at their maximum speed. The standard speed range is 50pps to 2000pps with other ranges available if required. The four drivers are capable of switching up to 4 amps per phase at 28 volts, with an optional capability of over 6 amps. To simplify installation the drivers are biased internally. This means the only components required are the current limiting resistors, which must be determined in each application to satisfy the motors current and voltage requirements. The drivers feature low saturation voltage to limit the power dissipation inside the module. Three external, high level logic inputs are used to test the status of the external system, a clockwise limit, counterclockwise limit, and a signal that indicates power is being applied to the motor. Logic is provided that will inhibit the driver if a limit signal is received and the motor is requested to, or is stepping in that direction. The number of steps is determined by a 16 bit command word that is in 2's compliment. Bit 16 determines direction and the remaining 15 bits contain the number of steps to be performed. An interrupt structure is provided to improve system integration. A LAM F.F. will be set by either a CW or CCW limit or when the counter reaches zero, indicating the end of a cycle.

The motor may also be clocked with external signals using the modules drivers. A CW and CCW input is provided that is decoded to the four phase code required by the drivers and will drive the motor independently of the dataway. The motor may also be driven manually by means of a front panel switch. This can be very useful for setup or for operation without the main system running. The manual mode speed is approximately 50pps. and the switch is a locking type with an off

position so that it will not be inadvertently switched during normal operations.

To provide the ability to drive motors that require more than 6 amps, two types of external signals are provided that can drive either type of external motor driver. A CW and CCW pulse train is available and also a clock signal and a direction bit. These signals contain the acceleration time and speed information generated by the module. The CW, CCW signals can also be used to monitor the module externally with an up-down counter like our Model S2. To truly monitor the system, however, we recommend monitoring the motor itself and not the driver. By using a synchro to digital converter or an incremental encoder attached to the motor and our Model SDC, synchro to digital converter readout or our Model IE incremental encoder readout. The loop is closed providing more dependable results. Please feel free to consult the factory for more information about this type system.

The following optional features are also available to further enhance the usefulness of this module.

MODEL SMC-LP, Programmable Operation

This option allows the maximum operating speed and the acceleration/deceleration time to be selected under program control rather than manually at the front panel. This is accomplished by the addition of a 16 bit register. Bits 1-8 are used to select the maximum speed and bits 9-16 are used to select the acceleration time desired. To verify the setting, this register can be read out using command N·F1·A0. In response to an initialize signal or during power up, this register is reset. This sets the speed to minimum and the acceleration time to maximum. The least severe operating mode.

MODEL SMC-LH, Half Step/Full Step Operation

This option provides the ability to improve resolution by being able to drive the motor in half steps in addition to the normal full step mode. The operating mode is selected by a front panel switch. This switch can also be read out on the dataway to verify its operating mode. Half step operation allows resolution to be improved and is especially useful where inaccuracys in mechanical gearing cannot be tolerated. It is also useful when a system is already in operation and improved resolution is required.

MODEL SMC-LC, High Current Operation

This option is for applications requiring higher drive current requirements. It provides an optically isolated drive capacity in excess of 6 amps.

The inclusion of any of these options to the Model SMC-L makes the module a double width unit. Any combination of these options may be supplied simultaneously.

MODEL SMC-R, Dual Channel Stepping Motor Controller

This module contains two independent stepping motor controllers and drivers packaged in a single width module. For more complete details consult the data sheet for the Model SMC-R.

SPECIFICATIONS:

Outputs (Logic outputs are TTL compatible, Logic "1" = 0 volts)

Motor Drivers	Four phase, unipolar drive, internally biased, capable of 4 amps at 28 volts, diode protected.
High Current Driver Option	The Model SMC-LC is capable of switching in excess of 6 amps.
Internal Motor Power	+24 volts from the dataway is available at the connector to drive the motor. This is fused at 3 amps.
Frequency and Acceleration Test Points	To monitor the frequency of the output and the acceleration time, test points are available at front panel and in the connector.
CW Output, CCW Output	To monitor both CW and CCW Steps. Motor steps on trailing edge. Can also be used to drive an external high current motor driver.
Direction Bit and Clock	These two signals can be used to drive external motor drivers that require sign/clock inputs.
Active	To indicate when a cycle is in progress.

Inputs

Clockwise Limit, Counterclockwise Limit, External Power	Logic "0" = 8v min., Logic "1" = 6v max. These signals must be in the logic "1" state for operation, thus both a limit signal or a broken wire would indicate an abnormal condition.
CW Input, CCW Input	The motor can be driven externally in the CW or CCW direction by a TTL signal (logic "1" = 0 volts). The motor steps on the trailing edge of the pulse.
Stop Input	A logic "1" (0 volts) will abort the cycle and reset the module.

Manual Control

A three position locking toggle switch is provided to step the motor in the CW or CCW direction. An OFF position is provided to disable this feature. This switch is gated with the CW and CCW limits so that the motor cannot be driven when a limit condition exists.

Front Panel Adjustments

Acceleration/Deceleration	A multi-turn pot adjusts acceleration and equal deceleration time from 20msec. to 2sec.
Maximum Frequency	A multi-turn pot adjusts the maximum frequency from 50pps to 2000pps. (Other frequencies can be provided, consult factory.)

CAMAC Commands

N·F0·A0	Reads count register onto read lines 1-16.
N·F0·A1	Reads status register onto read lines 1-5.
N·F1·A0	Reads out the control register on R lines 1-16. If the half speed option is also included it will read out this on R17, with a "1" indicating the module is in the half step mode.
N·F1·A15	Reads module identity in BCD: 00.260.X
N·F8·A15	Tests LAM, Q=1 if LAM F.F. is set and unit enabled.
N·F10·A15	Resets LAM F.F.
N·F16·A0·S1	Loads 2's compliment data into count register from write lines W1-16. Strobe S2 initiates the cycle. Note the limit and bit "16" must not be in conflict or the cycle will not begin and A Q=0 will be returned. Resets LAM F.F.
N·F17·A0	Loads the control register with data from the W lines 1-16. W1-8 selects the speed with all zeros selecting the minimum speed. W9-16 selects the acceleration/deceleration time with all zeros selecting the longest acceleration time.
N·F24·A15	Disables L response.
N·F25·A0	Stops motor, aborts cycle, resets unit.
N·F26·A15	Enables L response.
N·F27·A0	Tests module status to determine if module is ready for another operation. Q=1, module is ready.
N·F27·A1	Tests contents of count register, Q=1, CTR=0.
X Response	X=1 for all valid commands.
Q Response	Q=1 for F0, F1, F16, F17 and in response to F8 and F27.
L Response	An interrupt is generated if the LAM F.F. is set and the unit is enabled. It is inhibited by N.
Z·S2, Power Up	Resets count register, disables LAM response, resets LAM F.F. and resets control register.

Visual Indicators

"N"	Module is addressed.
CW	A clockwise limit exists.
CCW	A counterclockwise limit exists.
EXT. PWR.	External power is on.
CTR = 0	The counter is at zero.

Power Requirements: +6v, 490ma; +24v, 27ma; -24v, 27ma.

Size: Model SMC-L #1 CAMAC module, chassis can be isolated from signal ground. Connector, Cannon DD50P (mating half DD50S).
Model SMC-L/P, H, or C #2 CAMAC module.

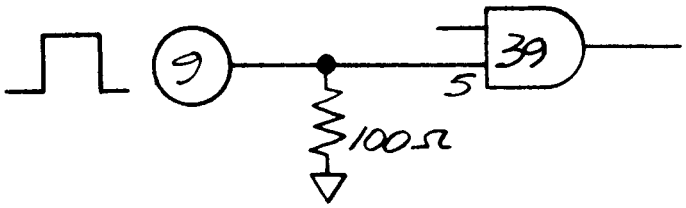
Temperature Range: 0°C to 50°C

10/80

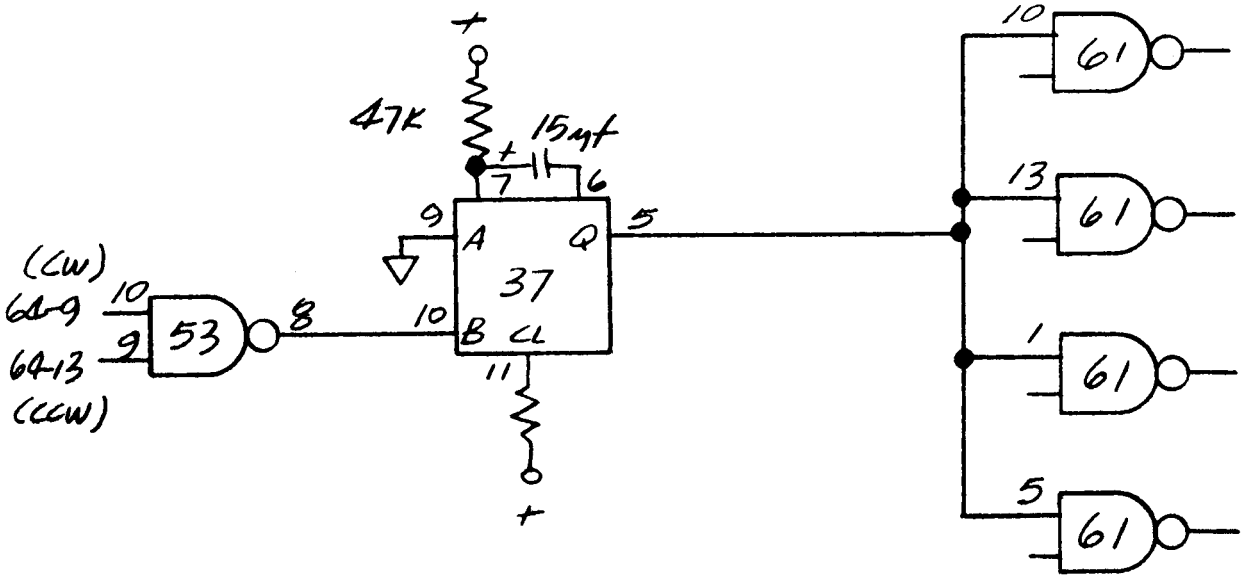
NOTE:

This Model SMC-L contains two options.

1. EXTERNAL START - Normally a cycle is triggered with function F16. At S1 time the number of steps to be performed is loaded into the counter and the operation is initiated at time S2. With this modification the operation is not started at S2. An external command is now required. Pin 9 in the front panel connector is used for this external trigger. A positive pulse of 3 volts minimum into 100 ohms is required. This change is accomplished by disconnecting the internal start pulse (16·S2) into IC 39, pin 5 and connecting pin 5 to pin 9 in the connector. A 100 ohm resistor is added to ground to terminate the signal.



2. POWER DOWN MODE - This mode has been added to reduce the power consumption of the module. When the module is not commanding the motor the drivers are turned off. Now when the motor is stopped there is no power being applied. It should be remembered however, that removing the power from the motor driver also eliminates the holding torque normally present with the motor at rest but powered. This change is accomplished by "ORing" the CW and CCW pulses in IC 53, 8, 9, 10 and triggering a long mono. The output of this mono enables the drivers by opening the gates in IC 61. Whenever the pulses stop the mono is not retriggered thus disabling the gate and turning off the drivers. The mono timing is long enough to insure the last step will be completed even under lowest speed conditions before the driver is turned off.



JOERGER ENTERPRISES, INC.

STEPPING MOTOR CONTROLLER AND DRIVER, MODEL SMC-L

THE MODEL SMC-L IS A SELF-CONTAINED STEPPING MOTOR CONTROLLER AND DRIVER ALL HOUSED IN A SINGLE WIDTH CAMAC MODULE. IT FEATURES AN ADJUSTABLE, LINEAR ACCELERATION AND DECELERATION TO PROVIDE AN EFFICIENT METHOD OF DRIVING HIGH TORQUE LOADS AT THEIR MAXIMUM SPEED. THIS MAXIMUM SPEED IS ADJUSTABLE FROM 50PPS TO 2000PPS. THE FOUR DRIVERS ARE CAPABLE OF SWITCHING UP TO FOUR AMPS PER PHASE AT A MAXIMUM OF 28 VOLTS. ALL COMPONENTS REQUIRED TO DRIVE THIS LOAD ARE INTERNAL WITH THE EXCEPTION OF THE CURRENT LIMITING RESISTORS WHICH ARE DETERMINED IN EACH APPLICATION BY THE MOTOR VOLTAGE AND CURRENT. THREE EXTERNAL, HIGH LEVEL LOGIC INPUTS ARE USED TO TEST THE STATUS OF THE EXTERNAL SYSTEM, A CLOCKWISE LIMIT, COUNTERCLOCKWISE LIMIT, AND A SIGNAL THAT INDICATES POWER IS BEING APPLIED TO THE MOTOR. LOGIC IS PROVIDED THAT WILL INHIBIT THE DRIVER IF A LIMIT SIGNAL IS RECEIVED AND THE MOTOR IS REQUESTED TO STEP IN THAT DIRECTION. THE NUMBER OF STEPS IS DETERMINED BY A 16 BIT COMMAND WORD THAT IS IN TWO'S COMPLIMENT. BIT 16 DETERMINES DIRECTION AND THE REMAINING 15 BITS CONTAIN THE NUMBER OF STEPS TO BE PERFORMED.

AN INTERRUPT STRUCTURE IS ALSO PROVIDED TO IMPROVE SYSTEM INTEGRATION. THE UNIT MAY ALSO BE CLOCKED WITH AN EXTERNAL PULSE TRAIN USING THE MODULE'S DRIVERS. BOTH CW AND CCW SIGNALS ARE AVAILABLE SO THAT THE MODULE MAY BE MONITORED EXTERNALLY WITH AN UP-DOWN COUNTER SUCH AS OUR MODEL S2. IT IS ALSO POSSIBLE TO OPERATE THE MODULE MANUALLY WITH A SINGLE FRONT PANEL SWITCH. EXTENSIVE USE OF LOW POWER IC'S RESULTS IN A POWER DISSAPATION OF APPROXIMATELY 4 WATTS

SPECIFICATIONS

OUTPUTS

MOTOR DRIVERS	FOUR PHASE, UNIPOLAR DRIVE, INTERNALLY BIASED, CAPABLE OF SWITCHING 2 AMPS, OR 4 AMPS AT 28 VOLTS. (CAN BE EXTERNALLY BIASED FOR HIGHER CURRENT SWITCHING)
INTERNAL MOTOR POWER	+24 VOLTS FROM THE DATAWAY IS AVAILABLE AT THE CONNECTOR TO DRIVE THE MOTOR. THIS IS FUSED AT 3 AMPS.
FREQUENCY TEST POINT	A PIN IS AVAILABLE IN THE OUTPUT CONNECTOR TO MONITOR THE FREQUENCY OF THE OUTPUT SIGNALS. LOGIC "0" 2.5V LOGIC "1" .5V
ACCELERATION TEST POINT	A PIN IS AVAILABLE TO MONITOR THE ACCELERATION TIME. LOGIC "0" 2.5V LOGIC "1" .5V

CCW OUTPUT	A TTL PULSE, LOGIC "1" = 0 VOLTS, TO MONITOR COUNTERCLOCKWISE STEPS. MOTOR STEPS ON TRAILING EDGE OF PULSE.
CW OUTPUT	A TTL PULSE, LOGIC "1" = 0 VOLTS, TO MONITOR CLOCKWISE STEPS. MOTOR STEPS ON TRAILING EDGE OF PULSE.
ACTIVE	A TTL LEVEL SIGNAL THAT INDICATES WHEN A CYCLE IS IN PROGRESS. 0 VOLTS = UNIT ACTIVE.

INPUTS

CLOCKWISE LIMIT, COUNTERCLOCKWISE LIMIT, EXTERNAL POWER	LOGIC "0" = 8 VOLTS MINIMUM LOGIC "1" = 6 VOLTS MAXIMUM THESE ARE ALL NORMALLY IN THE LOGIC "1" STATE, THUS BOTH A LIMIT SIGNAL OR A BROKEN WIRE WOULD INDICATE AN ABNORMAL CONDITION.
CW INPUT	THE MODULE CAN BE DRIVEN EXTERNALLY IN THE CW DIRECTION BY A TTL SIGNAL, (LOGIC "1" ZERO VOLTS). THE MOTOR STEPS ON THE TRAILING EDGE OF THE PULSE.
CCW INPUT	THE MODULE CAN BE DRIVEN EXTERNALLY IN THE CCW DIRECTION BY A TTL SIGNAL, (LOGIC "1" ZERO VOLTS). THE MOTOR STEPS ON THE TRAILING EDGE OF THE PULSE.
STOP INPUT	A LOGIC "1" (0 VOLTS) WILL ABORT THE CYCLE AND RESET THE MODULE.

MANUAL INPUT

MANUAL CONTROL	A THREE POSITION LOCKING TOGGLE SWITCH IS AVAILABLE TO STEP THE MOTOR IN THE CW OR CCW DIRECTION. AN OFF POSITION IS PROVIDED TO DISABLE THIS FEATURE. THE SWITCH GATES THE INTERNAL CLOCK (APPROX. 50HZ) TO STEP THE MOTOR. THIS SWITCH IS GATED WITH THE CW AND CCW LIMITS SO THAT THE MOTOR CANNOT BE DRIVEN INTO A LIMIT CONDITION.

FRONT PANEL ADJUSTMENTS

ACCELERATION/DECELERATION	THIS MULTI-TURN POT ADJUSTS THE ACCELERATION (AND EQUAL DECELERATION) TIME FROM 20MSEC. TO 2SEC.
MAXIMUM FREQUENCY	THIS MULTI-TURN POT ADJUSTS THE MAXIMUM FREQUENCY FROM 50PPS TO 2000PPS.

CAMAC COMMANDS

N•F0•A0	READS COUNT REGISTER ONTO READ LINES 1-16, RETURN Q=1.
N•F0•A1	READS STATUS REGISTER ONTO READ LINES 1-5, RETURNS Q=1. R1 = EXTERNAL POWER ON R2 = CLOCKWISE LIMIT R3 = COUNTERCLOCKWISE LIMIT R4 = COUNTER EQUALS ZERO R5 = INTERNAL +24 VOLTS, OFF
N•F1•A15	READS MODULE IDENTITY IN BCD 00.260.0
N•F8•A15	TESTS LAM, IF SET AND UNIT IS ENABLED IT WILL RESPOND WITH Q=1.
N•F10•A15	RESETS LAM FLIP-FLOP.
N•F16•A0•S1	LOADS TWO'S COMPLIMENT DATA INTO COUNT REGISTER FROM WRITE LINES W1-16. STROBE S2 INITIATES THE CYCLE. NOTE THAT THE LIMIT SWITCHES AND BIT "16" MUST NOT BE IN CONFLICT OR THE CYCLE WILL NOT BEGIN AND A Q=0 WILL BE RETURNED. RESETS LAM FLIP-FLOP.
N•F24•A15	DISABLES L RESPONSE.
N•F25•A0	STOPS MOTOR, ABORTS CYCLE, RESETS UNIT.
N•F26•A15	ENABLES L RESPONSE.
N•F27•A0	TESTS THE STATUS WORD TO DETERMINE IF MODULE IS READY FOR ANOTHER OPERATION. Q=1 IF EXTERNAL POWER IS ON AND COUNTER EQUALS ZERO AND STEPPING MOTOR IS NOT IN A LIMIT POSITION.
N•F27•A1	TESTS CONTENTS OF COUNT REGISTER AND GENERATES Q=1 IF THE COUNTER IS ZERO.
X RESPONSE	X=1 FOR ALL COMMANDS.
Z•S2 AND POWER UP	RESETS COUNT REGISTER, DISABLES LAM RESPONSE, AND RESETS LAM FLIP-FLOP.

VISUAL INDICATORS

"N"	TO INDICATE MODULE IS ADDRESSED.
CW	TO INDICATE A CLOCKWISE LIMIT.
CCW	TO INDICATE A COUNTERCLOCKWISE LIMIT.
EXT. PWR.	EXTERNAL POWER IS ON.
ACTIVE	THE MODULE IS PERFORMING AN OPERATION.
CTR = 0	THE COUNTER IS AT ZERO.

INTERRUPT STRUCTURE

A LAM FLIP-FLOP IS PROVIDED THAT IS SET BY EITHER LIMIT CONDITION, CW OR CCW, OR WHEN THE COUNTER GOES TO ZERO INDICATING THE END OF A CYCLE. IF THE UNIT IS ENABLED AN INTERRUPT WILL BE GENERATED ON THE L LINE. THIS SIGNAL IS INHIBITED WHEN THE MODULE IS BEING ADDRESSED ON ITS W LINE.

POWER REQUIREMENTS:	+6 VOLTS, 490MA +24 VOLTS, 27MA -24 VOLTS, 27MA
SIZE:	#1 CAMAC MODULE CHASSIS CAN BE ISOLATED FROM SIGNAL GROUND.
TEMPERATURE RANGE:	$0^{o}C$ TO $55^{o}C$
CONNECTOR:	CANNON DD50P MATING CONNECTOR CANNON DD50S

LOGIC SECTION

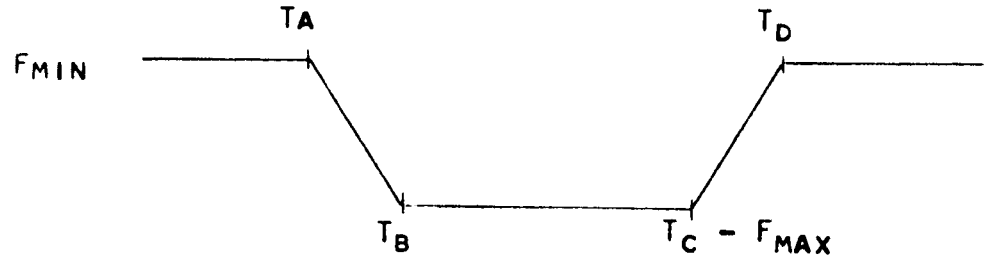
FULL DECODING IS PROVIDED TO GENERATE ALL FUNCTIONS USED BY MODULE. F0·A0 IS USED TO READ OUT THE 16 BIT "COUNTER A", (IC 18-21, 35). F0·A1 IS USED TO READ STATUS WHICH IS MADE UP OF A FIVE BIT WORD, CW LIMIT, CCW LIMIT, EXTERNAL POWER ON, COUNTER EQUALS ZERO, +24V OUTPUT. FUNCTION F27·A0 IS USED TO TEST THE STATUS OF THE MODULE AND THE RESPONSE IS RETURNED ON THE Q LINE. A Q=1 WILL BE RETURNED IF THE COUNTER IS AT ZERO, THE MOTOR IS NOT AT A LIMIT AND HAS POWER. THIS INDICATES THE UNIT CAN PERFORM THE NEXT OPERATION. F27·A1 IS USED TO TEST THE COUNTER ITSELF AND RETURNS A Q=1 IF THE COUNTER IS ZERO. F16 IS USED TO INITIATE AN OPERATION. TO GENERATE A VALID F16, THE INFORMATION ON W16 MUST BE COMPARED TO THE CLOCKWISE AND COUNTERCLOCKWISE LIMIT SWITCH INPUTS IN IC 40. IF W16 EQUALS ONE INDICATING COUNTERCLOCKWISE ROTATION IS REQUESTED, THE COUNTER-CLOCKWISE LIMIT MUST BE AT LOGIC 1 (0 VOLTS) INDICATING THAT THE MOTOR IS NOT AT THE COUNTERCLOCKWISE LIMIT. IF W16 EQUALS ZERO, INDICATING CLOCKWISE ROTATION, THE CLOCKWISE LIMIT POSITION MUST BE AT LOGIC 1. IF THESE CONDITIONS ARE MET IT IS CONSIDERED A VALID START COMMAND AND A Q-1 RESPONSE IS RETURNED. IF THESE CONDITIONS ARE NOT SATISFIED THE CYCLE WILL NOT BEGIN AND A Q=0 WILL BE RETURNED. F16·S1 IS USED TO PRESET COUNTER A WITH INFORMATION FROM WRITE LINES 1-16. ALTHOUGH THE UNIT SHOULD BE READY TO ACCEPT A NEW CYCLE, AS AN ADDED ASSURANCE, F16·S1 ALSO RESETS THE LOGIC REQUIRED TO START THIS NEW CYCLE. AT S2 THE CYCLE BEGINS. IT TRIGGERS THE GATE FLIP-FLOP AND ENABLES THE GATE INPUT OF COUNTER A AND COUNTER B. IT ALSO ENABLES THE "UP" INPUT FOR THE COUNTER IN THE OSCILLATOR SECTION, (IC 47,49).

INTERRUPT

TO HELP MONITOR THE MODULE AN INTERRUPT STRUCTURE IS PROVIDED. WHEN A CYCLE IS COMPLETE, INDICATED BY THE COUNTER REACHING ZERO, A LAM FLIP-FLOP IS SET, IC 24-2. THIS FLIP-FLOP IS RESET WITH COMMAND F10, F16 OR Z·S2. AN ENABLE DISABLE FLIP-FLOP IS PROVIDED IC 24-1 WHICH IS ENABLED BY F26 AND DISABLED BY F24 AND Z·S2. IF THE LAM FLIP-FLOP IS SET AND THE MODULE HAS BEEN ENABLED AN INTERRUPT L IS GENERATED WHEN THE MODULE IS NOT ADDRESSED. THIS MAY BE TESTED BY F8. EITHER A CW OR CCW LIMIT CONDITION WILL ALSO SET THE LAM F.F.

CLOCK GENERATION

THE CLOCK IS GENERATED FROM A VOLTAGE CONTROLLED OSCILLATOR, IC 60, THE CONTROL SIGNAL FOR THE FREQUENCY OSCILLATOR IS TRAPAZOIDAL IN SHAPE, AND SO THE OSCILLATOR'S OUTPUT FREQUENCY VARIES LINEARLY FROM A LOW FREQUENCY TO MAXIMUM, THEN AT A PREDETERMINED TIME DECREASES LINEARLY BACK TO IT'S MINIMUM FREQUENCY.



THIS TRAPAZOIDAL WAVESHAPE IS GENERATED BY USE OF AN OSCILLATOR, COUNTER AND DIGITAL TO ANALOG CONVERTER. THE ACCELERATION TIME, T_A-T_B, IS DETERMINED BY THE FREQUENCY OF THE ACCELERATION OSCILLATOR, IC 59, WHICH DETERMINES THE TIME IT WILL TAKE TO FILL THE EIGHT BIT COUNTER, (255 COUNTS).

$$T_{ACC} = \frac{1}{F\ OSC.} \times 255$$

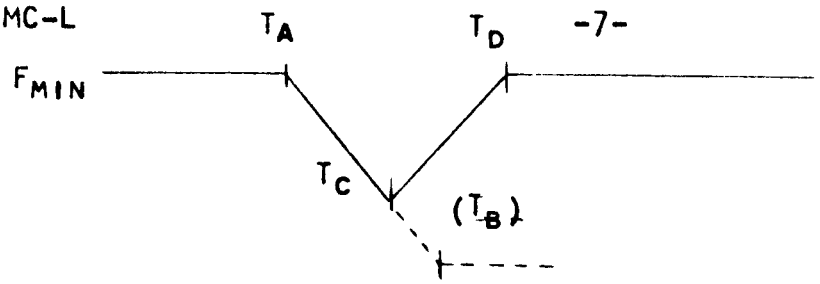
FOR: T_{ACC} = 2 SEC., $F_{OSC.}$ = 127HZ

T_{ACC} = 20MSEC., $F_{OSC.}$ = 12.7KHZ

THE OUTPUTS OF THE EIGHT BIT COUNTER, IC 47,49, ARE FED INTO AN EIGHT BIT D/A CONVERTER, IC 48, WHICH GENERATES A CURRENT OUTPUT INCREASING LINEARLY WITH TIME. THIS CURRENT OUTPUT IS CONVERTED TO VOLTAGE IN THE COMMON BASE AMPLIFIER Q2 AND FED TO THE CONTROL INPUT OF THE FREQUENCY OSCILLATOR, IC 60. THE MAXIMUM FREQUENCY OF THIS OSCILLATOR IS ADJUSTABLE FROM THE FRONT PANEL.OVER THE RANGE OF 50HZ TO 2KHZ.

A CYCLE IS INITIATED BY A VALID START SIGNAL $16_O \cdot S2$. THIS PRESETS FLIP-FLOP 51-1 AND ENABLES THE UP/DOWN COUNTERS (47,49) WHICH ARE IN THE "UP" MODE. THE CLOCK OUTPUT FROM IC 59 TRIGGERS THE COUNTERS AND DOES SO UNTIL BOTH COUNTERS HAVE FILLED, INDICATED BY THEIR MIN./MAX. SIGNALS GOING POSITIVE. THIS SIGNAL IS USED TO RESET FLIP-FLOP 51-1 VIA ITS K INPUT IN SYNC WITH THE CLOCK. THIS DISABLES THE COUNTERS WITH A FULL COUNT (ALL 1'S). THIS IS TIME T_B. THE MODULE WILL GENERATE PULSES AT THIS MAXIMUM FREQUENCY UNTIL IT IS DETERMINED DECELERATION SHOULD BEGIN, TIME T_C. THIS T_C SIGNAL SETS FLIP-FLOP 51-2 IN SYNC WITH THE CLOCK. THIS FLIP-FLOP ENABLES THE COUNTERS (47,49) AND PUTS IT IN THE "DOWN" MODE. THE COUNTER WILL NOW COUNT DOWN, CAUSING THE D/A CONVERTER OUTPUT TO DECREASE, THUS LOWERING THE "FREQUENCY OSCILLATOR" OUTPUT FREQUENCY LINEARLY TOWARD MINIMUM. THE MAIN COUNTER APPROACHES ZERO AS THE FREQUENCY GOES TO MINIMUM. THE CYCLE WILL NOT STOP, HOWEVER, UNTIL THE COUNTER REACHES ZERO, INDICATING THAT THE DESIRED NUMBER OF STEPS HAVE BEEN GENERATED. AT THIS TIME (T_D) THE GATE FLIP-FLOP IS RESET ALONG WITH THE COUNTERS AND LOGIC.

THIS DESCRIPTION ASSUMES THAT THE NUMBER OF STEPS REQUESTED WILL BE HIGH ENOUGH FOR THE SYSTEM TO ATTAIN MAXIMUM FREQUENCY. IF THE NUMBER OF STEPS IS SMALLER, HOWEVER, THE TRAPAZOIDAL CONTROL SIGNAL IS NEVER ACHIEVED AND THE RESULT IS A TRIANGULAR SHAPE.



THIS CYCLE WILL BEGIN THE SAME, AT T_A. HOWEVER, BEFORE ACCELERATION IS COMPLETE, THE UNIT WILL START TO DECELERATE IN ORDER TO END THE CYCLE AT THE MINIMUM FREQUENCY SO T_B IS NEVER ACHIEVED AND AT T_C THE DOWN CYCLE IS BEGUN AND THE UP CYCLE TERMINATED.

INTERNAL ADJUSTMENTS ARE PROVIDED FOR EACH OF THE OSCILLATORS. THE ACCELERATION OSCILLATOR'S MINIMUM FREQUENCY IS ADJUSTED BY POT R38. WITH THE FRONT PANEL ACCELERATION POT SET TO MAXIMUM ACCELERATION, (COMPLETELY CLOCKWISE), THE OUTPUT OF THE OSCILLATOR IS ADJUSTED TO HAVE A PERIOD OF 7.8MS. THE MAXIMUM FREQUENCY IS DETERMINED BY CAPACITORS C11 AND C12 WITH THE FRONT PANEL ACCELERATION POT SET TO MINIMUM (CCW). A TEST POINT IS PROVIDED AT PIN 42 IN THE CONNECTOR WHICH DISPLAYS THE ACCELERATION TIME $T_A - T_B$. IN TESTING THE ACCELERATION TIME MAKE CERTAIN THAT THE CYCLE IS LONG ENOUGH TO HAVE FULL ACCELERATION.

THE FREQUENCY OSCILLATOR IS SET SIMILARLY. HOWEVER, A CYCLE MUST BE RUNNING TO ADJUST MAXIMUM FREQUENCY SO IT IS BEST TO SET THE ACCELERATION POT TO MINIMUM AND LOAD IN THE MAXIMUM COUNT FROM THE WRITE LINES. THIS WILL ASSURE THE FREQUENCY OSCILLATOR IS RUNNING AT THE MAXIMUM FREQUENCY FOR THE LONGEST TIME. THE FREQUENCY MAY BE MONITORED ON PIN 43 OF THE OUTPUT CONNECTOR. WITH THE FRONT PANEL FREQUENCY SET AT MINIMUM (COMPLETELY COUNTERCLOCKWISE), SET POT R56 FOR A FREQUENCY OF 50HZ. WITH THE FREQUENCY POT AT MAXIMUM THE FREQUENCY WILL BE DETERMINED BY CAPACITORS C19 AND C20. THIS FREQUENCY SHOULD BE APPROXIMATELY 2KHZ.

THESE ADJUSTMENTS ARE DESCRIBED FOR YOUR INFORMATION. THEY ARE MADE AT THE FACTORY AND SHOULD NOT HAVE TO BE READJUSTED. IF YOU HAVE AN APPLICATION WHERE A DIFFERENT ACCELERATION RANGE OR FREQUENCY RANGE WOULD BE USEFUL, IT IS RECOMMENDED THAT THE OSCILLATOR'S CAPACITORS BE CHANGED. IF YOU NEED ANY ASSISTANCE PLEASE FEEL FREE TO CONTACT THE FACTORY.

COUNTER SECTION

THE COUNTER SECTION IS MADE UP OF TWO COUNTERS. COUNTER A IS A 15 BIT UP/DOWN COUNTER. COUNTER B IS A 12 BIT UP/DOWN COUNTER. COUNTER A IS THE MAIN COUNTER AND COUNTER B IS USED TO DETERMINE THE TIME FOR DECELERATION. BECAUSE THE INFORMATION ON THE WRITE LINES IS IN TWO'S COMPLIMENT, THE LOGIC FOR COUNTERCLOCKWISE AND CLOCKWISE MOVEMENT IS REVERSED.

CLOCKWISE MOVEMENT -

THE NUMBER LOADED INTO COUNTER A (IC 18-21,35) IS TAKEN FROM THE WRITE LINES AND INVERTED, COUNTER B IS RESET. THE INCOMING CLOCK IS ENABLED AND RESHAPED IN A MONOSTABLE (IC 41) TO INSURE RELIABLE CLOCK PULSES. THE CLOCK INPUT IS STEERED BY INFORMATION FROM W16 INTO THE "DOWN" INPUT OF COUNTER A. THESE SAME CLOCK PULSES ARE ALSO GATED INTO THE "UP" INPUT OF COUNTER B. COUNTER B COUNTS THESE CLOCK PULSES DURING ACCELERATION TIME. WHEN ACCELERATION IS OVER (T_B) THESE CLOCK PULSES ARE DISABLED AND THE

NUMBER LEFT IN COUNTER B REPRESENTS THE NUMBER OF PULSES REQUIRED FOR ACCELERATION AND IS ALSO EQUAL TO THE NUMBER OF PULSES THAT WILL BE REQUIRED FOR DECELERATION. AS COUNTER A CONTINUES TO COUNT DOWN IT'S LEAST SIGNIFICANT 12 BITS IS COMPARED TO THE 12 BITS FROM COUNTER B IN THREE 4 BIT COMPARATORS. WHEN THE THREE MOST SIGNIFICANT BITS IN COUNTER A ARE EQUAL TO ZERO AND COUNTER A'S LEAST SIGNIFICANT 12 BITS BECOME LESS THAN COUNTER B, THIS INDICATES THE TIME WHEN DECELERATION SHOULD BEGIN (T_c). THIS SIGNAL IS USED AS DESCRIBED PREVIOUSLY IN THE OSCILLATOR SECTION TO REDUCE THE CLOCK FREQUENCY TOWARD ZERO. COUNTER A REMAINS COUNTING DOWN UNTIL IT'S CONTENTS EQUAL ZERO. THIS IS DETERMINED BY SENSING THE OUTPUT BITS OF COUNTER A. WHEN COUNTER A EQUALS ZERO, THE CYCLE IS COMPLETE, THE GATE FLIP-FLOP IS CLOSED AND THE LOGIC IS RESET.

COUNTERCLOCKWISE MOVEMENT

COUNTER A IS PRESET IN THE SAME FASHION, HOWEVER, NOW COUNTER B IS PRESET TO ALL 1'S AND CLOCK PULSES ARE GATED TO THE "UP" INPUT OF COUNTER A AND THE "DOWN" INPUT OF COUNTER B. COUNTER B COUNTS DOWN DURING THE ACCELERATION TIME. COUNTER A IS AGAIN COMPARED WITH COUNTER B TO DETERMINE THE START OF DECELERATION, HOWEVER, THIS TIME THE THREE MOST SIGNIFICANT BITS OF COUNTER A MUST BE EQUAL TO 1'S AND WHEN COUNTER A'S CONTENTS ARE GREATER THAN COUNTER B'S, DECELERATION IS INITIATED.

IF DURING A CYCLE A LIMIT SIGNAL IS RECEIVED THE MODULE WILL STOP GENERATING OUTPUT SIGNALS UNTIL EITHER THE LIMIT SIGNAL IS REMOVED, OR IT IS COMMANDED TO MOVE IN THE OPPOSITE DIRECTION. ONLY THE LIMIT SWITCH APPROPRIATE FOR THE OPERATION, I.E. CW LIMIT FOR CW OPERATION, IS MONITORED AND HAS CONTROL OVER THE MODULE. THIS IS DONE BY GATING THE CONTENTS OF FLIP-FLOP 35 WHICH STORES "W16" WITH THE LIMIT SWITCHES IN IC 40.

DRIVER SECTION

THIS SECTION TAKES THE CLOCKWISE AND COUNTERCLOCKWISE PULSES USED TO CLOCK COUNTER A AND PUTS THEM IN THE PROPER FORMAT TO DRIVE THE STEPPING MOTOR. FOR A CLOCKWISE OPERATION THESE CLOCK PULSES GO INTO A 2 BIT "UP" COUNTER, IC 63. FOR A COUNTERCLOCKWISE OPERATION, THE CLOCK PULSES ARE APPLIED TO THE "DOWN" INPUT OF THIS 2 BIT COUNTER. BIT 2 AND ITS COMPLIMENT ARE USED TO DRIVE ONE SECTION OF THE MOTOR. AN EXCLUSIVE OR OF BIT 1 AND 2 IS GENERATED AND THIS WITH ITS COMPLIMENT IS USED TO DRIVE THE OTHER SECTION OF THE STEPPING MOTOR. TWO PHASES OF THE STEPPING MOTOR ARE DRIVEN AT EACH TIME. THEIR PHASE RELATIONSHIPS DETERMINE CLOCKWISE OR COUNTERCLOCKWISE ROTATION. EACH OF THE FOUR DRIVERS ARE OPTICALLY ISOLATED. THE OUTPUT OF THE OPTICAL ISOLATOR IS APPLIED TO AN EMITTER FOLLOWER TO PROVIDE CURRENT GAIN. ITS OUTPUT DRIVES A POWER TRANSISTOR TO SUPPLY A MINIMUM OF TWO AMPS SINKING CURRENT FOR EACH PHASE. A DIODE CLAMP IS PROVIDED FOR EACH DRIVER TO SUPPRESS TRANSIENTS.

TO ALLOW THE MODULE TO BE MONITORED THE CW AND CCW TRIGGERS ARE MADE AVAILABLE IN THE FRONT-PANEL CONNECTOR. THESE ARE IIL LEVELS. AN UP-DOWN COUNTER SUCH AS OUR MODEL S2 COULD BE USED TO COUNT THESE SIGNALS AND VERIFY THE MOTORS POSITION. IT IS ALSO POSSIBLE TO DRIVE THE MOTORS EXTERNALLY WITH A TTL SIGNAL VIA THE FRONT PANEL. THE CW OR CCW PULSES ARE FED TO THE DRIVERS TO STEP THE MOTOR. THIS INPUT BYPASSES ALL THE MODULE LOGIC EXCEPT THE LIMIT INPUTS WITH WHICH IT IS GATED. THE MOTOR STEPS ON THE TRAILING EDGE OF THE LOGIC "1" INPUT PULSE.

WITH REGARD TO THE DRIVERS, THEY ARE INTERNALLY BIASED TO DRIVE 2 AMPS AT 28 VOLTS. THE BIAS RESISTORS ARE R67, 71, 75 AND 79. BECAUSE THE WINDINGS ARE DRIVEN IN PAIRS THERE NEED ONLY BE TWO RESISTORS. HOWEVER, TO BETTER DISSIPATE THE HEAT FOUR RESISTORS ARE USED. IF YOU REQUIRE A HIGHER DRIVE CURRENT (UP TO 4 AMPS MAX.) YOU CAN PARALLEL THESE RESISTORS. THEY ARE MADE AVAILABLE AT THE FRONT PANEL CONNECTOR, PINS 21, 25, 29, 33. PINS 21 AND 25 SHOULD BE JUMPED TOGETHER AND PINS 29 AND 33. THIS WILL INCREASE THE POWER DISSIPATION IN THE MODULE, HOWEVER, BECAUSE OF THE EXTENSIVE USE OF LOW POWER I.C.'S THE POWER CONSUMPTION IN THE MODULE IS LOW. TO DRIVE ABOVE 4 AMPS THE UNIT MUST BE EXTERNALLY BIASED. RESISTORS MUST BE PLACED IN PARALLEL WITH THE INTERNAL BIAS RESISTORS. THIS IS DONE BY WIRING RESISTORS OF THE APPROPRIATE SIZE BETWEEN THE EXTERNAL BIAS POINTS AND THE POWER LINE. THE BETA OF THE DRIVE TRANSISTOR AT THIS CURRENT LEVEL SHOULD BE CONSIDERED 20. PLEASE FEEL FREE TO CONSULT THE FACTORY REGARDING YOUR PARTICULAR BIAS REQUIREMENTS.

MANUAL OPERATION

TO FACILITATE STEPPING THE MOTOR MANUALLY DURING SETUP OR WHEN THE COMPUTER IS NOT CONNECTED, A MANUAL MODE IS AVAILABLE. THIS IS A THREE POSITION LOCKING TOGGLE SWITCH THAT ALLOWS THE MOTOR TO BE STEPPED EITHER CW OR CCW. AN "OFF" POSITION IS PROVIDED TO DISABLE THIS FEATURE. THE SWITCH GATES THE INTERNAL CLOCK, APPROXIMATELY 50HZ, INTO THE DRIVER SECTION. THIS SIGNAL IS GATED WITH THE LIMIT INPUTS TO INSURE THE MOTOR CANNOT BE DRIVEN INTO A LIMIT.

STOP MODE

A CYCLE MAY BE ABORTED EITHER EXTERNALLY WITH A STOP INPUT OR UNDER PROGRAM CONTROL WITH F25. EITHER OF THESE SIGNALS HAS THE SAME EFFECT AS A Z·S2 COMMAND. IT RESETS THE UNIT, STOPS THE OPERATION, AND DISABLES THE LAM.

NOTE: THE CW AND CCW INPUTS MUST BE GROUNDED FOR THE MODULE TO OPERATE. AN OPEN CONDITION PRESENTS A LIMIT CONDITION TO THE MODULE. THE MODULE WILL RESPOND BY INHIBITING THE INITIATION OF EITHER A CW OR CCW CYCLE.

MODEL SMC-L

CONNECTOR PIN ASSIGNMENTS

17	+24v OUT	33	EXT. BIAS #4	50	CHASSIS GND.
16	+24v OUT	32	#4 OUT	49	CCW IN
15	+24v OUT	31	#4 OUT	48	CCW OUT
14	+24v OUT	30	#4 OUT	47	CW IN
13	EXT. POWER IN	29	EXT. BIAS #3	46	CW OUT
12	EXT. POWER IN	28	#3 OUT	45	STOP IN
11	EXT. POWER IN	27	#3 OUT	44	ACTIVE OUT
10	EXT. POWER IN	26	#3 OUT	43	FREQ. TEST PT.
9		25	EXT. BIAS #2	42	ACC. TEST PT.
8	DIRECT-ION OUT	24	#2 OUT	41	EXT. PWR. RET
7	GROUND	23	#2 OUT	40	EXT. PWR. RET
6	CCW LIMIT	22	#2 OUT	39	EXT. PWR.RET.
5	GROUND	21	EXT. BIAS #1	38	EXT. PWR.RET.
4	CW LIMIT	20	#1 OUT	37	GROUND
3	GROUND	19	#1 OUT	36	GROUND
2	EXT. POWER ON	18	#1 OUT	35	GROUND
1	GROUND			34	GROUND

CONNECTOR CANNON DD-50P

MATING CONNECTOR CANNON DD-50S

MODEL SMC-L

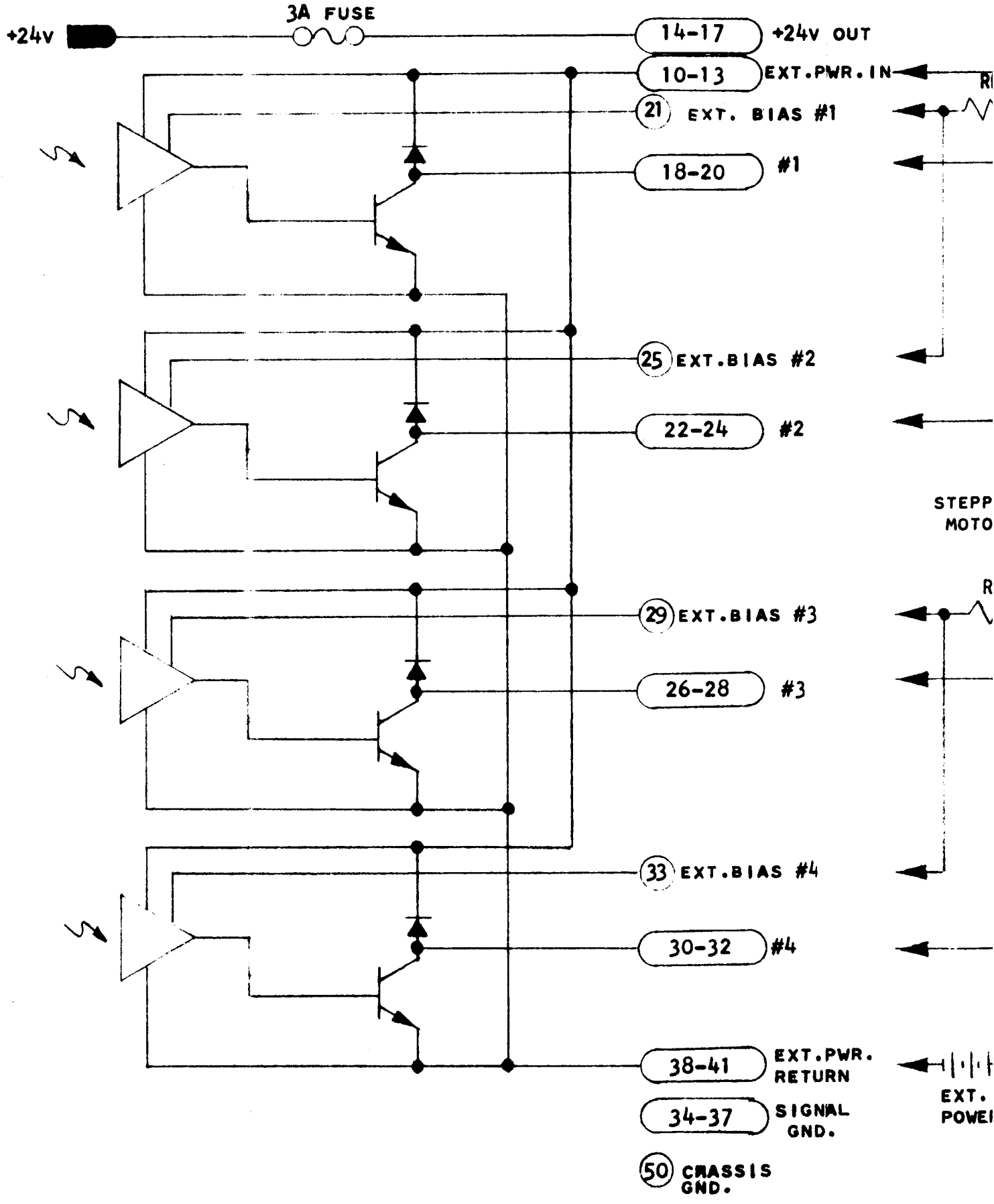
PARTS LIST

P.C. BOARD #SMC-101

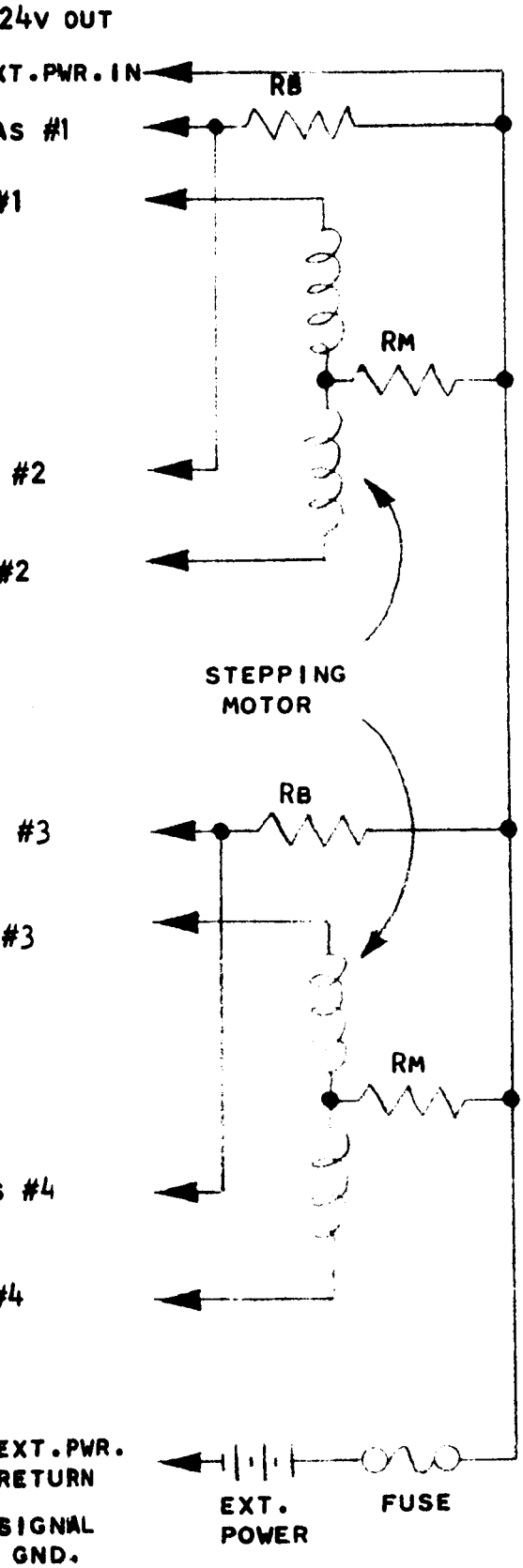
	REFERENCE DESIGNATION	DESCRIPTION
INTEGRATED CIRCUITS	IC 1,5,16,17,33,42	SN74LS04N
	IC 2,23	SN74LS20N
	IC 3,54	SN74LS27N
	IC 4,32	SN74LS11N
	IC 6-9,15,27	SN74LS38N
	IC 10,11	SN74LS139N
	IC 12,44	SN74LS10N
	IC 13,28,[illegible],31,38,52,55	SN74LS02N
	IC 14	SN7417N
	IC 18-21,56-58,63	SN74LS193N
	IC 22	SN74LS30N
	IC 24,51	SN74LS76N
	IC 25,43,53,30	SN74LS00N
	IC 26,29,34,64	SN74LS32N
	IC 35	SN74LS74N
	IC 36,45,46	SN74LS85N
	IC 37,41	SN74LS123N
	IC 39,50,65	SN74LS08N
	IC 40	SN74LS51N
	IC 47,49	SN74LS191N
	IC 48	MC1408/6
	IC 59,60	8038
	IC 61	SN74LS37N
	IC 62	SN74LS86N
	IC 66	MC681P
	IC 67-70	4N28
TRANSISTORS	Q 2	2N3641
	Q 3,5,7,9	2N5370
	Q 4,6,8,10	D44H11
DIODES	CR 1-3,9-20,24-28	1N914
	CR 5,6,7,8	1N4003
	CR 21,22	1N5245
	CR 23	1N4001
	CR 29,30	1N5223
RESISTORS (ALL ¼W 10% EXCEPT WHERE INDICATED)	R 7-9,35,39,40,47,58,59,86,87, 105,111,116,117	10K
	R 10-12	560
	R 13	470
	R 14,15,22,57	3.3K
	R 17,21,48,49,52,53,100,101,109, 110	2.2K
	R 23	6.8K
	R 24,46,60,81,88,93,94,96,98,106	4.7K
	R 30-34,89,103,112,113	150
	R 37,107	15K
	R 36,114,115	22K
	R 41,62	82K
	R 44	330
	R 63	680
	R 55	100K
	R 64,68,72,76,80,85	1K

RESISTORS CONT'D	REFERENCE DESIGNATION	DESCRIPTION
	R 65,69,73,77,109,90	220
	R 66,74	1.5K ½W
	R 67,71,79,75	680 2W
	R 92,95	330 ½W 5%
	R 104	47K
CAPACITORS	C 4-6,11,13	.0022UF
	C 8	47PF
	C 10,18-20,28,34,35,38,64,65	.01UF
	C 12,14,27,62,63,22,21	1000PF
	C 16,58,60	220PF
	C 23,61	470PF
	C 26	.05UF
	C 39,40,42-54	.1UF
	C 41,56,59	15UF
POTS	R 35	XXXXX ET34P103-10K
	R 56,38	PIHER - 100K
	R 102	ET34P102 - 1K
FUSES	F 1-2	3 AMP
INDICATORS	I 106	TIL209
CONNECTOR	J 1	CANNON DD50P OR EQUIV.

TYPICAL APPLICATION, MODEL SMC

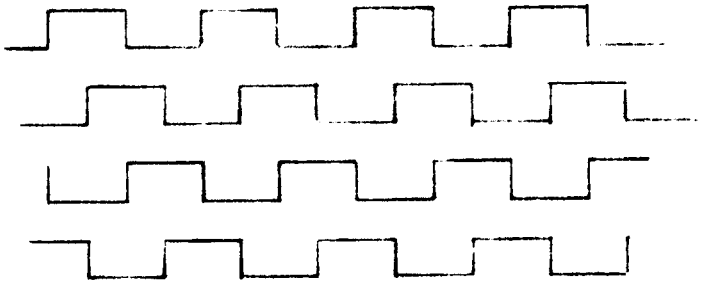


CATION, MODEL SMC-L

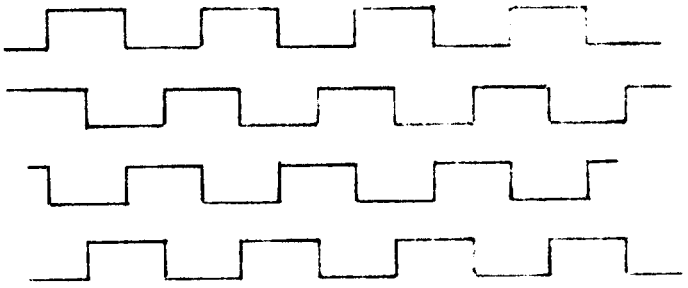


TYPICAL WAVE SHAPES

CLOCKWISE ROTATION



COUNTERCLOCKWISE ROTATION



$$R_M = \frac{V_{EXT.} - V_{MOTOR}}{I_{MOTOR}}$$

IF I MOTOR IS GREATER THAN 4 AMPS

$$R_B = \frac{V_{EXT}}{I_{MOTOR}/20}$$