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FROM: C NEUMEYER
SUBJECT: CHI MODELING RESULTS AND RECOMMENDATIONS

Summary

A simulation model of the CHI system was developed using the transient analysis program PSCAD. The results suggest that some improvements can be made to reduce the voltage overshoot/oscillation and the potential for noise generation in instrumentation.

Summary conclusions are as follows:

1) There are no major defects in the circuit layout as it stands. Voltages are within range of those anticipated by the system design. However, stray parameters cause voltage overshoot and oscillation, which can lead to noise problems.

2) The line to line surge suppressors are the most effective way to clamp the voltage produced by rapid variations in the impedance of the CHI plasma. However, as presently configured, there is too much inductance between the VV and the suppressors assembly. It is connected via a 25' length of #2 cables, then the main CHI bus run for 16', then the new CHI disconnect/ground switch, then a 10' length of 500MCM cables to the ring bus. A coax cable connection, and a shorter length, would be better by an order of magnitude. The coaxial connection should be made directly at the machine, despite the need for occasional disconnection for line-to-line hipot testing. The suppressor assemblies should be located as close to the machine as practical so as to minimize the impedance of the leads.

3) The conduction duty of the line-to-line suppressors needs to be monitored so that we can determine how much energy is being dissipated during CHI operation. In the case of an extreme event where the CHI plasma goes to an open circuit after conducting 50kA, then the energy which must be absorbed by the suppressors (mainly due to FCPC inductors) is of order 100kJ. The banks are rated 300kJ. During an actual pulse, depending on the CHI behavior, the suppressors are probably conducting regularly at some level and duty cycle TBD. We need to confirm that they are not on the verge of being overloaded. Current monitoring would be desirable, but not practical if the assemblies are located close to the machine. Therefore high bandwidth voltage monitoring can be used to ascertain the conduction duty.

4) The extent to which the Class 3 and Class 4 instrument racks follow the transient behavior of the VV depends on the stray impedance in the connection from the VV to the racks, and the stray capacitance from the racks to ground from all sources. This factor is important in the context of instrumentation noise. The most likely sources of stray capacitance are the main 75kVA 480/480V isolation transformers, which are not designed specifically for noise suppression. It may be desirable to replace these with special transformers with Faraday shields between primary and secondary windings. The need for this can be assessed by measuring the primary to secondary capacitance and comparing the existing value to that obtainable using specialized transformers. An additional stray capacitance to ground arises from the rack chassis to the reinforced concrete. This can be minimized by removing the bottom panels and possibly raising the racks (e.g. by inserting 1/4" G-10 instead of the existing 1/16" material). The inductance of the common connection to the racks can also be minimized by replacing the #2 cable with flat bus bar run along the floor, but carefully insulated from the floor.

5) Because the capacitances from each pole of the circuit to ground are approximately equal, the voltage of each pole to ground will tend to be equal under AC conditions, compared to the imbalance which we are trying to impose via the unequal grounding resistors, which are effective under DC conditions only. Therefore it is unrealistic, especially with CHI, to expect that the outer VV will not reach or exceed the full power supply voltage, unless the grounding is relocated to the test cell and lowered in its impedance value. Therefore it is very important to recover the ability of both poles of the circuit to withstand a 3kV hipot.

6) The line-to-ground surge suppressor seems to be less important than the line-to-line, but the simulation modeling does not properly handle the skin effect in the cable runs to the FCPC ground so this result may be misleading. Line-to-ground protection is prudent, of course, but the voltage rating of the suppressor must be ≥1kV. Otherwise it will become a second ground fault in case of an initiating ground fault on the other line. The line-to-ground suppression should be reconnected in the same fashion as the line-to-line suppression using coax cable.

7) An alternative grounding scheme would consist of a single resistor connected from the outer VV Class 4 terminal to ground in the test cell, with a current transformer to measure the ground current. The effectiveness of the grounding increases as the resistance is lowered, but the prospective power in a single ground fault increases. With the 1kV power supply the present system allows 1kV^2/1kΩ=1kW. A value of 10Ω would be very effective in limiting the outer VV potential while still limiting the fault power to 100kW. While the higher prospective fault power would be a disadvantage, the tighter control of the voltage would alleviate the need to clear the existing leakage faults on the outer VV, and might reduce the noise problem as well. If the grounding resistor is added then the

line-to-ground suppressor can be retained as a back-up in case of an accidental open circuit in the grounding resistor.

Summary recommendations are as follows, in order of priority:

1) Change the line-to-line and line-to-ground surge suppressor connections to coaxial cable and relocate the assemblies closer to the machine.

2) Put procedures in place to verify the integrity of the line-to-line and line-to-ground suppressors after restoration following each hipot, prior to any CHI operations.

3) Redouble efforts to increase the outer VV hipot capability to the originally intended 3kV.

4) Purchase and install MHz bandwidth voltage dividers to measure voltage to ground from inner Class 3 and outer Class 4 VV electrodes (it may be possible to use spare Ross Engineering units from FCPC or NBI).

5) Remove the bottom panels from the Class 3 and Class 4 racks, and try to increase gap to floor to 1/4".

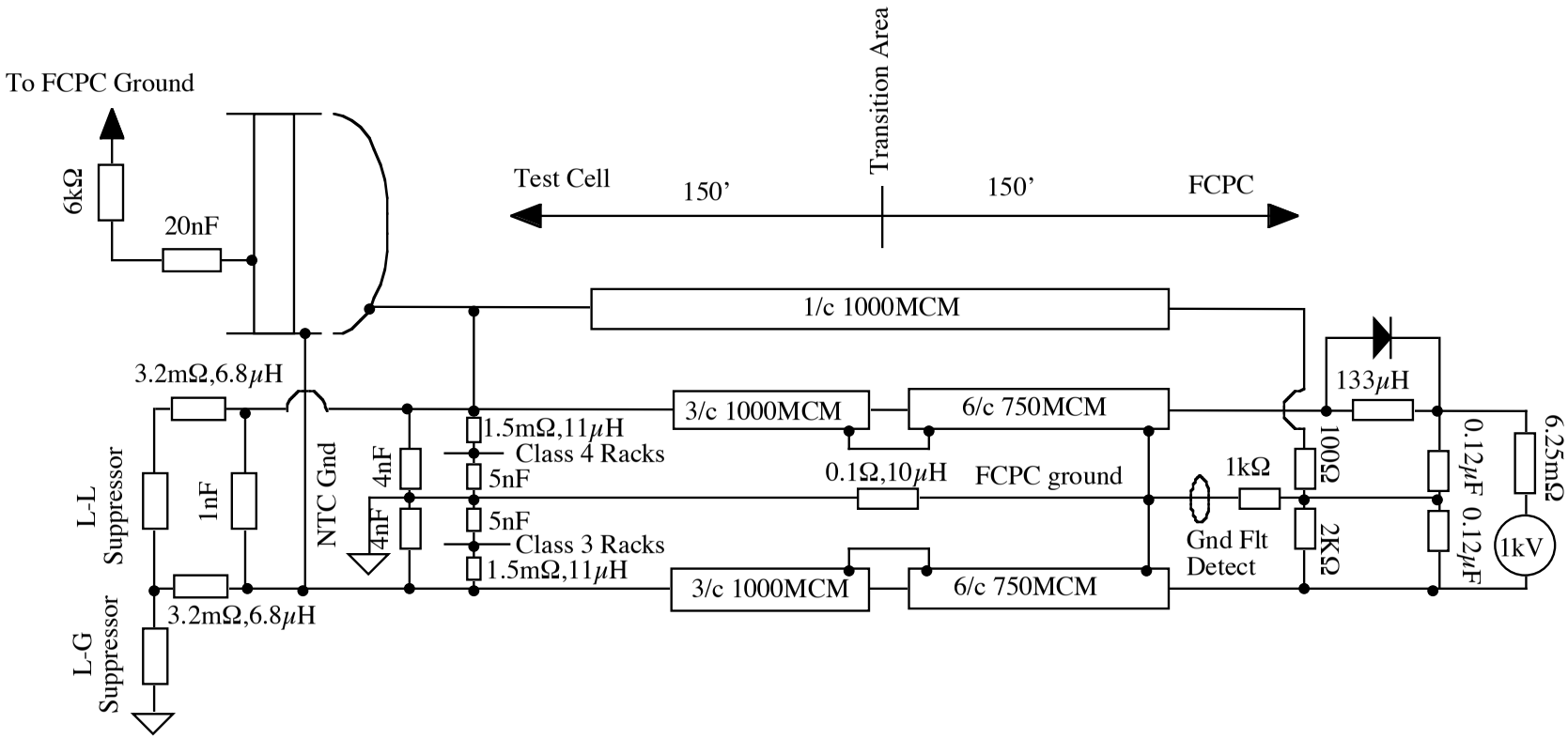
6) Design a new 10Ω grounding scheme to be located in the test cell close to the machine with current sensing for ground fault detection.

7) Measure the primary to secondary capacitance of the 480V/480V, 75kVA isolation transformers. If it is significantly larger than that obtainable by special noise suppression design, purchase replacement transformers.

8) Re-route the common connections to the Class 3 and Class 4 racks using flat bus, insulated from but routed along the floor.

Simulation Model

The main elements of the simulation model are shown in the following figure.


To FCPC Ground
6kΩ
20nF
Test Cell
150'
Transition Area
150'
FCPC
1/c 1000MCM
3.2mΩ,6.8μH
133μH
3/c 1000MCM
6/c 750MCM
1.5mΩ,11μH
Class 4 Racks
5nF
0.1Ω,10μH
FCPC ground
1kΩ
100Ω
0.12μF
6.25mΩ
L-L Suppressor
1nF
NTC Gnd
4nF
4nF
5nF
Class 3 Racks
1.5mΩ,11μH
Gnd Flt Detect
2KΩ
0.12μF
1kV
3.2mΩ,6.8μH
L-G Suppressor
3/c 1000MCM
6/c 750MCM

The power supply is represented as a simple 1kV voltage source with internal impedance such that the short circuit current is 120kA. The stray capacitance to ground from each terminal of the power supply to ground is 0.12μF, based on previous measurements. The 265μH inductors in each of the two parallel branches are represented by one 133μH inductor, with parallel freewheeling diode. The grounding resistors are connected to the FCPC ground which is connected to the NTC ground via an impedance. The resistance value is based on ground grid measurements made in 1984. The various cable runs are each represented by two series lumped RLC sections, which include the shield and mutual inductance between the main conductor and shield. The shields are grounded at the FCPC end only. The Class 3 and Class 4 racks are attached to the (+) and (-) poles via 25' of #2 conductor, approximately 8' above ground level, and the corresponding inductances and resistances are as indicated. A 5nF capacitance from the racks to ground is assumed (this could arise, e.g., from the AC isolation transformer). Stray capacitances of 4nF to ground are assumed from the inner and outer VV. The surge suppressors are connected via a 25' length of #2 cables, then the main CHI bus run for 16', then the new CHI disconnect/ground switch, then a 10' length of 500MCM cables to the ring bus. The calculated impedance is as indicated in the figure. The stray capacitance from the inner VV (and the OH ground plane, to which it is tied) to the OH coil copper is estimated to be 20nF and is effectively connected to the FCPC ground through two parallel 10kΩ resistors and one series 1kΩ resistor, amounting to 6kΩ.

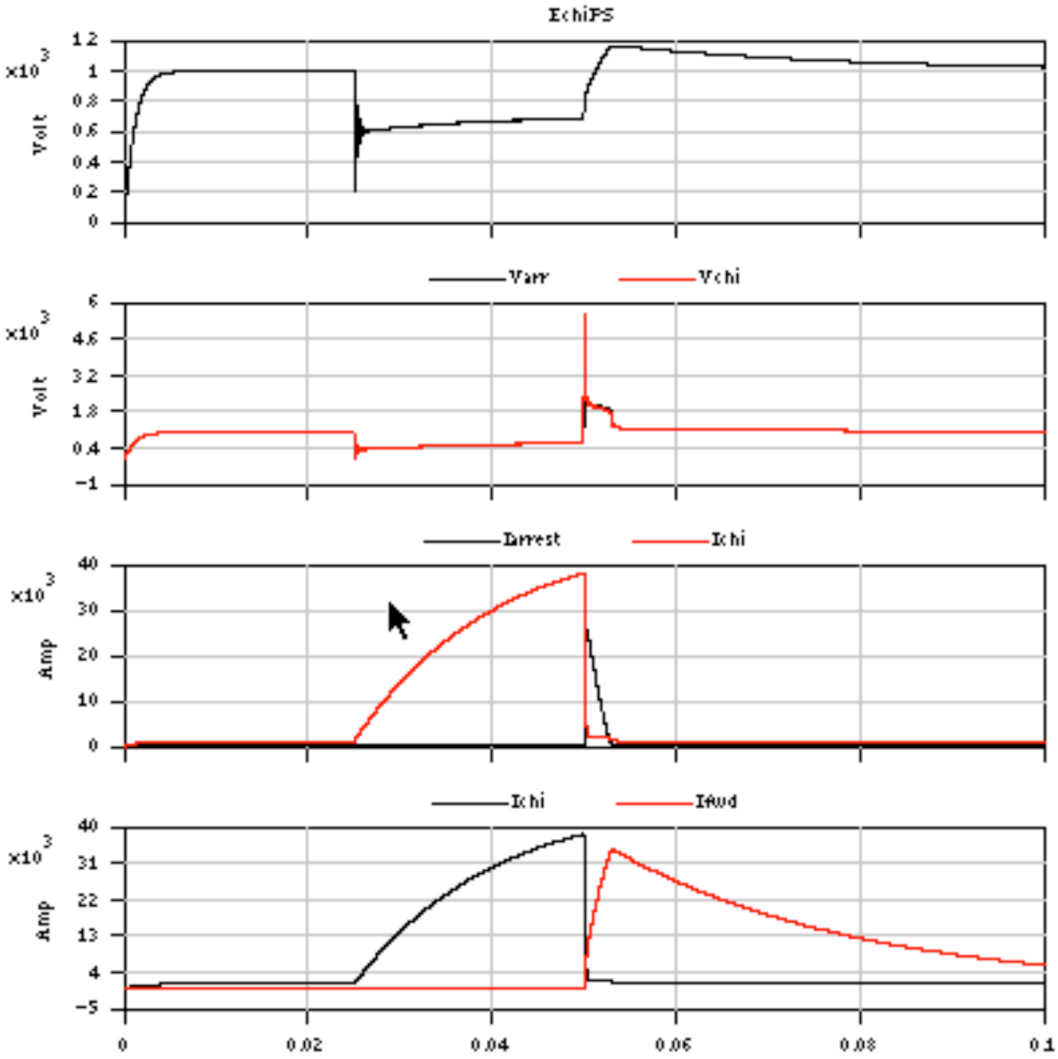
The CHI plasma is modeled as a inductance of 10^2*1μH = 100μH, accounting for a plasma inductance of order 1μH and the 10:1 ratio of I_p to I_{chi}, and a switched series resistance. The closed switch resistance is set to 13.75mΩ in order to draw around 50kA from the power supply. The open switch resistance is set to 1Ω. This is a somewhat arbitrary value aimed at generating a voltage spike across the VV terminals. Actual CHI behavior is much more complex, of course, but this is thought suitable to demonstrate the basic circuit behavior. In actual practice, as measured, the voltage across the VV terminals is highly transient, due to high frequency fluctuations in the inductance and/or resistance.

The simulation is considered to be semi-quantitative, in that it represents the CHI plasma behavior in a crude way, it approximates many of the circuit parameters, and it does not account for the skin effect on the conductor resistance, which will result in much greater damping but also more voltage overshoot in some situations.

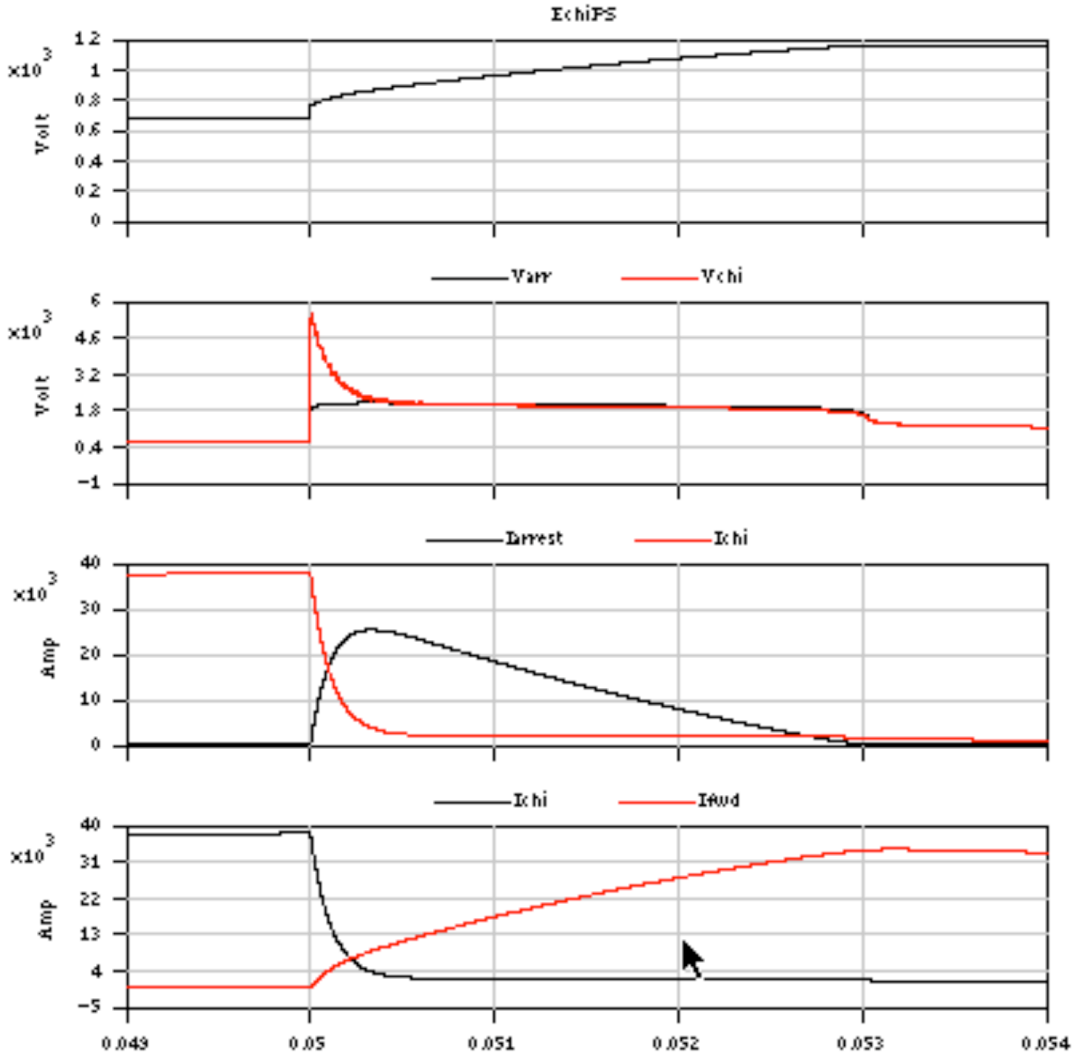
Nevertheless, the simulation does provide some insight into the overall circuit behavior.

Simulation Results

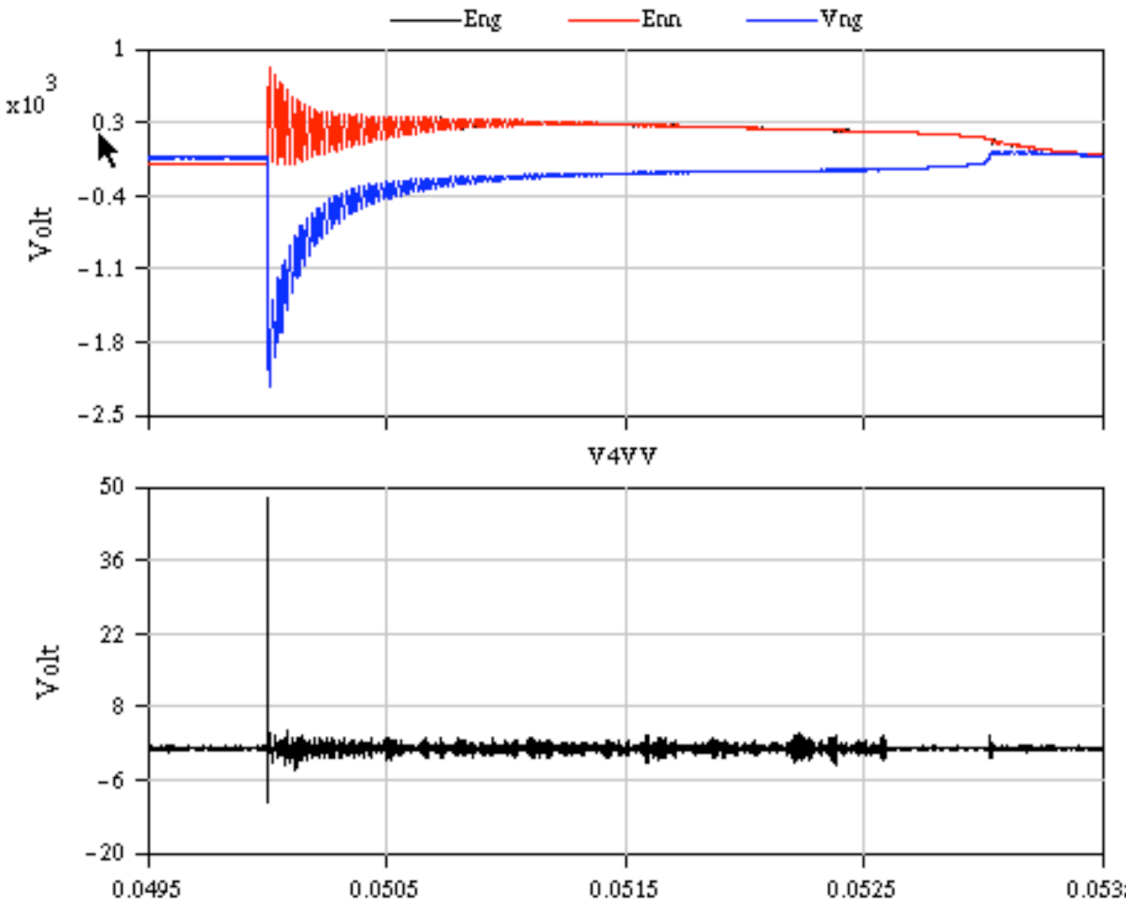
Selected results are given in the following figures, most of which depict the time window when the CHI plasma "switch" is attempting to open the circuit.



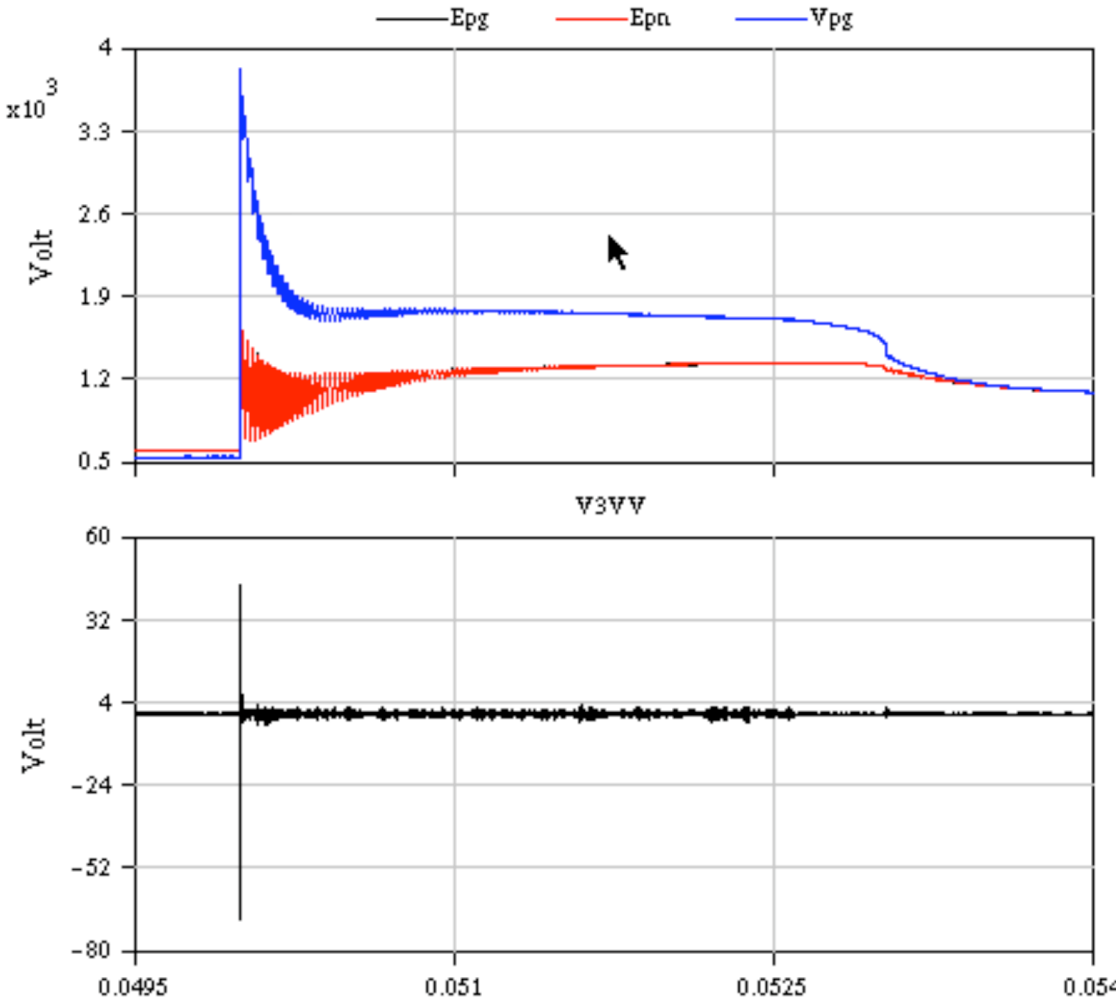
Overall simulation window showing CHI current initiation and interruption
(Note: high voltage spike is fictitious, for demonstration purposes only)



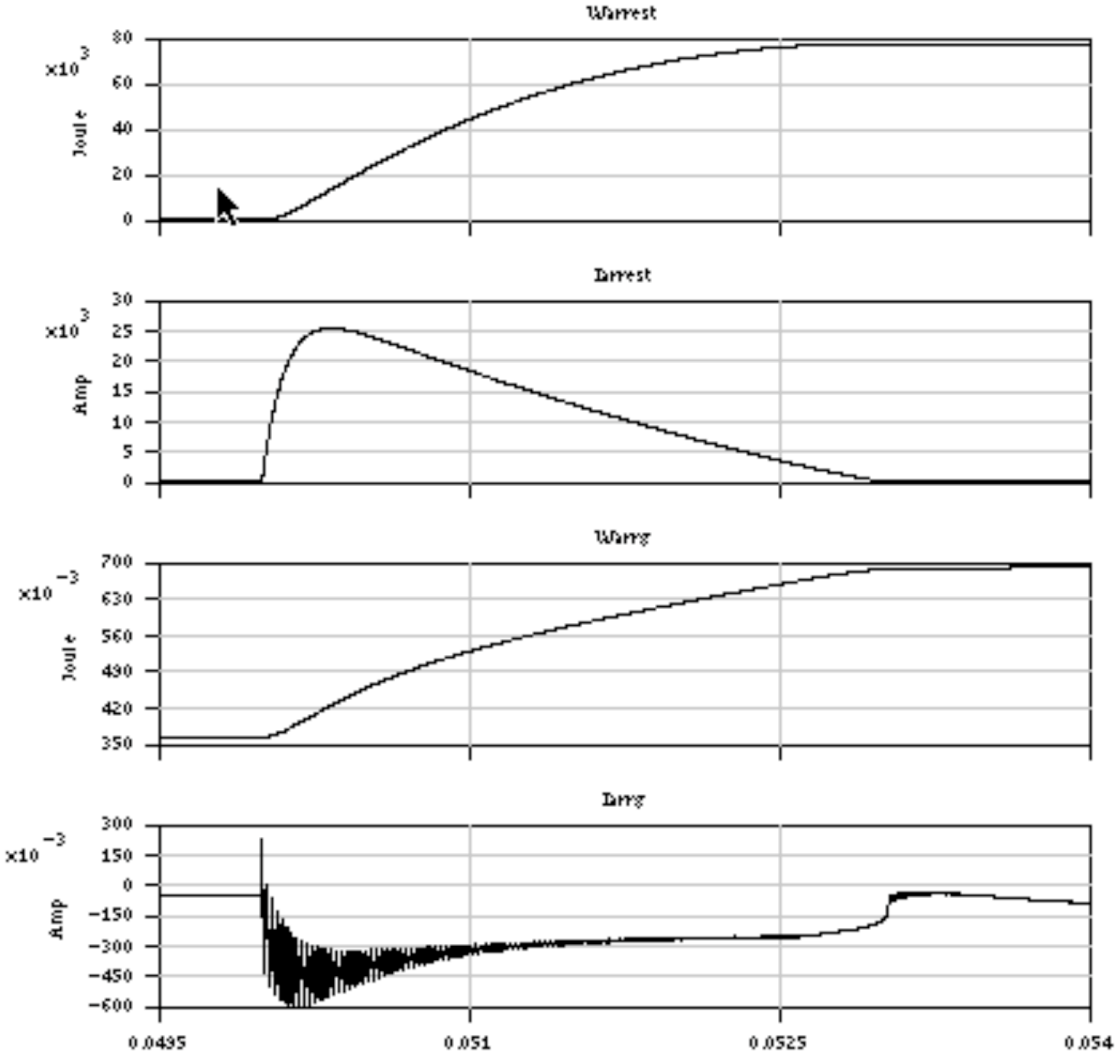
Zoom view showing CHI current interruption
(Note: high voltage spike is fictitious, for demonstration purposes only)
Current commutates from CHI plasma into arrester, then into freewheeling diode



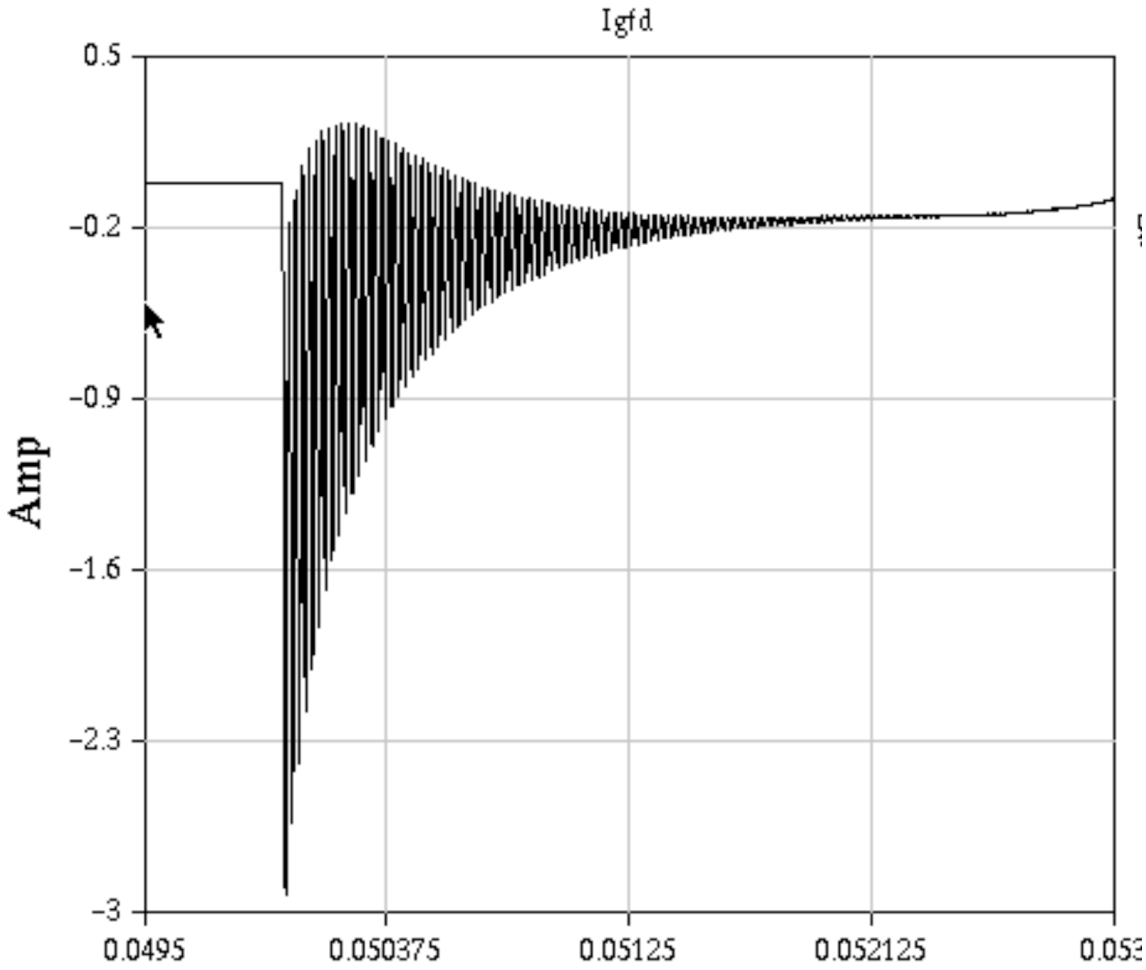
Zoom view during CHI current interruption shown negative pole (outer VV) voltage to neutral (Enn) and to ground (Eng) at FCPC and voltage to ground at VV (Vng) in NSTX Test Cell, along with voltage between Class 4 racks and outer VV
(Note: high voltage spike is fictitious, for demonstration purposes only)



Zoom view during CHI current interruption showing positive pole (inner VV) voltage to neutral (Epn) and to ground (Epg) at FCPC and voltage to ground at VV (Vpg) in NSTX Test Cell, along with voltage between Class 3 racks and outer VV
(Note: high voltage spike is fictitious, for demonstration purposes only)



Zoom view during CHI current interruption showing line-line and line-ground suppressor loading



Zoom view during CHI current interruption showing ground fault detector current

Cc:	M Bell	R Raman	T Jarboe	B Nelson	M Schaffer
	S Ramakrishnan	R Marsala	D McBride	H Schneider	D Mueller
	J Menard	D Gates	M Ono	R Kaita	A VonHalle
	M Williams	E Synakowski		M Peng	R Maingi