22-020628-CLN-01

TO: DISTRIBUTION
FROM: C NEUMEYER
SUBJECT: TASKS RELATED TO CHI ABSORBER FIELD NULLING SYSTEM

This memo lists tasks associated with the implementation of the CHI Absorber Field Nulling system, along with action items and a schedule.

Comments and estimates of resource requirements (man-days, M&S costs) are hereby requested.

1.0 Requirements **ACTION: R Raman**
- 1.1 Provide a written statement of the requirements in concise form, e.g. purpose and justification, field to be produced by each coil at a particular location B(r,z), and ramp rate requirement.

2.0 Coil and Mounting Structure Description **ACTION: C Neumeyer**
- 2.1 Provide a description of the coils in a format amenable to analysis (Rcenter, Zcenter, ΔR, ΔZ, #turns, conductor dimensions (width, height, corner radius, cooling hole diameter)
- 2.2 Provide a description of the additional structure which is relevant to EM analysis (dimensions, materials)

3.0 EM Analysis **ACTION: C Neumeyer**
- 3.1 Calculate coil inductances (including mutual inductances with other NSTX coils) and coil resistances
- 3.2 Evaluate eddy current effects and confirm that coils meet requirements for B(r,z)
- 3.3 Calculate induced voltages in coils due to NSTX operations and confirm compatibility
- 3.4 Calculate axial forces on coils including effects of other NSTX coils

4.0 Structural Analysis **ACTION: I Zatz**
- 4.1 Determine adequacy of structural supports vs. axial forces

5.0 Power Supply Design
- 5.1 Provide detailed information (operating manuals, schematics, etc.) of IGBT/Cap bank to be supplied by U of Washington. **ACTION: R Raman**
- 5.2 Perform electrical analysis including determination of requirements of cap bank charging power supply. **ACTION: C Neumeyer**
- 5.3 Develop overall electrical schematic including disconnect/grounding switches, grounding, current measurements, voltage measurements. **ACTION: S Ramakrishnan**
- 5.4 Develop physical design including equipment location, cabling design. **ACTION: S Ramakrishnan**

5.5 Develop interlock design and incorporate interlocks with existing FCPC and NSTX interlock systems. **ACTION: S Ramakrishnan**

6.0 Cooling System Design **ACTION: M Kalish**

6.1 Determine temperature distribution during bakeout (coils and O-rings must be maintained below 150°C, while inboard divertor tiles, mounted on CS casing flange, must be baked to 350°C).

6.2 Determine required cooling water flow rates and pressure drops.

6.3 Develop design for additions and modifications to existing system, including cooling hose selection and routing, changes to existing manifolding

6.4 Provide additional flow switches and PLC interlock monitoring

7.0 I&C

7.1 Determine I/O requirements and control algorithms. **ACTION: R Raman**

7.2 Determine appropriate host for control (e.g. SKY computer or other). **ACTION: R Marsala**

7.3 Develop control software. **ACTION: D Gates**

7.4 Implement control and I/O hardware and integrate with existing NSTX systems including data aquisition. **ACTION: R Marsala**

7.5 Develop coil protection system and integrate with existing NSTX systems. **ACTION: R Marsala**

8.0 Design Integration ACTION: C Neumeyer

8.1 Conduct design reviews of various parts

8.2 FMEA

Tentative schedule for the tasks, in order to be ready for NSTX operations restart in December '02, and field nulling power supply operations in March '03, is given in the following figure.

cc:

M Bell	J Chrzanowski	T Egebo	D Gates	M Kalish
R Marsala	M Ono	M Peng	S Ramakrishnan	
R Raman	A Von Halle	M Williams	I Zatz	

		July	Aug	Sept	Oct	Nov	Dec	Jan	Feb	March
Milestones										
Nulling Coils Installed			X							
NSTX Operations Started							X			
CHI Field Null Coil PS Energization										X
1.0 Requirements	Raman	X								
2.0 Coil/Structure Description	Neumeyer	X								
3.0 EM Analysis	Neumeyer	X								
3.1 R&L Calc	Neumeyer	X								
3.2 Eddy Current Analysis	Neumeyer	X								
3.3 Induced Voltage	Neumeyer	X								
3.4 Axial Forces	Neumeyer	X								
4.0 Structural Analysis	Zatz		X							
5.0 Power Supply Design										
5.1 IGBT/Cap Bank Info	Raman	X								
5.2 Electrical Analysis	Neumeyer		X							
5.3 Schematic	Ramakrishnan		X							
5.4 Physical/cabling	Ramakrishnan			X	X	X				
5.5 Interlocks	Ramakrishnan				X	X	X	X	X	
6.0 Cooling	Kalish									
6.1 Temp Dist during Bakeout	Kalish	X								
6.2 Flow Rates/Pressure Drops	Kalish	X								
6.3 Plumbing	Kalish		X							
6.4 Flow switches/Interlocks	Kalish			X	X	X				
7.0 I&C										
7.1 I/O and Algorithms	Raman	X								
7.2 Determine control host	Marsala			X						
7.3 Control Software	Gates				X	X	X	X	X	
7.4 Control Hardware	Marsala			X	X	X	X	X		
7.5 Coil Protection	Marsala			X	X	X	X	X	X	
8.0 Design Integration										
8.1 Review Coil EM Analysis	Neumeyer		X							
8.2 Review Structural Analysis	Zatz		X							
8.3 Review PS Design	Ramakrishnan				X					
8.4 Review Cooling Design	Kalish		X							
8.5 Review I&C Design	Marsala					X				