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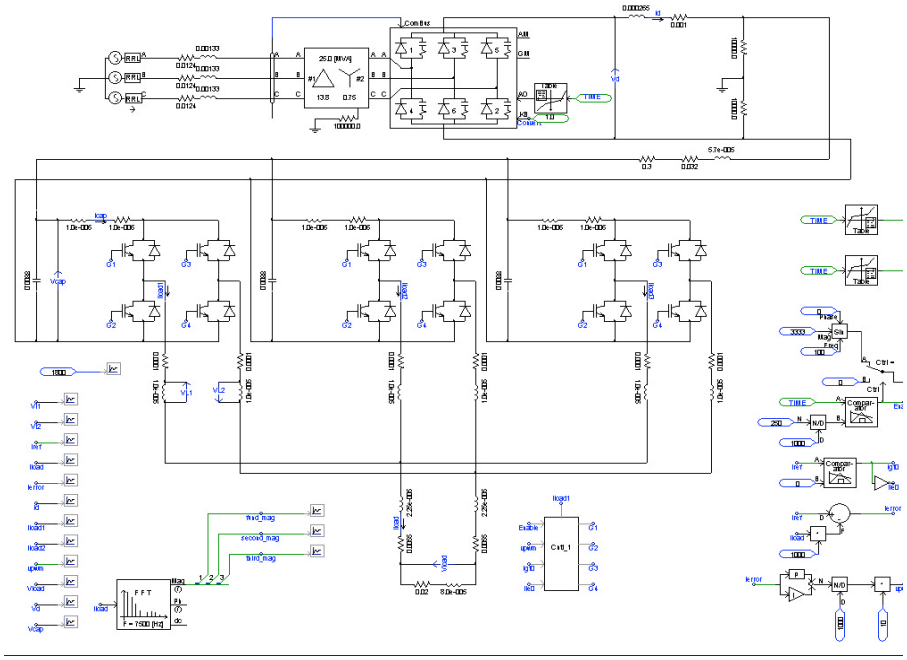
SUBJECT: SIMULATION OF RWM/FEC SPA, REVISED

Reference: 55_040206_CLN_01.doc "SIMULATION OF RWM/FEC SPA"

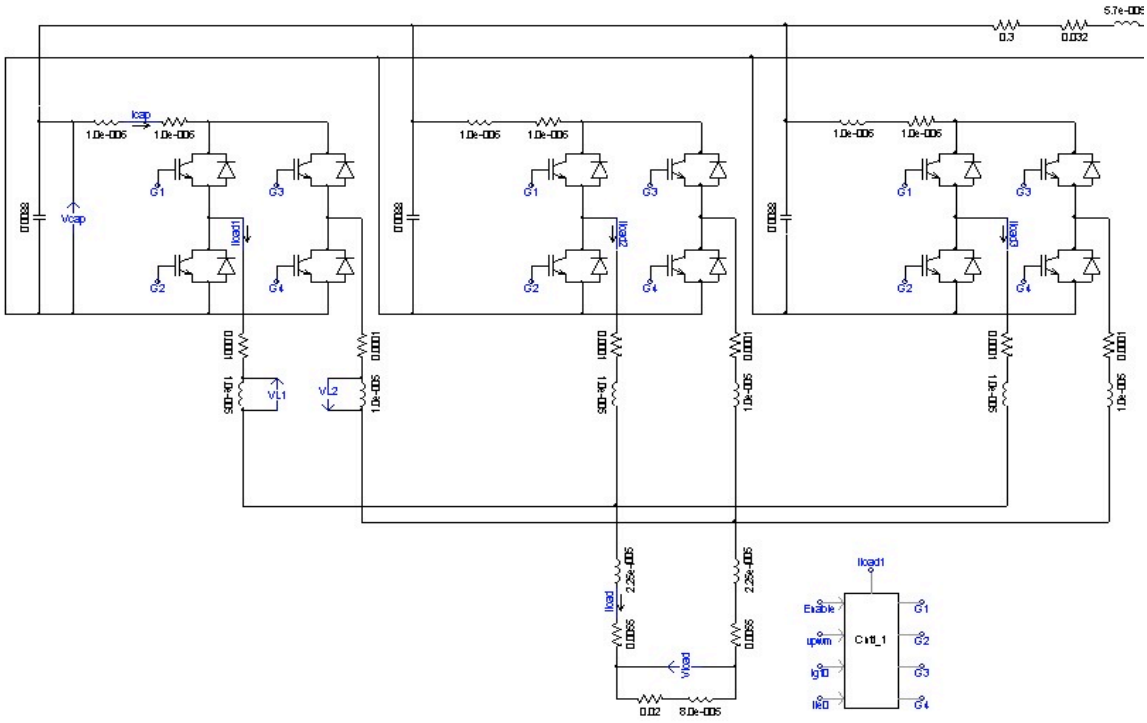
This memo presents results of a simulation of a Switching Power Amplifier (SPA) to be used for Resistive Wall Mode (RWM) and Field Error Correction (FEC). The simulation was performed using the Power Systems Computer Aided Design (PSCAD) software. Compared to the reference memo, this revision reflects a revised Pulse Width Modulation (PWM) scheme, revised feedback control scheme, and higher switching frequency.

MODELING

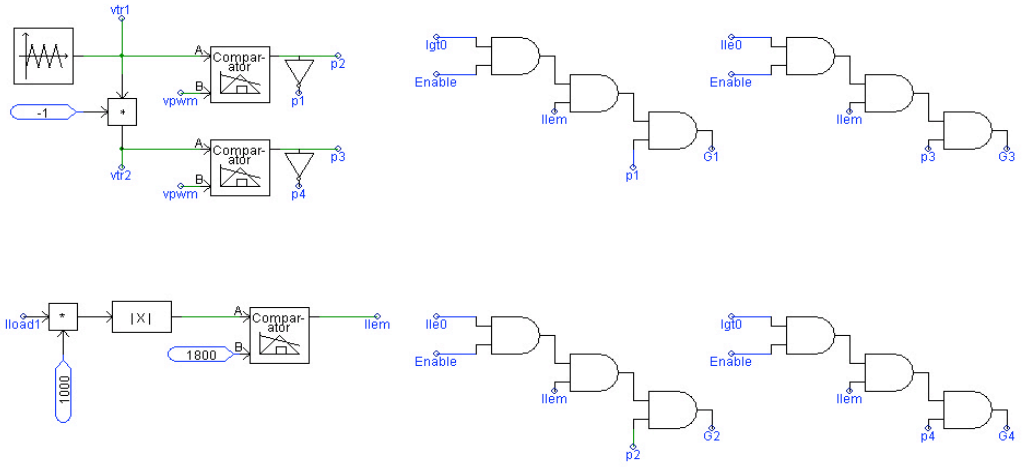
The overall PSCAD setup is shown in the following figure. One SPA, consisting of three parallel H-bridge choppers, is simulated, being fed from a Transrex 6-pulse rectifier through realistic cable impedances consistent with the SPA being located in the mezzanine of the Neutral Beam Power Conversion (NBPC) building. In addition, a 0.3 ohm series current limiting resistor is added to limit inrush current. In actuality, three SPAs would be fed, and the load on the Transrex would be 3x the amount simulated. However, the load is relatively low, and the voltage drop will be insignificant.



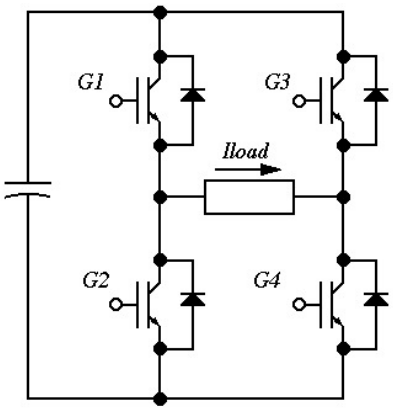
A zoomed view of the SPA model and load is given in the following figure. There are three parallel H-bridge choppers which operate simultaneously using an "alternate gating" control scheme such that individual IGBTs switch at 3.75kHz while the net voltage output switches at 7.5kHz. The 10μH inductors in each leg of each chopper output promote balance of the current between the parallel choppers which, ideally, switch at the same time but practically have some finite differences due to individual characteristics. The cable impedances which connect to the 20mOhm, 80microH load are realistic for the SPA being located in the NBPC mezzanine and the coils in the NSTX Test Cell (NTC). The block labeled "Cntl_1" provides the SPA IGBT firing pulse controls.



The control logic of Cntl_1 is shown in the following figure. Triangle waves "vtr1" and "vtr2" (180^{o} out of phase with vtr1) at 3.75kHz and their intersections with a PWM feedback control reference demand "vpwm" control the time at which IGBT firing pulses to p1, p2, p3, and p4 to the IGBTs should be issued. The vpwm signal is generated based on a proportional and integral (PI) control (G_P = 1.0 ohms, G_I=100.0 ohm/sec) on the current error. The firing pulses G1, G2, G3, and G4 will follow p1, p2, p3, and p4 depending on 1) enable signal, 2) polarity of load current, 3) IGBT current less than or equal maximum allowed (signal "ilem").



The utilization of the four H-bridge IGBTs to produce positive and negative voltage under conditions of positive and negative load current (4-quadrant operation) in the is explained by the following figure and table.



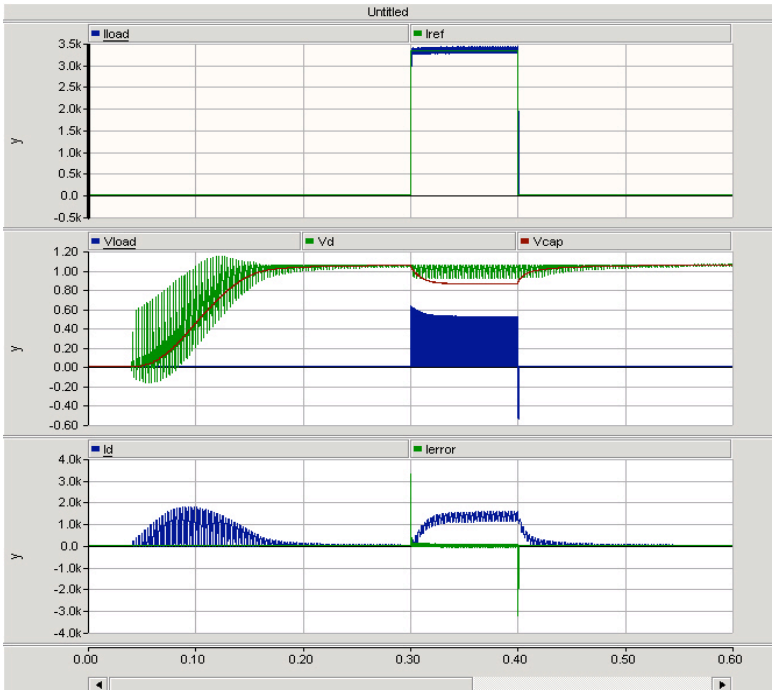
Iload	Vload	G1	G2	G3	G4
> 0	+	1	0	0	1
	0	0	0	0	1
	0	1	0	0	0
	-	0	0	0	0
< 0	+	0	0	0	0
	0	0	1	0	0
	0	0	0	1	0
	-	0	1	1	0

It is noted that, e.g., when the load current is positive, the switching between +V and 0 can be accomplished using either G1 or G4. By alternating the switching of G1 and G4 each at a frequency *f*, the net ouput frequency is 2*f*. This is the essence of the "alternate gating" scheme.

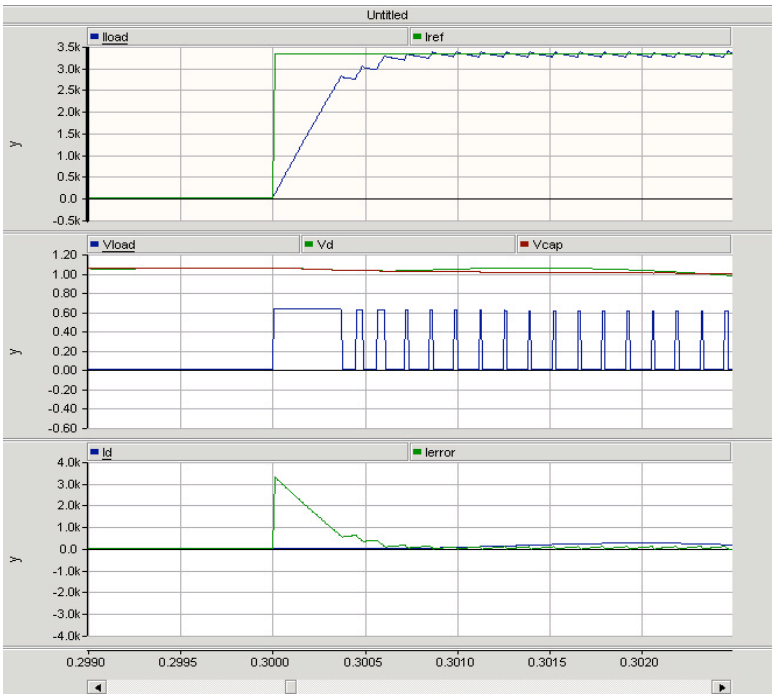
To test the SPA, its response to a square pulse, bipolar pulse, and 100Hz sine wave was simulated, in each case with a peak current of 3333A reference.

SQUARE PULSE RESPONSE

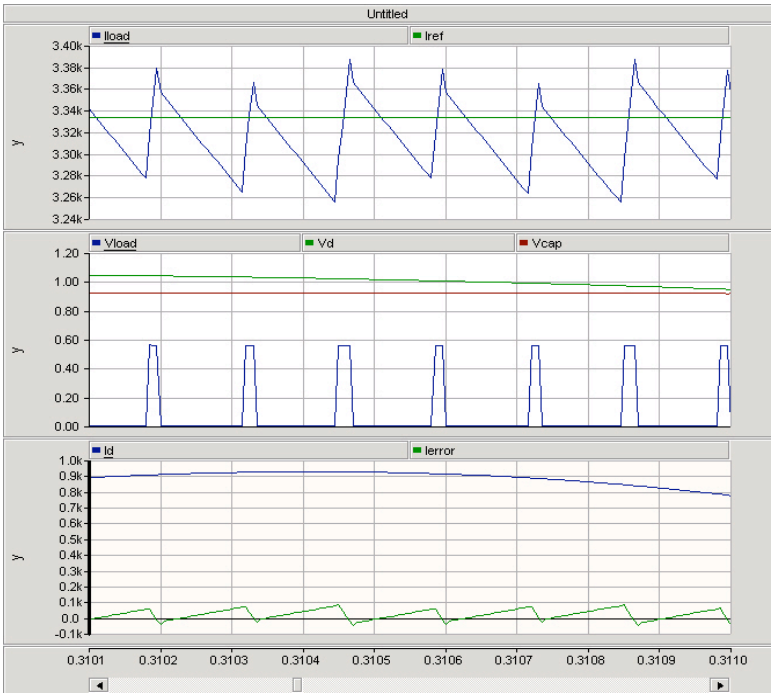
In the following figure, the top graph shows the load current Iload and reference current Iref. The next graph shows the Transrex output Vd, the SPA cap bank voltage Vcap, and the voltage on the 80microH, 20mOhm load coil. The next graph shows the Transex current Id (x3) and the error in the load current (Iref-Iload). The Transrex voltage was controlled by ramping the phase control signal a from 180^o to 0^o in 200mS. With the selected values of series resistor and SPA capacitance, the cap bank voltage drop under load is modest, and the Transrex inrush current and current during the SPA pulse are modest at around 2kA. This will permit the use of a relatively light cable. In addition, the maximum residual energy stored in the Transrex connection, which must be absorbed by the cap bank in case of a fault when the IGBTs are gated off, is relatively small, so the cap bank overvoltage is very limited. The energy W is $1/2LI^2$=0.5*265e-6*2e3^2=530J. The cap overvoltage is sqrt(2W/C+Vo^2)=sqrt(2*530/26400e-6+1e3^2)=20V. Finally, note that the maximum droop of the cap bank is approximately 100V.



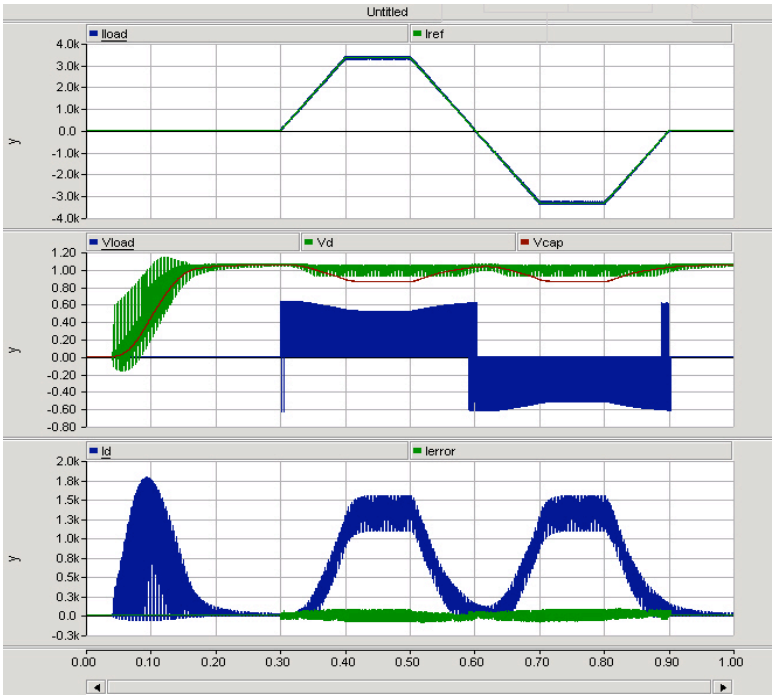
The following figure shows a zoom-in during the square pulse. The current rise time is less than 1.0mS.



The following figure shows a zoom-in of the flat top of the square pulse. The peak-peak ripple is 100A and the fundamental is at 7.5kHz.

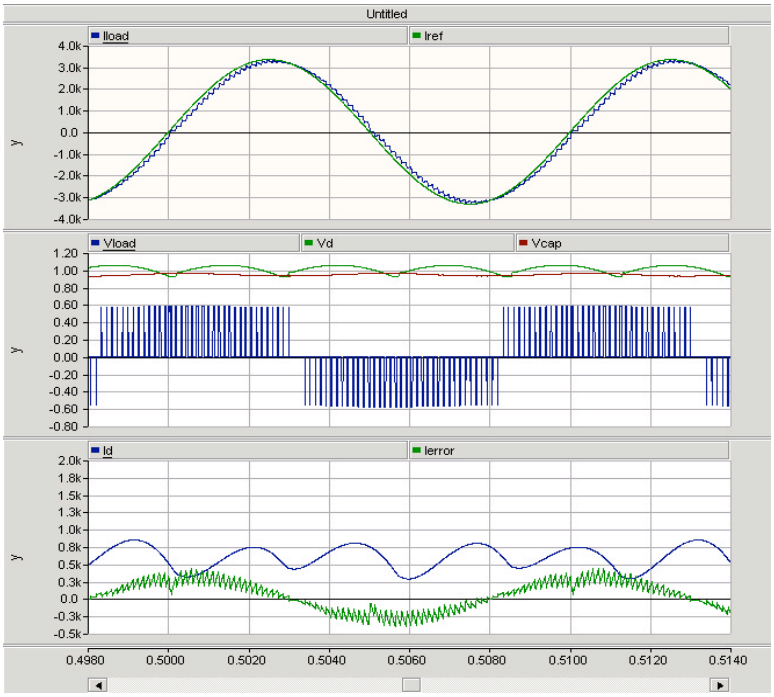


BIPOLAR PULSE RESPONSE

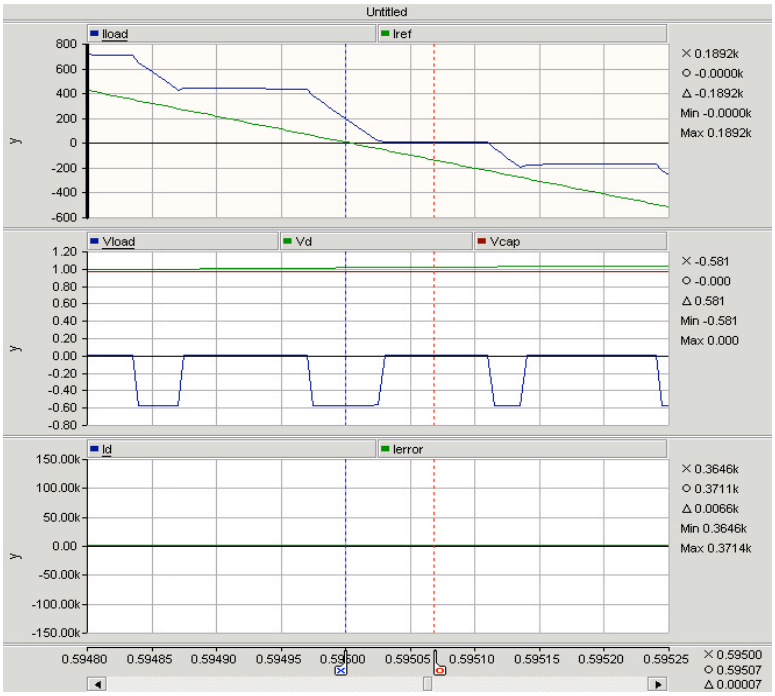


SINE WAVE RESPONSE

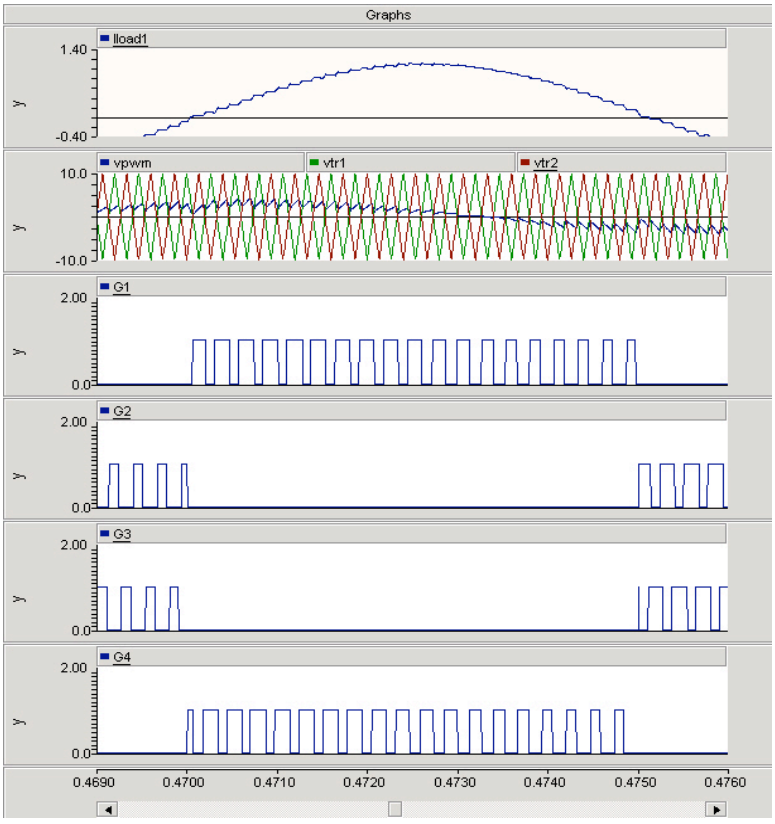
The following figure shows the sine wave case at 100Hz.

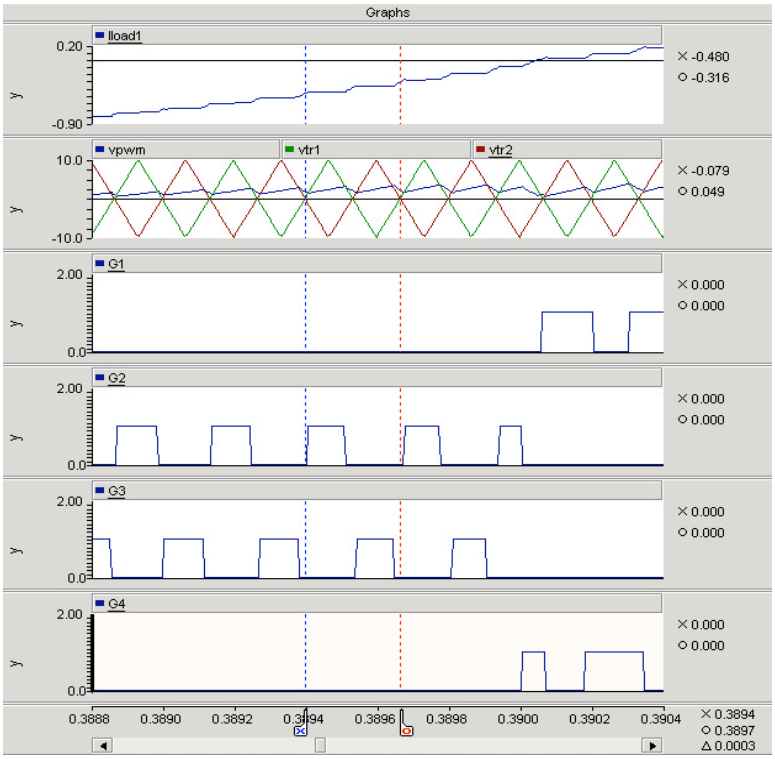


The following figure shows a zoom-in on the load current and the reference. The shift in their zero crossings is around 70 µS which amounts to 2.8^{o} at 100Hz.



The following figures show the PWM and gating signals.





CONCLUSIONS

Compared to the prior scheme investigated, the scheme described herein is superior in that it has less circuit inductance and higher switching frequency. This beneficially reduces the step response time, latency, and phase lag.

Cc:

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