71-000128-CLN-01

***TO: DISTRIBUTION***
***FROM: C NEUMEYER***
***SUBJECT: NSTX VOLTAGE ISOLATION***

***References:***

[1] 1X-980623-CLN-01, "Potentials of Machine Components", C. Neumeyer
[2] SR-180399-1, "CHI Ground Detection", S. Ramakrishnan
[3] CR-062, "CHI Power Loop Grounding Changes"
[4] SR-011100-1, "CHI Load Monitor", S. Ramakrishnan

The purpose of this memo is to revisit the requirements for voltage isolation and segregation of components associated with the center stack casing and outer vacuum vessel, and to recommend revisions to the requirements and other changes based on operating experience gained thus far.

Summary of Recommendations

*1) For all future operations, the CSC shall be biased above ground and the outer VV shall be held near ground by the resistor grounding network.*

*2) Future CHI operations shall be limited to 1kV.*

*3) The now floating group of components in the center stack (OH tension tube, PF1a and PF1b ground planes and coil holders, TF hub assemblies) shall be tied locally to the center stack casing on top and bottom using 10Ω resistors.*

*4) If the need to go to Vchi = 2kV is identified at a later date, then tests should be performed on a sample of 0.050" thick Scotchply and, assuming that sufficient dielectric strength is verified, the TF hipot level should be increased from 3kV to at least 4.5kV (safety factor of 1.5), preferably 6.0 kV (safety factor of 2.0).*

*5) Class 4 hipot requirement shall be reduced to 2*1+1=3kV. If the need for Vchi = 2kV is identified at a later date, the 3/2=1.5 safety factor can be accepted, since, except under fault conditions, the outer VV will stay near ground potential.*

*6) Requirement for special treatment (floating electronics racks and segregated wiring) of components connected to the outer VV shall be dropped, on the condition that the TFTR Ground Fault Monitor, or an equivalent device, be added to NSTX such that a horn is sounded in the NSTX Test Cell if a spurious conducting path is introduced from either the CSC or outer VV to ground.*

Background

The baseline design of NSTX reflects the requirements given in the GRD with regard to CHI operation (section 1.3.2) as follows….

*"The center stack casing and inner wall of the bore of the machine, including the inboard divertor plates, shall be electrically isolated from the remainder of the Vacuum Vessel to permit the biasing of this structure with respect to the Vacuum Vessel, to drive a poloidal component of plasma current. Both the center stack casing and the outer Vacuum Vessel shall be isolated from ground such that either one can be grounded during CHI operations, with the other biased at the CHI potential"*

The required level of isolation based on CHI operation up to 2kV was 2*2 + 1 = 5kV DC, imposed on the center stack casing and the outer vacuum vessel, between each other and to ground.

It was originally envisioned to run with the outer vacuum vessel (VV) at or near ground and the center stack casing (CSC) elevated above ground. Furthermore, it was planned to ground the OH coil ground plane (the electrostatic shield which surrounds the OH coil groundwall insulation), as well as the other isolated parts within the CSC (OH tension tube, etc.). However, in this configuration, the small annular gap between the CSC and OH ground plane was subject to the full CHI voltage. Further aggravating this condition was the fact that within the annular space were various diagnostics such as Ip Rogowski coils, flux loops and thermocouples, which were to be referenced to ground potential.

As time went on the concern about the annular region, and the severe impact to the NSTX program in case of a fault therein, led us to a preferred configuration whereby the CSC was held at or near ground while the outer VV was elevated above ground (ref. [1]). It was reasoned that, given the greater availability of space on the outside, it was easier to deal with the isolation requirement and, furthermore, should a ground fault occur, it would be easier to repair.

During the time of review of the Lower Dome Gas Injection system for CHI, however, concern developed that breakdown might occur on any of the many ceramic insulators associated with systems attached to the CSC and outer VV (gas injection lines, diagnostics, vacuum pumping duct, NBI, etc.) under certain combinations of voltage, gas pressure, and background magnetic field. The lower dome gas injection was rearranged to include a section of the foreline which was provided with a ceramic break and which could be pumped down to high vacuum conditions after loading in the gas to down stream storage chambers. An interlock on the gas pressure in this foreline volume was introduced so as to prevent application of power supply voltage if the region of the ceramic was not under high vacuum.

In response to this concern about inadvertent breakdown and a chit at the review, another meeting was held to review the CHI grounding and it was decided that the outer VV would be held near ground using the resistive

grounding scheme. Solid grounding was not selected because of the high current which would flow in case of a single ground fault, and also the desire to allow a small voltage to develop on the outer vacuum vessel for purposes of ground fault detection thereon. Furthermore, to alleviate the concern about voltage stress in the annular gap, it was decided to tie the OH ground plane to the center stack casing potential. This shifted the CHI voltage stress from the annular gap to the OH coil ground wall insulation (ref. [2], ref. [3]).

Prior to the first CHI operations, we discovered during VV hipot, high conductivity from the outer VV to ground. Much time and effort was spent to locate the source of this conductivity. It was finally attributed to the ceramic on the vacuum pumping duct. At this point, based on the fact that the outer VV would remain near ground, we elected to proceed with the first CHI operations. We noted that the low insulation resistance (1200Ω) from outer VV to ground would cause the background ground current during a pulse to be higher than originally anticipated, such that the sensitivity of the ground fault detection circuitry to a real ground fault would be reduced.

After the initial round of CHI operations a drop in the insulation resistance between the CSC and the outer VV from 10's of MΩ down to 300kΩ was noticed. This was attributed to the significant amount of arcing which characterized some of the initial CHI experiments. During the second round of CHI operations, better control of the background magnetic field along with the implementation of an arc detector feature in the software led to the gradual improvement in the resistance up to the level of several MΩ.

While troubleshooting the drop in insulation resistance from the CSC to the outer VV, it was noticed that whereas we had tied the OH ground plane effectively to the CSC, we have at present no definite connection for other components in the same vicinity which are at present "floating" together as a group. These include the OH tension tube (the OH ground plane only covers the outer diameter of the coil, not the inner diameter), the PF1a coil supports, PF1b coil supports, and the TF hub assemblies (refer to Figure 1 (NSTX EDC-1005)). While there is no definite connection, there are thermocouples glued to the surface of the PF1a coil which go back to the same electronics rack which services the diagnostics which surround the OH coil ground plane in the annular region. This situation presents somewhat of a dilemma, since, if we tie these parts to the CSC then the CSC potential will appear on the tension tube which faces the TF coil inner leg insulation, such that the 1kV TF insulation system must withstand Vtf + Vchi. On the other hand, if we tie these parts to ground to keep the CSC voltage off of the TF inner legs, we put an unintended stress between the PF1a coil holders and the OH ground plane, and across the surface of the OH coil from the ground plane on the outer diameter to the tension tube on the inner diameter. In addition, this would have the thermocouples attached to two different voltage levels.

Present Status

The present situation is depicted in Figure 2 and is described as follows:

• The grounding resistor network provides a voltage divider such that, nominally, 1kV * 10/(2000+10) ≈ 5 volts appears from the outer VV to ground when the CHI power supply is at 1kV. In practice there are voltage transients and capacitive effects which cause somewhat higher voltages. The pathway to ground is accomplished via a 1kΩ resistor, the current through which is measured and used for ground fault detection.

• The 1kV power supply, when configured with two power supply sections in parallel, has an equivalent series resistance of around 8mΩ and series inductance of 135$\mu$H. The resistance of the cable run from FCPC to the NSTX test cell is of order 1.9mΩ per leg. Thus the voltage V applied between the CSC and outer VV via the CHI bus in the NSTX test cell is equal to the 1kV power supply voltage minus the drop in its internal impedance and external circuit, including the cable run.

• The OH ground plane, which extends only around the outside of the OH coil, is connected to the CSC through 10Ω (this is shown for simplicity only on the bottom of the machine; in fact the ground plane is divided into upper and lower parts, each further divided into two parts toroidally. Each of these four parts connects to the CSC through 10Ω. The connections are made locally on the top and bottom of the machine to avoid excess loop inductance.

• The tension tube within the OH coil, and surrounding the TF coil inner legs, has at present, no fixed voltage reference.

• Class 4 diagnostics are those which are physically mounted on, and in some cases electrically connected to, the outer VV or internal hardware mounted to same. They go to dedicated electronics racks, and feed into high input impedance differential amplifiers. The common of the Class 4 racks are tied to the outer VV via a single cable. The Class 4 racks have a dedicated 120VAC feed through a high voltage isolation transformer as well as a low voltage (Topaz type) isolation transformers at each rack. The load side of the high voltage isolation transformer connects to the outer VV via a single cable at the CHI bus. There are four Class 4 racks at present.

• Class 3 diagnostics are those which are physically mounted on, but electrically insulated (< 1kV rating) from, the CSC. They go to dedicated electronics racks, and feed into high input impedance differential amplifiers. The common of the Class 3 racks are tied to the CSC via a single cable. The Class 3 racks have a dedicated 120VAC feed through a high voltage isolation transformer as well as a low voltage (Topaz type) isolation transformers at each rack. The load side of the high voltage isolation transformer connects to the CSC via a single cable at the CHI bus. There are two Class 3 racks at present.

• Class 2i diagnostics are those which are physically mounted on, but electrically insulated (< 1kV rating) from the OH ground plane. They go to a dedicated electronics rack, and feed into high input impedance differential amplifiers. Class 2i diagnostics were originally envisioned to be Class 2, i.e. ordinary diagnostics ground reference. When it was decided to tie the CSC to the OH ground plane these diagnostics became, essentially, Class 3. But it was decided to maintain the possibility of separating them at a later date. So, the "2i" Class was created. The common of the Class 2i rack is tied to the Class 3 rack common. The Class 2i rack shares its 120VAC feed with the Class 3 isolated system. There is only one Class 2i rack at present.

• All sensor wiring to the Class 2i, 3, and 4 racks is segregated into the three separate classes, each of which runs around the machine in a dedicated cable tray system.

• All data I/O transmitted to/from the Class 2i,3, and 4 racks is by fiber optics.

• Other auxiliary equipment which physically connects to the outer VV but which is at ground potential has a suitable ceramic break for voltage isolation. Related electronic racks are at Class 2 diagnostic common.

• Other sensors on outer VV side of ceramic break, which have rated voltage isolation, transmit signals to the Class 2 racks (at present, only 1 of these types exists).

• GDC/filament system (not shown) is treated same as Class 4 (it is fed by isolated AC power and all components including associated equipment rack is tied to outer VV potential).

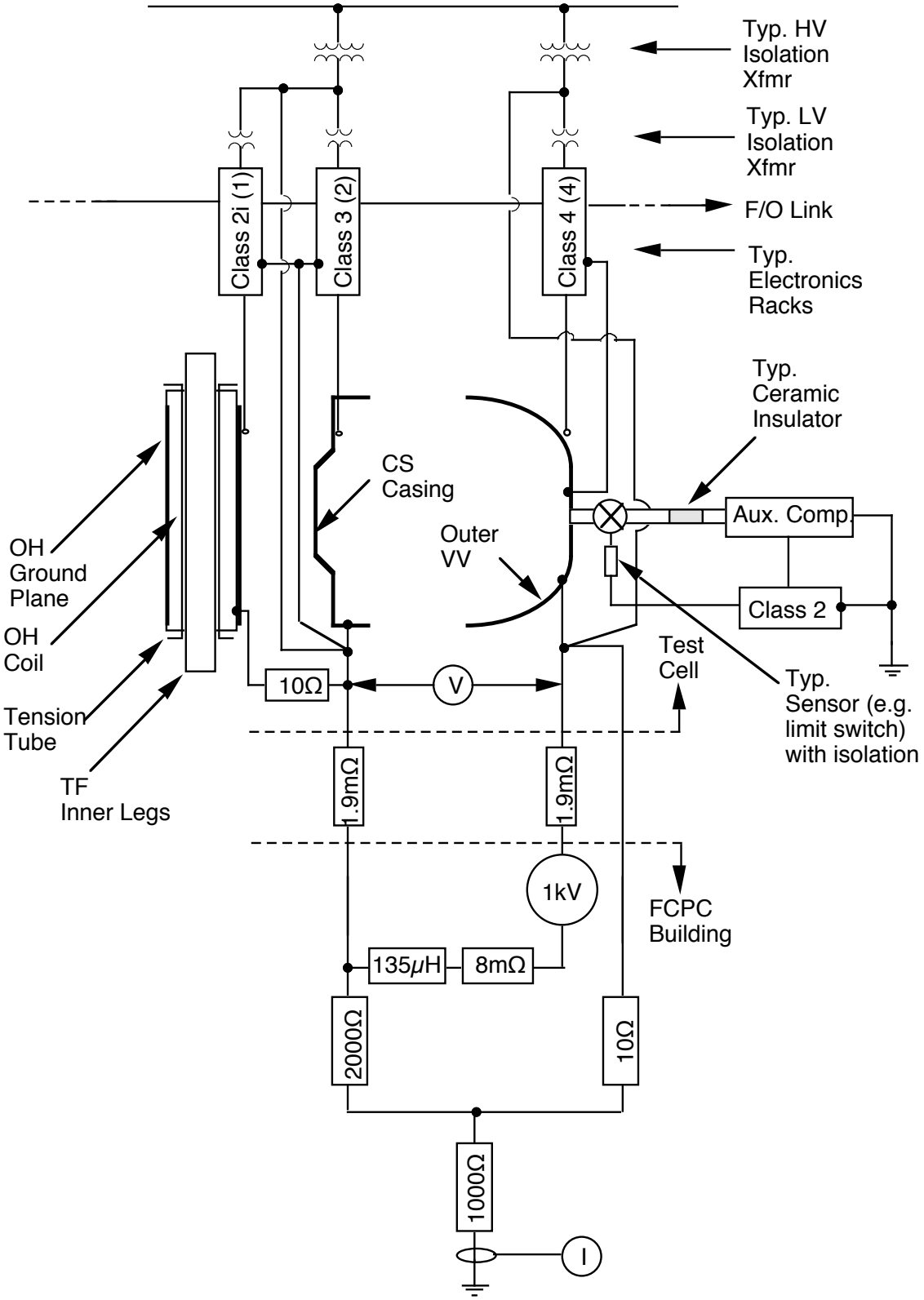
Typ. HV Isolation Xfmr
Typ. LV Isolation Xfmr
F/O Link
Typ. Electronics Racks
Class 2i (1)
Class 3 (2)
Class 4 (4)
Typ. Ceramic Insulator
CS Casing
Outer VV
Aux. Comp.
Class 2
OH Ground Plane
OH Coil
Tension Tube
TF Inner Legs
10Ω
V
Test Cell
Typ. Sensor (e.g. limit switch) with isolation
1.9mΩ
1.9mΩ
1kV
FCPC Building
135μH
8mΩ
2000Ω
10Ω
1000Ω
I

Figure 2

Issues and Recommended Solutions

1) CHI biasing

From a physics perspective, as long as a potential is applied between the CSC and outer VV, the relative voltage of these components to ground is irrelevant.

Because of the aforementioned issue of inadvertent breakdown across ceramics which connect from the outer VV to components at ground, of which there are many, it is undesirable to elevate the outer VV above ground. On the other hand the ceramics which feed the gas injection storage reservoirs at the CSC potential are evacuated and interlocked so as to prevent accidental breakdown.

*Therefore, for all future operations, the CSC shall be biased above ground and the outer VV shall be held near ground.*

2) Potentials of center stack components

Because of the concern about breakdown in the annular region between the CSC and the OH coil ground plane, the scheme which ties the CSC potential to the OH ground plane (through the 10Ω resistors) remains the preferred one.

The OH Tension Tube, PF1A and PF1B coil holders and ground planes, and the TF Hub Assemblies are all tied together due to their mechanical contact. However, at present there is no direct connection to any reference. But, the PF1A coils groundwalls do have thermocouples attached which go to the Class 2i rack.

It is recommended that a local 10Ω connection be put in place between the aforementioned group of items and the CSC, both top and bottom (even though the tension tube bridges between the top and bottom, for transients, the connection both above and below is preferred).

With this connection in place, the CHI voltage appears on the CSC, OH ground plane, OH tension tube, PF1a ground planes and coil holders, and the TF hub assembly. This situation was not intended in the original design (these parts were to be grounded). A consequence is that, while we gain by protecting the critical annular region, we lose by adding voltage stress to the OH, PF1a, PF1b, and TF inner leg groundwall insulations.

This situation is quantified in the following three tables, which assume the jumpering of the CSC/OH ground plane/OH tension tube/PF1a & 1b ground planes together, and which assume Vchi = 1kV. The tables indicate the voltage (kV) to ground on the various electrodes, and the voltage across the various elements which separate the electrodes. Two cases are included, one with the nominal voltage to ground on each coil terminal (with high resistance grounding it is equal to 1/2 of the line to line voltage) as well as those with a single ground fault on one terminal (the other terminal goes to the full line-line voltage). It is noted that the start and finish leads of the OH coil are located on the outer a

inner layers of the four layer coil, respectively, and that this effects the voltage stress of the components which physically interface with the coil.

From these tables it is noted that with Vchi = 1kV, the safety factor on the insulation (hipot level/max operating level) is somewhat compromised (slightly less than the 2x desired) in the various cases, but seriously reduced to 1.5 in the case of the TF. If Vchi = 2kV, then the maximum voltage across the TF inner leg groundwall insulation could go to 3kV, which is the hipot level (i.e. the safety factor is gone).

On the other hand, the dielectric strength of the TF coil inner legs can probably take much higher voltages. The nominal groundwall insulation thickness is 50 mils Scotchply, rated 620 volts/mil. However, the outer Scotchply layer was machined so as to produce a precision cylinder for insertion into the OH tension tube. Therefore the 50 mil value needs to be thought of as an average; certain areas may be thinner.

Based on the aforementioned considerations, it is recommended that:

• *Future CHI operations shall be limited to 1kV;*

• *The now floating group of components(OH tension tube, PF1a and PF1b ground planes and coil holders, TF hub assemblies) shall be tied locally to the center stack casing on top and bottom using 10Ω resistors;*

It is not expected that the 1kV constraint will seriously limit CHI experiments.

*However, if the need to go to 2kV is identified at a later date, then tests should be performed on a sample of 0.050" thick Scotchply and, assuming that sufficient dielectric strength is verified, the TF hipot level should be increased from 3kV to at least 4.5kV (safety factor of 1.5), preferably 6.0 kV (safety factor of 2.0).*

Outer VV – to – TF Coil Inner Legs:

| Electrodes | Vmax | Vmin | Vmaxgf | Vmingf | Between Electrodes | nom \|ΔV\| | max \|ΔV\| | Hipot Level | Hipot/ nom \|ΔV\| | Hipot/ max \|ΔV\| |
|---|---|---|---|---|---|---|---|---|---|---|
| Outer VV | 0 | 0 | 1 | -1 | | | | | | |
| | | | | | Ceramic Insulators | 1 | 1 | 5 | 5.0 | 5.0 |
| CS Casing | 1 | -1 | 1 | -1 | | | | | | |
| | | | | | $\mu$therm | 0 | 0 | 5* | n.a. | n.a. |
| OH Ground Plane | 1 | -1 | 1 | -1 | | | | | | |
| | | | | | OH Ground-wall | 4 | 7 | 13 | 3.3 | 1.9 |
| OH Coil Layer 4 | 3 | -3 | 6 | -6 | | | | | | |
| | | | | | OH Coil | 6 | 6 | n.a. | n.a. | n.a. |
| OH Coil Layer 1 | 3 | -3 | 6 | -6 | | | | | | |
| | | | | | OH Ground-wall | 4 | 7 | 13 | 3.3 | 1.9 |
| Tension Tube | 1 | -1 | 1 | -1 | | | | | | |
| | | | | | TF Ground-wall | 1.5 | 2 | 3 | 2.0 | 1.5 |
| TF Coil Inner Legs | 0.5 | -0.5 | 1 | -1 | | | | | | |

* = never tested

CS Casing – to – PF1a Coil – OH Ground Plane

| Electrodes | Vmax | Vmin | Vmaxgf | Vmingf | Between Electrodes | nom \|ΔV\| | max \|ΔV\| | Hipot Level | Hipot/ nom \|ΔV\| | Hipot/ max \|ΔV\| |
|---|---|---|---|---|---|---|---|---|---|---|
| CS Casing | 1 | -1 | 1 | -1 | | | | | | |
| | | | | | $\mu$therm | 0 | 0 | 5* | n.a. | n.a. |
| PF1A Ground Plane | 1 | -1 | 1 | -1 | | | | | | |
| | | | | | PF1A Ground-wall | 3 | 5 | 9 | 3.0 | 1.8 |
| PF1A Coil | 2 | -2 | 4 | -4 | | | | | | |
| | | | | | PF1A Ground-wall | 3 | 5 | 9 | 3.0 | 1.8 |
| PF1A Ground Plane | 1 | -1 | 1 | -1 | | | | | | |
| | | | | | Gap | 0 | 0 | n.a. | n.a. | n.a. |
| OH Ground Plane | 1 | -1 | 1 | -1 | | | | | | |

PF1b Coil

| Electrodes | Vmax | Vmin | Vmaxgf | Vmingf | Between Electrodes | nom \|ΔV\| | max \|ΔV\| | Hipot Level | Hipot/ nom \|ΔV\| | Hipot/ max \|ΔV\| |
|---|---|---|---|---|---|---|---|---|---|---|
| PF1B Ground Plane | 1 | -1 | 1 | -1 | | | | | | |
| | | | | | PF1B Ground-wall | 2 | 3 | 5 | 2.5 | 1.7 |
| PF1B Coil | 1 | -1 | 2 | -2 | | | | | | |

3) Hipot Requirement for Class 4 Equipment

Class 4 equipment is that which has a physical connection to the outer VV. Such equipment must be electrically isolated, and the isolation is required to pass a 5kV DC hipot based on 2*2+1=5kV.

One could argue that the outer VV will never go to a high voltage, because the grounding scheme fixes it to near ground. However, if a single ground fault occurs on the opposite terminal of the CHI power supply, then the outer terminal

potential to ground will rise up toward the CHI power supply voltage. This could be ameliorated by providing non-linear resistor based surge suppression on the outer VV terminal. The prospective current, power, and energy which would have to be absorbed are large, though do-able. Let us assume a solid ground fault (zero impedance), and that the CHI power supply is limited to Vchi=1kV, and further that we wish to limit the voltage of the outer VV to 100V. Based on the loop resistance and inductance (Figure 2), and the assumption that the power supply can shut off in 1/2 cycle (8mS) providing 1kV at the source during that interval (actually it would shut off in sinusoidal fashion), then the demands on the surge suppressor would be Imax = 40kA, W = 20kJoule. It is to be noted that this situation (the combination of a ground fault and the simultaneous conduction of a surge supressor) is like a double ground fault, and the 40kA fault current would flow the facility ground grid between the surge arrestor and the initiating ground fault.

In considering whether or not to install a surge arrestor, there is a trade-off between 1) limiting the voltage of the outer VV vs. 2) limiting the power dissipated in a single ground fault and limiting the fault current through ground.

As a compromise, a surge suppressor is not recommended at this time, but a reduction in the hipot requirement can be justified based on the earlier dictum that Vchi shall be limited to 1kV.

*Class 4 hipot requirement shall be reduced to 2*1+1=3kV. If the need for Vchi =2kV is identified at a later date, the 3/2=1.5 safety factor can be accepted, since, except under fault conditions, the outer VV will stay near ground potential.*

4) Segregation and Method of Isolation of Class 4 Equipment

The most numerous of the Class 4 equipment are the magnetic sensors. For these, as described earlier, the approach has been to tie the common of the receiving electronics racks to the outer VV, and to provide a single high voltage break in the AC power source. Also, all of the related cabling and tray has been carefully segregated. The idea here is to provide a single, robust high voltage break, rather than a large number of perhaps less robust breaks at various locations. This reduces the likelihood of a fault, and facilitates troubleshooting of unexpected conducting paths from the outer VV to ground, because the number of pathways is limited. The GDC system was treated in the same fashion as the magnetics. One limit switch in the gas injection system is not treated this way; it has a local isolation which passes the 5kV hipot requirement, but its output is received by electronics rack which is at ground (Class 2).

Now that more Class 4 type equipment is being added to the machine, e.g. the TIV and shutter control system, the issue arises as to how to deal with this equipment. Should it be segregated and isolated at a few breaks, or isolated locally as it contacts the outer VV, and then routed as an ordinary Class 2 signal, to a Class 2 rack at ground?

On TFTR, there was no segregation requirement. Many components were physically attached but electrically isolated from the machine, at the machine, such that the wiring running away from the machine did not require segregation. Since there was no CHI consideration, the main concern was toroidal loop voltage from plasma disruption. Another difference relates to the fact that since the TFTR vacuum vessel was not toroidally continuous as is the NSTX vacuum vessel, a measurable voltage could appear on the vessel in case of a disruption event.

TFTR had a "ground fault monitor" which sounded an alarm in the TFTR Test Cell when any spurious grounds were placed accidentally on the vacuum vessel. At the present time NSTX does not have such a feature, although it has been discussed. We have been planning to implement, prior to the next run period, a new feature to the CHI grounding system which will provide 100V or so of voltage between the CSC and outer VV (ref. [4]) but this system will not alert us to spurious leakage paths to ground. Leakage paths to ground are detected via the hipot of the CHI system, which places a common mode voltage on the CSC and outer VV to ground. However, present practice is such that the CHI hipot is only performed in the morning on run days when the CHI power supply system is to be operated.

If we decide to allow that new components can be added to NSTX without following the Class 4 isolation and segregation techniques implemented thus far, then we add the risk that faults to ground through these items become more probable, and the identification and location of such faults becomes more difficult. On the other hand it has been argued that the segregation costs money.

*As a compromise, it is recommended that the special treatment of components connected to the outer VV be dropped, on the condition that the TFTR Ground Fault Monitor, or an equivalent device, be added to NSTX such that a horn is sounded in the NSTX Test Cell if a spurious conducting path is introduced from either the CSC or outer VV to ground.*

By sounding a horn in the test cell, problems can be identified at the moment they are introduced, thereby alleviating the problem of fault identification and location. Such a scheme is not the equivalent of a hipot since it will not have the sensitivity to detect faults with resistance > 10's of ohms. But, for operation days when CHI is not running, this level of sensitivity is probably OK (as it evidently was for TFTR). On CHI days, the morning hipot of the CHI power supply system will identify high resistance problems, which will then need to be chased down amongst the many possible paths.

cc:

| | | | |
|---|---|---|---|
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