Digital Input and Timestamp Module (DITS) User's Guide

Draft 24Aug2006 PS
Rev 0 10Jan2007 PS
Rev 1 23Feb2007 PS

1.0 INTRODUCTION....2

2.0 REFERENCES....2

3.0 MODULE DESCRIPTION....2

4.0 MODULE FEATURES....4

4.1 Mechanical Characteristics....4

4.2 Connectors....4

4.3 FPDP Interface....5

4.4 LEDs....6

4.5 Front-Panel Switches....6

4.6 Front-Panel LEMO Inputs....6

4.7 Opto-22 Style Digital Inputs....7

4.8 'P2' Opto-isolated Digital Inputs....8

4.9 General Purpose Inputs/Outputs....8

4.10 Test Points....8

4.11 Configuration Jumper Summary....9

4.12 Fuses....9

5.0 CPLD DESCRIPTION....9

6.0 FIGURES & TABLES....9

1.0 Introduction

The Digital Input and Timestamp Module (DITS) is a VME-format board that provides timing and synchronization as well as digital input information onto an FPDP bus. In response to an external 'sample' signal the module will drive eight 32-bit words on the FPDP bus. This document will describe the module's characteristics, configuration, operation, performance constraints, and design reference material. A block diagram of the board is shown in fig. 1.

2.0 References

1) FPDP Specification: *title/rev/date/managing-organization*
2) Peer Review for DITS, August 3, 2006, per Work Planning Form #1296.
3) DITS Software Design Document, M. Isaacs, August 2006.
4) DITS Design Notebook, R. Marsala office files.
5) Family Tree Drawing for the DITS, B-AE4001, SH 12.
6) Schematic, FPDP Digital Input & Time Stamp (DITS), C-AE4250.
7) Assembly, FPDP Digital Input & Time Stamp (DITS), B-AE4251.
8) Parts List, FPDP Digital Input & Time Stamp (DITS), A-AE4252.
9) PC Layer Info, FPDP Digital Input & Time Stamp (DITS), C-AE4253.

3.0 Module Description

The module is fabricated as a B-Size VME board with a single width (4HP by 6U) front panel. The module provides Digital Input and Timing and Synchronization information. The front-panel FPDP bus connection is used to transmit eight 32-bit command words. A notch in the front panel allows two ribbon cables to enter the board. Each of the cables is configured so that it can be directly connected to an 'Opto-22' rack panel which holds up to 16 I/O modules. Modules are available with a variety characteristics for common to controls system applications. In addition there are 16 opto-isolated digital inputs connected to the 'P2' VMEbus connector.

There are two counters on the DITS module, the Timestamp Counter and the Block Counter.

Timestamp

The 48-bit 'Timestamp' will essentially provide the time (on FPDP words 1 and 2) at which the *sample clock* was received. The time

is in microseconds and is relative to the *reset pulse*. Reset may occur at the start of the NSTX clock cycle (e.g. T[-140] seconds.)

- 48 bits (~9 years)
- Counter incremented from a 1 MHz *Timestamp Clock*.
- Counter halts when full. Value = 0xFFFF_FFFFFFFF.
- The *sample clock* and the *timestamp reset pulse* can be accepted from front-panel LEMO connectors or from the FPDP bus PIO1/PIO2 lines. The source is selectable with a jumper. The selected signal is routed to a Test Point (ref. table 1)
- The module status (word 3) contains the *overflow* status of the *Timestamp Counter.*

Sample/Block Counter

The 32-bit block counter is simply a counter of *sample clock*s. The Block Counter is presented on FPDP word 5.

- At NSTX, the sample clocks presently run at 1 Hz between NSTX shots and at 5 KHz during the NSTX shot. The module's software and hardware design will accommodate much higher (500 KHz) sample clock rates.
- When the counter becomes full (> 1 year) it will rollover and continue counting.
- The Block Counter is reset in one of two ways, depending upon a jumper (see Table 2). In one mode the counter is reset from the LEMO/PIO2 *timestamp reset pulse* (same as the Timestamp counter). In the other mode the Block Counter is rest only via the front-panel *module reset* pushbutton
- The *Block Counter timestamp reset pulse* can be accepted from front-panel LEMO connectors or from the FPDP bus PIO1/PIO2 lines.

Timestamp Clock (1 MHz)

- External LEMO connector: Nominally accepts a 1 MHz clock that is externally sourced, e.g., from the Facility Clock using CAMAC 313 module or Universal Networked Timer (UNT) device.
- An internal 1 MHz clock takes over if external clock doesn't toggle within ~800 nanosecs. The internal 1 MHz is based on a 32 MHz CPLD System Clock.
- Once switched to the internal/back-up clock source, the internal clock is used until the next *Reset pulse*, which switches back to try the external clock.
- The module status (word 3) contain the status of the external *Timestamp Clock* signal and also the internal/external clock-source.

An 8-LED array provides diagnostic and operating information. Two pushbuttons are on the front panel to RESET the module and CLEAR latched LEDs. A few general purpose I/O points are available at the rear VMEbus 'P2' connector.

The DITS contains a CPLD (Complex Programmable Logic Device) which provides a high degree of flexibility in the module's operating characteristics and on-board diagnostic capability. The module is configurable using on-board jumpers.

4.0 Module Features

4.1 Mechanical Characteristics

The module is fabricated as a B-Size VME board. The front-panel (fig. 2) is single-width (4HP, 0.8"). The board requires only +5V power from the VME bus. It will pass the VMEbus control lines as necessary such that the board will not prevent 'downstream' VME modules from operating correctly. The outer rows (A, C) of the P2 connector are available for board-specific I/O.

4.2 Connectors

Front Panel Connectors

- FPDP (80-pin)

Board Mounted Connectors Accessible Via Front Panel Notch

- Digital Input (Two, 50-pin headers to interface with an Opto-22 relay panels)

Rear VMEbus Connectors

- P1 and the center row (B) of P2 are reserved for the normal VMEbus connections. (P2 row B will have +5 V and Ground levels on the power pins sourced from the module, see fig.7.)
- The outer rows (A, C) of the P2 connector can optionally be used for board-specific I/O. The board-specific P2 pin assignments are shown on fig. 7.

On-Board Connectors

- JTAG: A 7-pin JTAG connection is available to program the CPLD. Fig. 11 provides information about the JTAG connections and programs.

4.3 FPDP Interface

The DITS module drives/provides a nominal 16 MHz pECL clock (aka PSTROBE/PSTROBE*); timing for this bus is shown in figs. 8 and 10. The FPDP can send a word every ~63 nanoseconds. So, the 8-word block takes about 512 nanoseconds, thus limiting the external Sample Clock rate to about 1.5 MHz. The 8-word block is described on fig. 9.

The DITS will assert the FPDP lines 'NRDY*' (not ready for data) and 'Suspend*' and DVALID* (Data Valid). The DIR* (FPDP data direction) is pulled low to continuously assert the 'data source/output) mode. The CPLD device on the DITS is capable of responding to or asserting the PIO1 and PIO2 lines. On-board jumpers are used to configure the input or output mode for these lines. There are presently no plans to use the PIO signals. The FPDP SYNC* signal is optionally (via jumper) asserted with the final word.

FPDP Word/Block Format

The FPDP Word Format (8-word block) for the DITS is shown in fig. 9. This block is output on to the FPDP bus in response to a Sample Clock input's rising/leading edge.

- Word 0: Fixed-format 'header' word.
  - If jumper installed, value = 0x87654321
    - For the NSTX PCS, this value indicates the first word of an NSTX data block.
    - Only one module in an FPDP data stream should have the jumper in this position.
  - If jumper removed, value = 0x12345678.
- Word 1: Most significant 16 bits of 48-bit Timestamp.
- Word 2: Least significant 32 bits of 48-bit Timestamp.
- Word 3:
  - 16 bits of 'P2' Opto-isolated Digital Inputs.
  - (8) General Purpose Inputs
  - 8 bits of Module Status
    - bit 0 (lsb): Power status (+5, 3.3, Opto-22) (1=OK)
    - bit 1: Timestamp counter full (1=Not Full)
    - bit 2: Timestamp Clock source (1=External{normal}, 1=Internal)
    - bit 3: Timestamp Clock active (1=TS Clock input active)
    - bits 4-7(msb): spare (set to 0).
- Word 4: Opto-22 Style Inputs (2 banks of 16 bits)
- Word 5: 32-bit Block/Sample Counter

- Word 6: Fixed-format word. This word is 'spare' and may be replaced if an application arises.
- Word 7: Fixed-format word. This word is 'spare' and may be replaced if an application arises.

4.4 LEDs

Module Status

A front-panel array of 8 LED's is used to indicate module activity and status. Fig. 2 provides details about the LEDs.

- Module +5 V power
- FPDP Bus Active
- Timestamp Reset pulse
- spare
- Timestamp Clock Fault
- Timestamp counter full
- Voltage Fault
- Opto-22 Logic Voltage Fault

LED's for 'P2' Opto-isolated Digital Inputs

An array of 16 LED's show the on/off status of each of the 16 opto-isolated digital inputs received at the VMEbus 'P2' connector.

4.5 Front-Panel Switches

There are two momentary front-panel momentary buttons:

- MODULE RESET: turns off latched LEDs, resets all CPLD state machines to Idle state, resets all counters.
- CLEAR LEDs: turns off latched LEDs.

4.6 Front-Panel LEMO Inputs

Consult the data sheets and schematic diagrams, C-AE4250, for details. Portions of the schematic and electrical parameters are shown on fig. 3. All three inputs use a 3-pin LEMO connector. All LEMO pins/signals are isolated from the board's ground (to several hundred volts).

Sample Clock: This input uses an opto-isolator and expects to receive a 5 volt signal. The positive-going or rising edge is the

active edge. This transition will increment the 32-bit Block Counter and then cause the module to generate its 8-word FPDP block. By using configuration jumpers (see table 2) the module can also accept the sample clock from the PIO1 line. The positive-going or rising edge of the PI01 line is the active edge.

Timestamp Reset: This input is transformer-coupled and expects to receive a 5 volt, 1 microsecond pulse. The positive-going or rising edge is the active edge. This transition will RESET the 48-bit Timestamp and the 32-bit Sample/Block Counter. By using configuration jumpers (see table 2) the module can also accept the *reset pulse* from the PIO2 line. The positive-going or rising edge of the PI02 line is the active edge.

Timestamp Clock/Increment Input: This input is transformer-coupled and expects to receive a 5 volt, 1 MHz clock. The positive-going or rising edge is the active edge. This transition will increment the 48-bit Timestamp value.

4.7 Opto-22 Style Digital Inputs

The DITS provides two banks of 16 digital inputs via two 50-pin headers. The headers are located near the front panel and are configured to ribbon-cable directly to an Opto-22 Rack Panel, supporting the G1 and G4 I/O module families. The 'field' side of the Opto-22 modules is compatible with a variety of AC and DC control voltages. The Opto-22 modules provide electrical isolation between the DITS and the 'field' wiring.

- Figure 4 is a portion of the schematic diagram that shows some characteristics of the electrical interface and Opto-22 part references.
- An 'energized' Opto-22 input module will present a logic '1' in the FPDP word.
- In response to the Sample Clock the two banks will be read and the data presented to the FPDP bus on word 4 (see fig. 9).

Opto-22 Logic Power

- The I/O modules on the Opto-22 rack panel require a source of 5 Vdc power to operate their 'logic' side. The logic power can be supplied by either the DITS or from an external power supply. The modules' 'field' power is electrically isolated from the logic power and is separately supplied by the 'field' electrical system.
- A DITS front-panel LED will illuminate if the +5V Logic power is not present (from either external supply or

DITS-sourced via the fuse). This will also be annunciated on the FPDP bus via the module status bits in word 3.

- If the DITS is used to supply the logic power:
  - The DITS 5V VMEbus power is used via a 1A fuse, for each 50-pin header/rack panel.
  - The fuse on the Opto-22 rack panel has no affect.
- If an external 5V power supply is used to supply the logic power:
  - The DITS 5V 1A fuse, for each 50-pin header/rack panel, must be removed.
  - The fuse on the Opto-22 rack panel must be installed.

Digital Input Bank Reference

Bank ID	50-pin Connector ID	Fuse ID
Input Bank (0)	J3	F2
Input Bank (1)	J6	F3

4.8 'P2' Opto-isolated Digital Inputs

The DITS module has 16 opto-isolators that provide electrical isolation and level translation for 16 bits of digital input that enter the module via the VMEbus 'P2' connector. There are jumpers to configure each input bit for either contact, 5V, or 7-45 v inputs. Fig. 5 shows the electrical characteristics, fig. 7 lists the P2 connector pin assignments, and Table 2 lists the jumper settings.

4.9 General Purpose Inputs/Outputs

Eight General Purpose Outputs and eight General Purpose Inputs are available at the VMEbus P2 connector. These inputs/outputs are connected, via a level shifting buffer, to the CPLD. The inputs can be used to alter the operation of the CPLD while the outputs can be used for monitoring and status. External circuitry must be designed to be electrically compatible with the GP input circuit. Fig. 6 shows the electrical characteristics and fig. 7 lists the P2 pin assignments.

4.10 Test Points

To aid in troubleshooting and design verification there are 26 test points (including 4 ground test points) on the printed circuit board. The test points are described in Table 1.

4.11 Configuration Jumper Summary

Table 2 provides details about the DITS' jumper settings. In summary:

- PIO1 & PIO2 usage.
- Sample clock and Reset source.
- 'P2' Opto-isolated Digital Inputs *input type* (16).
- Spare Jumpers.

4.12 Fuses

The table below shows the on-board fuses.

Fuse ID	Description	Rating	Mfgr/Part#
F1	3.3 V reg.	1A	Wickmann 396 1100 044
F2	Opto-22 Input Bank 0 Logic pwr	1A	Wickmann 396 1100 044
F3	Opto-22 Input Bank 1 Logic pwr	1A	Wickmann 396 1100 044

Notes: All fuses are type 'time lag'.

5.0 CPLD Description

The CPLD is a XiLinx product (XC9500XL). The software was developed using XiLinx's ISE WebPACK development tool. The CPLD's functions and timing diagrams are described in reference 3, the DITS CPLD Design Notebook. The module's block diagram (fig. 1) indicates some of the CPLD's functions.

6.0 Figures & Tables

Figure 1: Block Diagram
Figure 2: Front Panel Layout & LED's
Figure 3: Front Panel Timing/Counter Control Signals (LEMO)
Figure 4: Opto-22 Style Digital Inputs (via Front Panel notch)
Figure 5: 'P2' Opto-Isolated Digital Inputs
Figure 6: General Purpose I/O Information
Figure 7: VMEbus P2 Connector Pin Assignments
Figure 8: FPDP Timing Diagram
Figure 9: FPDP Word Format for the DITS
Figure 10: Module Throughput Timing Diagram
Figure 11: JTAG Connector and Reference

Table 1: Test Points
Table 2: Configuration Jumper Plugs
Table 3: General Timing Parameters

Figure 1: Block Diagram

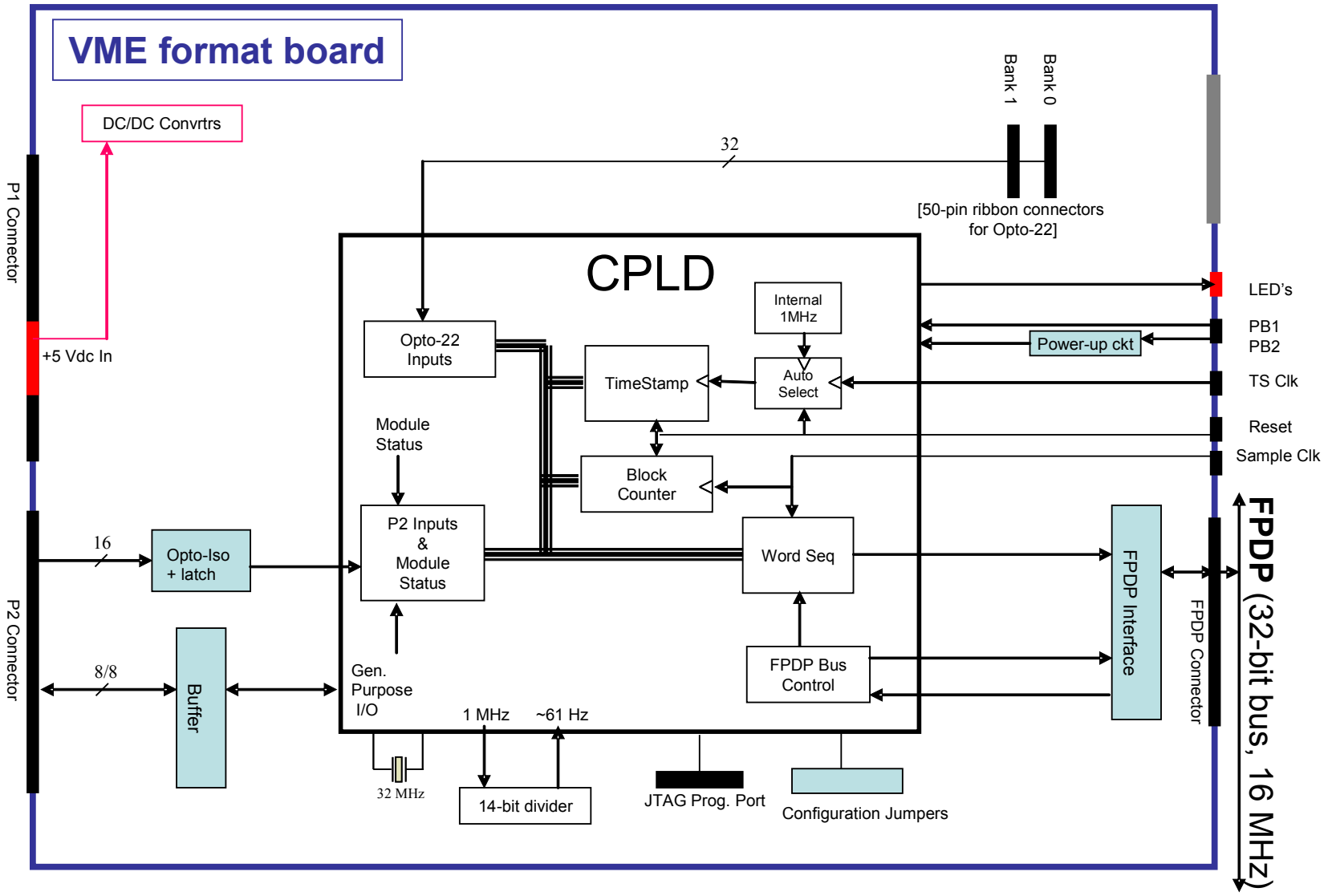
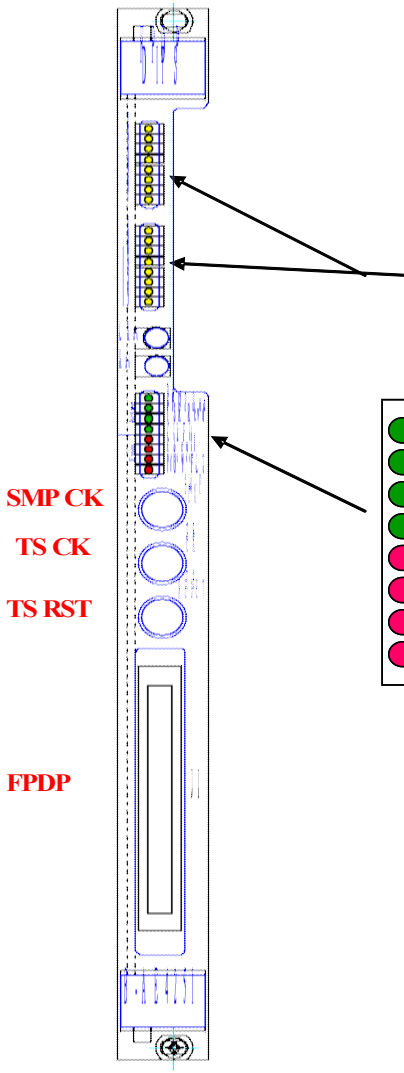


Figure 2: Front Panel Layout & LEDs

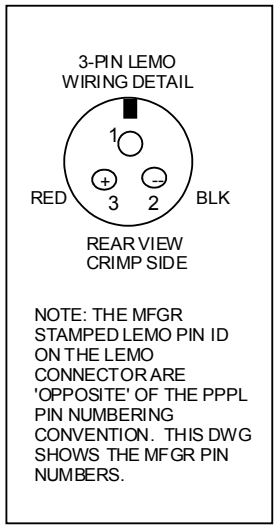


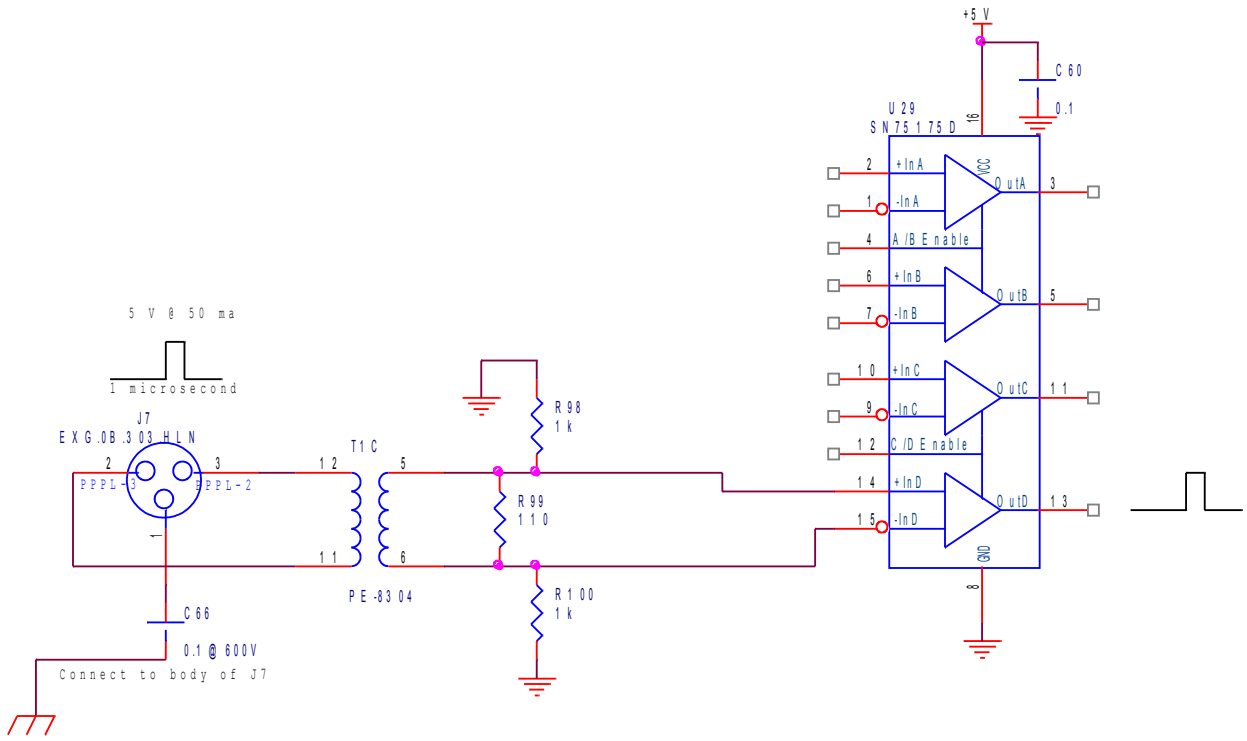
LEDs show 'P2' Opto -Isolated Inputs (16)

Description

Pwr	Lit when +5 Vdc VMEbus Power is OK
FPDP Bus	Flash when FPDP output occurs (also Sample Clock)
TSR Rcvd	Flash when TimeStamp Reset pulse is received
.	spare
Clk Flt	External TS Clk Dropout/Fault
TS Full	Lights (latched) when TimeStamp counter is full.
Vlt Flt	Lights (latched) upon any out -of-tolerance supply voltage (+5, +3.3)
I/O V FLT	Lights (latched) when the Opto -22 voltage is not present.

Figure 3: Front Panel Timing/Counter Control Signals (LEMO) part 1 of 2



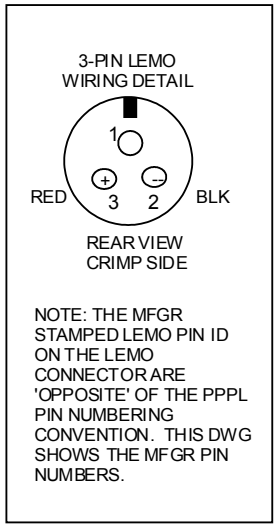


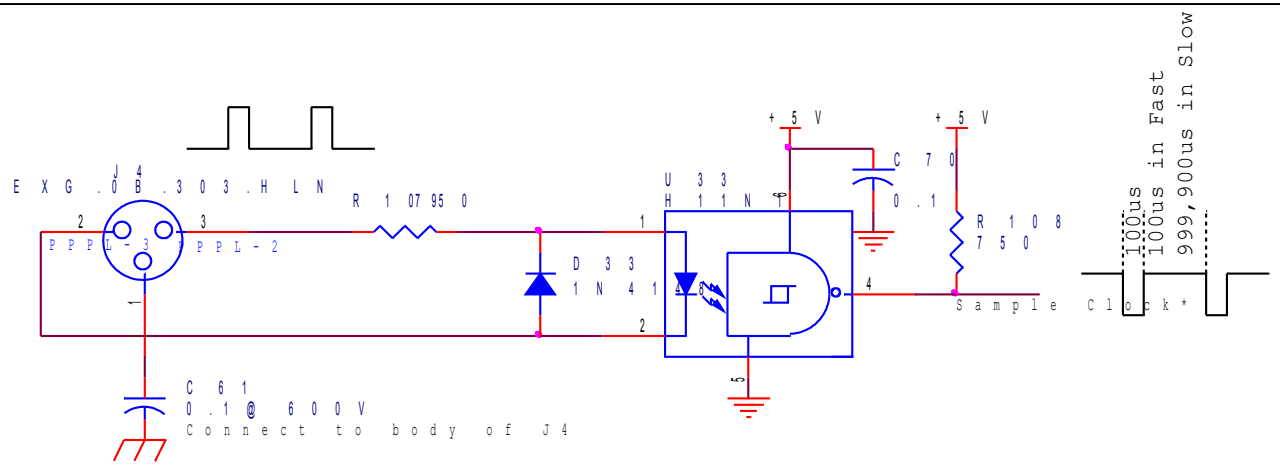
Pin arrangement for mating LEMO connector (attached to field cable).	1) Input circuit for **Time Stamp Clock** and the **Time Stamp Reset** input. 2) Inputs are 5 volts, one microsecond (transformer-coupled signal). 2) The active edge is the leading/rising edge. 3) Vmax = 12.0 V, Vmin = 3.0 V.

Notes:
1) The pin orientation for the female on-board 3-pin LEMO receptacle when viewed from the front of the module is the same as in the diagram above.
2) LEMO part number for female on-board 3-pin LEMO: EXG.0B.303.HLN

3) Typical LEMO Part Number for mating cable-plug, male 3-pin LEMO: FGG.0B.303.CYC

Figure 3: Front Panel Timing/Counter Control Signals (LEMO) part 2 of 2

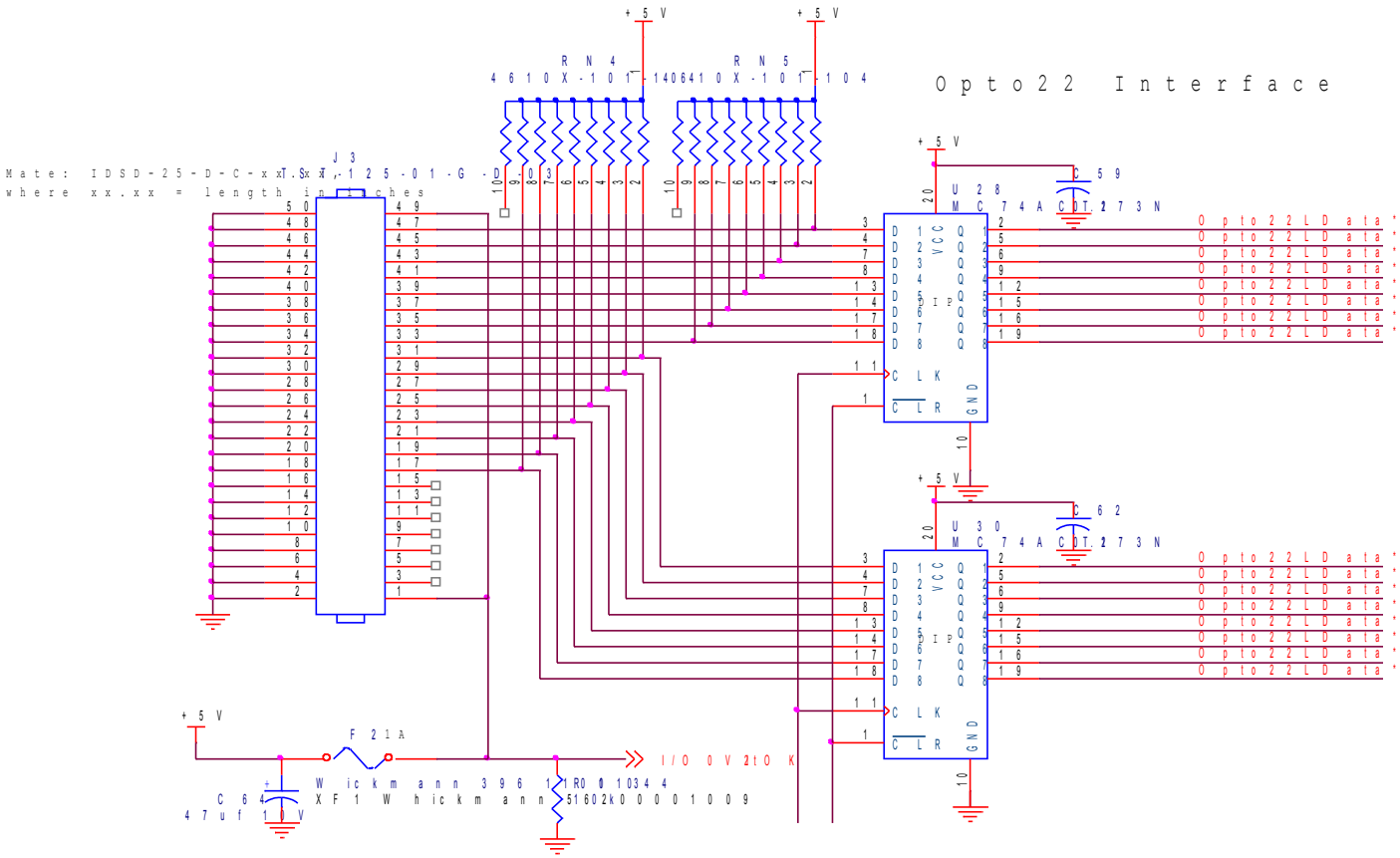




Pin arrangement for mating LEMO connector (attached to field cable).	1) Input circuit for (Data) **Sample Clock** input. 2) The active edge is the leading/rising edge. 3) Pulse Vmax = 9.5 V, Pulse Vmin = 4.4 V. Base Vmax = 0.8 V 4) Fmax for Sample Clock is About 500 KHz.

Notes:
1) The pin orientation for the female on-board 3-pin LEMO receptacle when viewed from the front of the module is the same as in the diagram above.
2) LEMO part number for female on-board 3-pin LEMO: EXG.0B.303.HLN
3) Typical LEMO Part Number for mating cable-plug, male 3-pin LEMO: FGG.0B.303.CYC

Figure 4: Opto-22 Style Digital Input Signals (front panel notch)



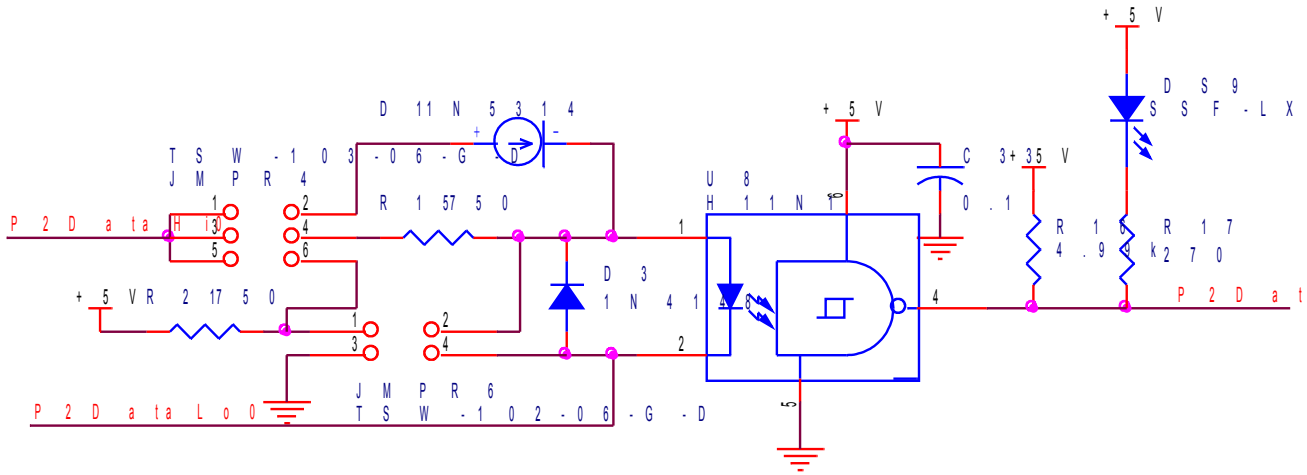
Notes:

1) Single-ended inputs. Vmax = 5.5 V Vmin (for a logic '1') = 2.0 V. Vmax (for logic "0").= 0.8 V

2) An Opto-22 rack panel which mates with the DITS 50-pin connector via a ribbon cable is part# PB16H for the G1 I/O module family, or G4PB16H for the G4 I/O module family.

3) If the 'Logic Side' +5V power on the Opto 22 rack panel is **externally supplied** (i.e., external supply is wired to PB16H terminals [+5 & GND]) then **remove the 1A fuse on the DITS board**. See section 4.12 for a listing of the fuses.

Figure 5: 'P2' Opto-isolated Digital Input Signals



Input Signal	Jmpr4	Jmpr6	Logic	Signal Parameters
Contact	5-6	1-2 3-4	Closed Contact = logic '1'	Current sink ~5 ma
5 V	3-4	open	5 V = logic '1' <0.8 V = logic '0'	Vmin = 4.4 V Vmax = 9.5 V Inom = 4 ma @ 5 V
7-45 V	1-2	open	Vin > 7 V = logic '1' < 1.5 V = logic '0'	Vmin = 7 V Vmax = 45 V Inom = 4.7 ma for all voltage above 7 V

Figure 6: General Purpose I/O Information

VMEbus Connector 'P2' Auxiliary Input/Outputs

P2 Pin #	Outputs	P2 Pin #	Inputs
C1	GP Out 0	C9	GP In 0
C2	GP Out 1	C10	GP In 1
C3	GP Out 2	C11	GP In 2
C4	GP Out 3	C12	GP In 3
C5	GP Out 4	C13	GP In 4
C6	GP Out 5	C14	GP In 5
C7	GP Out 6	C15	GP In 6
C8	GP Out 7	C16	GP In 7

- P2-A1 thru P2-A16 are Ground

Table showing basic GP I/O Electrical Characteristics

Description	Value	Unit	Comment
Vin High	2.0	V	Min. (note 2)
Vin Low	0.8	V	Max.
Vout High	4.7	V	Min (@ 24 mA source)
Vout Low	0.55	V	Max (@ 24 mA sink)

1) **Inputs** tied to DITS internal +5 V supply via 10K resistor. See fig 4.
2) **Max voltage** on any pin w/o damage = 5.5 V.
3) Reference Schematic diagram, C-AE4250 for electrical interface details. Interface device is SN74ACT541E.

Figure 7: VMEbus Connector P2 Input/Output

Row A Pin #	Description	Row B Pin #	Description	Row C Pin #	Description
A1	ground	B1	Ground	C1	GP Out bit 0
A2	ground	B2	+5 Vdc	C2	GP Out bit 1
A3	ground	B3	Reserved for VME use	C3	GP Out bit 2
A4	ground	B4	See B3	C4	GP Out bit 3
A5	ground	B5	See B3	C5	GP Out bit 4
A6	ground	B6	See B3	C6	GP Out bit 5
A7	ground	B7	See B3	C7	GP Out bit 6
A8	ground	B8	See B3	C8	GP Out bit 7
A9	ground	B9	See B3	C9	GP In bit 0
A10	ground	B10	See B3	C10	GP In bit 1
A11	ground	B11	See B3	C11	GP In bit 2
A12	ground	B12	Ground	C12	GP In bit 3
A13	ground	B13	+5 Vdc	C13	GP In bit 4
A14	ground	B14	See B3	C14	GP In bit 5
A15	ground	B15	See B3	C15	GP In bit 6
A16	ground	B16	See B3	C16	GP In bit 7
A17	Digital Input bit 15 (-)	B17	See B3	C17	Digital Input bit 15 (+)
A18	Digital Input bit 14 (-)	B18	See B3	C18	Digital Input bit 14 (+)
A19	Digital Input bit 13 (-)	B19	See B3	C19	Digital Input bit 13 (+)
A20	Digital Input bit 12 (-)	B20	See B3	C20	Digital Input bit 12 (+)
A21	Digital Input bit 11 (-)	B21	See B3	C21	Digital Input bit 11 (+)
A22	Digital Input bit 10 (-)	B22	Ground	C22	Digital Input bit 10 (+)
A23	Digital Input bit 9 (-)	B23	See B3	C23	Digital Input bit 9 (+)
A24	Digital Input bit 8 (-)	B24	See B3	C24	Digital Input bit 8 (+)
A25	Digital Input bit 7 (-)	B25	See B3	C25	Digital Input bit 7 (+)
A26	Digital Input bit 6 (-)	B26	See B3	C26	Digital Input bit 6 (+)
A27	Digital Input bit 5 (-)	B27	See B3	C27	Digital Input bit 5 (+)
A28	Digital Input bit 4 (-)	B28	See B3	C28	Digital Input bit 4 (+)
A29	Digital Input bit 3 (-)	B29	See B3	C29	Digital Input bit 3 (+)
A30	Digital Input bit 2 (-)	B30	See B3	C30	Digital Input bit 2 (+)
A31	Digital Input bit 1 (-)	B31	Ground	C31	Digital Input bit 1 (+)
A32	Digital Input bit 0 (-)	B32	+5 Vdc	C32	Digital Input bit 0 (+)

- See figure 6 for additional details on Spare/General Purpose inputs and outputs.

Figure 8: FPDP Timing Diagram
(Part 1 of 2)

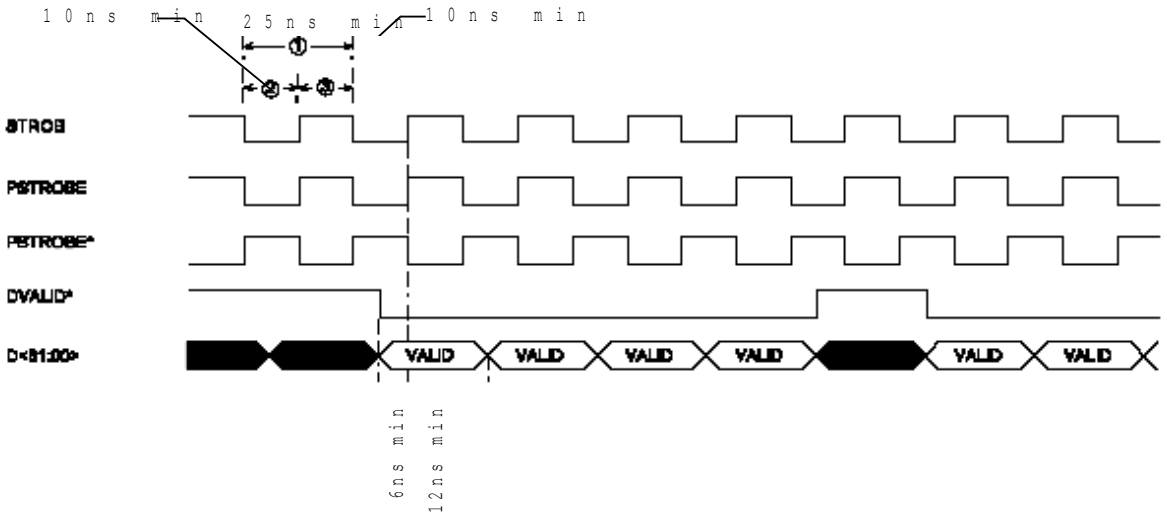


Figure 8: FPDP Timing Diagram
(part 2 of 2)

	PARAMETER	At Transmitter End of Cable	At Receiver End of Cable
1	STROB period	25 ns min.	25 ns min.
2	STROB low	10 ns min.	10 ns min.
3	STROB high	10 ns min.	10 ns min.
4	DATA, DVALID* & SYNC* Setup to STROB	5.5 ns min.	4.5 ns min.
5	DATA, DVALID* & SYNC* Hold from STROB	12.0 ns min.	11.0 ns min.
6	SUSPEND* to DVALID* negated	16 STROB max.	16 STROB max.
7	SUSPEND* negated to DVALID* re-asserted	1 STROB min.	1 STROB min.

Note: Parameters 4 and 5 refer to both rising and falling edge transitions of DATA, DVALID* AND SYNC*.

Figure 9: (FPDP) DITS Command Word Format

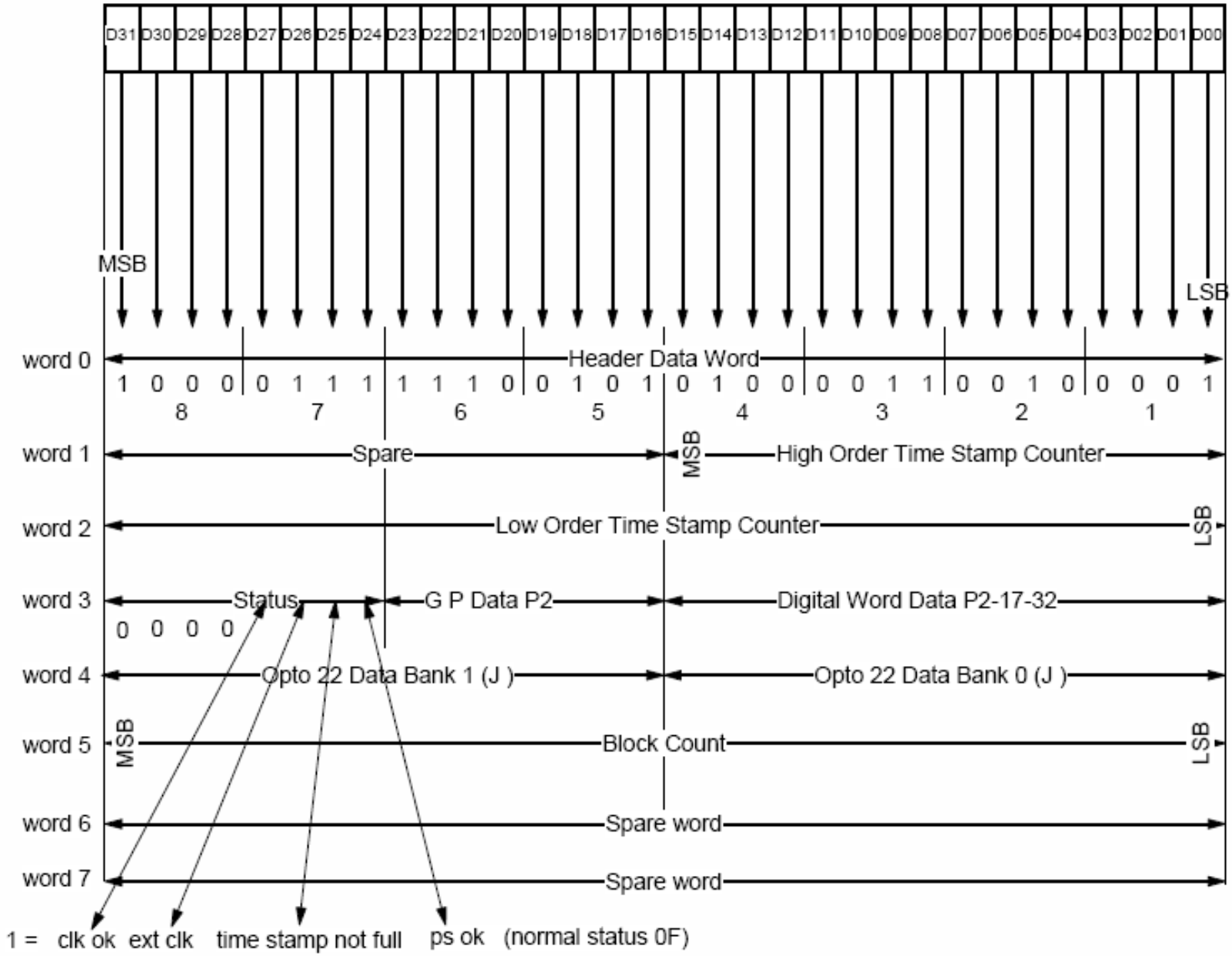
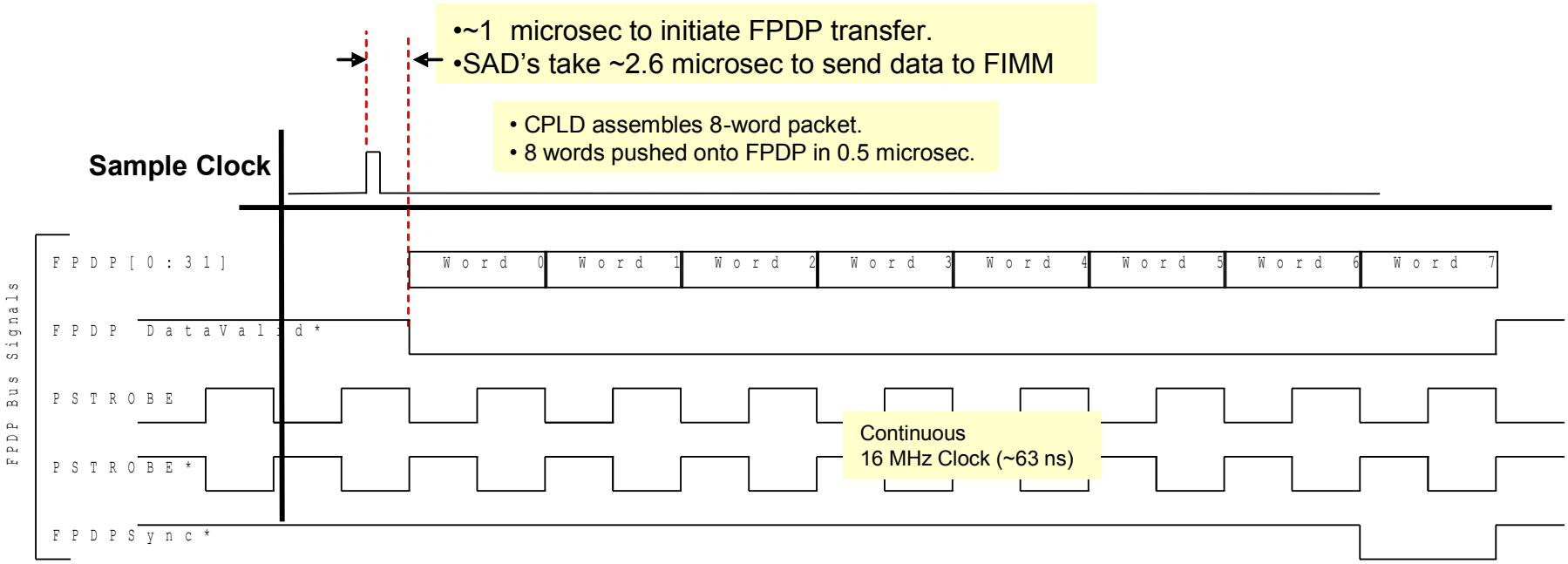

D31 D30 D29 D28 D27 D26 D25 D24 D23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00
MSB
LSB
word 0
Header Data Word
1 0 0 0 0 1 1 1 1 1 1 0 0 1 0 1 0 1 0 0 0 0 1 1 0 0 1 0 0 0 0 1
8 7 6 5 4 3 2 1
word 1
Spare
MSB
High Order Time Stamp Counter
word 2
Low Order Time Stamp Counter
LSB
word 3
Status
G P Data P2
Digital Word Data P2-17-32
0 0 0 0
word 4
Opto 22 Data Bank 1 (J)
Opto 22 Data Bank 0 (J)
word 5
MSB
Block Count
LSB
word 6
Spare word
word 7
Spare word
1 = clk ok ext clk time stamp not full ps ok (normal status 0F)

Figure 10: Module Throughput Timing Diagram



Notes: FPDPSync* line can be suppressed with a Jumper. See Table 2.

Figure 11: JTAG Connector and Reference

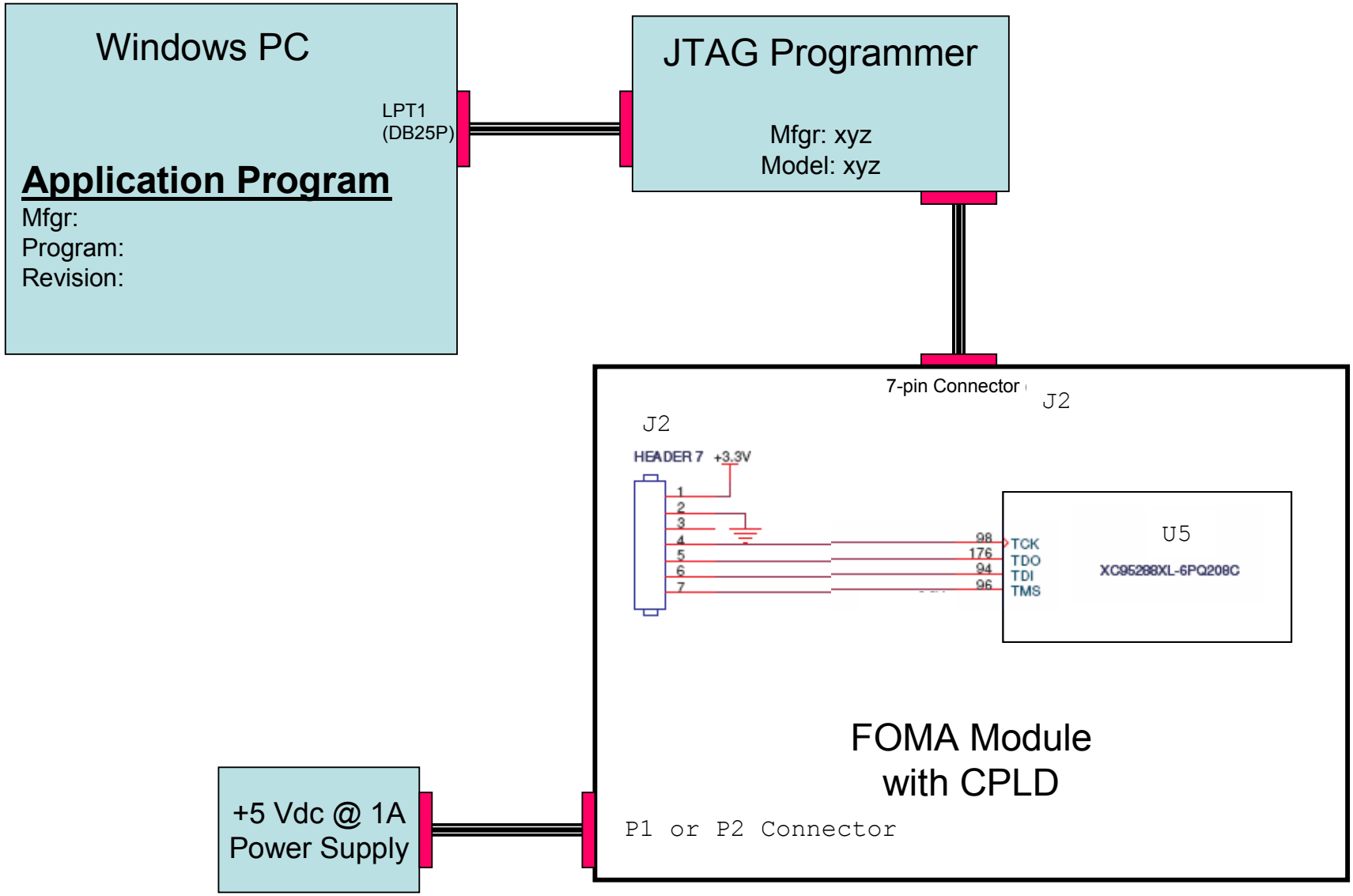


Table 1: Test Points

Reference schematic diagram for details.

TP	Description
1	FPDP_VALID* (direct on bus) (low level indicates data on the bus is valid)
2	FPDP_SYNC* (direct on bus)
3	PSTROBE (direct on bus) , PECL Levels
4	FPDP Clk (sourced by CPLD)
5	Not used
6	Sync* (sourced by CPLD)
7	Selected Sample Clock (CPLD pin 67 output)
8	Selected Reset Pulse (CPLD pin 173 output)
9	Spare 171 (CPLD pin 171 output)
10	Spare 70 (CPLD pin 70 output)
11	Spare 169 (CPLD pin 169 output)
12	Spare 168 (CPLD pin 168 output)
13	32 MHz clock
14-17	Ground
18	+3.3v
19	80 MHz clock
20	LEMO Sample Clock* (buffered and inverted version of the LEMO input)
21	Time Stamp Clock (buffered from LEMO)
22	Time Stamp Reset (buffered from LEMO)
23	20 Hz clock
24	All Power OK
25	PSTROBE* (direct on bus), PECL Levels
26	Reset (active high. TP activates at power-up [20 ms] or front-panel RESET switch).
27	Data_Valid* (sourced by CPLD)

Notes:

1) An asterisk '*' at the end of a signal name indicates an ACTIVE LOW signal.

Table 2: Configuration Jumper Plugs

(part 1 of 4)

Jumper ID	Description	Position	Operation
Jmpr1	PIO1: Sample Clock	b-c b-a off	Only ONE module on the FPDP bus should drive PIO1! • **Async** PIO1 Output (buffered CPLD output). Jmpr3-3/4 must also be ON. • **Sync** PIO1 Output (CPLD output sync'd with FPDP Clock). Jmpr3-1/2 must also be ON. • PIO1 is an **Input** to CPLD (no output/drive). Jmpr3- 3/4 must also be OFF.
Jmpr2	PIO2: Reset Pulse	b-c b-a off	Only ONE module on the FPDP bus should drive PIO2! • **Async** PIO2 Output (buffered CPLD output). Jmpr3-3/4 must also be ON. • **Sync** PIO2 Output (CPLD output sync'd with FPDP Clock). Jmpr3-1/2 must also be ON. • PIO2 is an **Input** to CPLD (no output/drive). Jmpr3-3/4 must also be OFF.
Jmpr3-1/2	Block Counter Reset mode	Off On	• BC reset by front-panel MODULE RESET button (only). • Block Counter reset by front-panel MODULE RESET button OR by TIMESTAMP RESET pulse.
Jmpr3-3/4	Sample Clock and Reset Pulse source	Off on	• Signals sourced from PIO1 (Sample Clock) and PIO2 (Reset). Jmpr1 and Jmpr2 must also be OFF. • Signals sourced from the front panel LEMO connectors.
Jmpr3-5/6	FPDP Sync control	off on	• (logic 1) Suppress Sync line • (logic 0) Generate Sync FPDP line on last (8^{th}) word.
Jmpr3-7/8	Header Word Selection	off on	• 0x12345678 • 0x87654321
Jmpr3-9/10	SPARE Jumper CPLD pin 202	Ref Jmpr3 -15/16	Ref Jmpr3 -15/16
Jmpr3-11/12	SPARE Jumper CPLD pin 203	Ref Jmpr3 -15/16	Ref Jmpr3 -15/16
Jmpr3-13/14	SPARE Jumper CPLD pin 205	Ref Jmpr3 -15/16	Ref Jmpr3 -15/16
Jmpr3-15/16	SPARE Jumper CPLD pin 208	off on	• Binary '1' (note 1) • Binary '0'
Jmpr4-1/2	'P2' Opto-Isolated Digital Input – bit 0	See Fig. 5	Configure with Jmpr6 for input type (5 V, 7-45V, contact)

Jmpr4-3/4	See Jmpr4-1/2	See Jmpr4-1/2	See Jmpr4-1/2
Jmpr4-5/6	See Jmpr4-1/2	See Jmpr4-1/2	See Jmpr4-1/2
Jmpr6-1/2	See Jmpr4-1/2	See Jmpr4-1/2	Configure with Jmpr4 for input type (5 V, 7-45V, contact)
Jmpr6-3/4	See Jmpr4-1/2	See Jmpr4-1/2	See Jmpr6-1/2

Notes: 1) Pin is pulled high (3.3V) with 10k resistor

Table 2: Configuration Jumper Plugs

(part 2 of 4)

Jumper ID	Description	Position	Operation
Jmpr5-1/2	'P2' Opto-Isolated Digital Input – bit 1	See Fig. 5	Configure with Jmpr7 for input type (5 V, 7-45V, contact)
Jmpr5-3/4	See Jmpr5-1/2	See Jmpr5-1/2	See Jmpr5-1/2
Jmpr5-5/6	See Jmpr5-1/2	See Jmpr5-1/2	See Jmpr5-1/2
Jmpr7-1/2	See Jmpr5-1/2	See Jmpr5-1/2	Configure with Jmpr5 for input type (5 V, 7-45V, contact)
Jmpr7-3/4	See Jmpr5-1/2	See Jmpr5-1/2	See Jmpr7-1/2
Jmpr8-1/2	'P2' Opto-Isolated Digital Input – bit 2	See Fig. 5	Configure with Jmpr10 for input type (5 V, 7-45V, contact)
Jmpr8-3/4	See Jmpr8-1/2	See Jmpr8-1/2	See Jmpr8-1/2
Jmpr8-5/6	See Jmpr8-1/2	See Jmpr8-1/2	See Jmpr8-1/2
Jmpr10-1/2	See Jmpr8-1/2	See Jmpr8-1/2	Configure with Jmpr8 for input type (5 V, 7-45V, contact)
Jmpr10-3/4	See Jmpr8-1/2	See Jmpr8-1/2	See Jmpr10-1/2
Jmpr9-1/2	'P2' Opto-Isolated Digital Input – bit 3	See Fig. 5	Configure with Jmpr11 for input type (5 V, 7-45V, contact)
Jmpr9-3/4	See Jmpr9-1/2	See Jmpr9-1/2	See Jmpr9-1/2
Jmpr9-5/6	See Jmpr9-1/2	See Jmpr9-1/2	See Jmpr9-1/2
Jmpr11-1/2	See Jmpr9-1/2	See Jmpr9-1/2	Configure with Jmpr9 for input type (5 V, 7-45V, contact)
Jmpr11-3/4	See Jmpr9-1/2	See Jmpr9-1/2	See Jmpr11-1/2
Jmpr12-1/2	'P2' Opto-Isolated Digital Input – bit 4	See Fig. 5	Configure with Jmpr14 for input type (5 V, 7-45V, contact)
Jmpr12-3/4	See Jmpr12-1/2	See Jmpr12-1/2	See Jmpr12-1/2
Jmpr12-5/6	See Jmpr12-1/2	See Jmpr12-1/2	See Jmpr12-1/2
Jmpr14-1/2	See Jmpr12-1/2	See Jmpr12-1/2	Configure with Jmpr12 for input type (5 V, 7-45V, contact)
Jmpr14-3/4	See Jmpr12-1/2	See Jmpr12-1/2	See Jmpr14-1/2
Jmpr13-1/2	'P2' Opto-Isolated Digital Input – bit 5	See Fig. 5	Configure with Jmpr15 for input type (5 V, 7-45V, contact)
Jmpr13-3/4	See Jmpr13-1/2	See Jmpr13-1/2	See Jmpr13-1/2
Jmpr13-5/6	See Jmpr13-1/2	See Jmpr13-1/2	See Jmpr13-1/2
Jmpr15-1/2	See Jmpr13-1/2	See Jmpr13-1/2	Configure with Jmpr13 for input type (5 V, 7-45V, contact)
Jmpr15-3/4	See Jmpr13-1/2	See Jmpr13-1/2	See Jmpr15-1/2
Jmpr16-1/2	'P2' Opto-Isolated Digital Input – bit 6	See Fig. 5	Configure with Jmpr18 for input type (5 V, 7-45V, contact)
Jmpr16-3/4	See Jmpr16-1/2	See Jmpr16-1/2	See Jmpr16-1/2
Jmpr16-5/6	See Jmpr16-1/2	See Jmpr16-1/2	See Jmpr16-1/2
Jmpr18-1/2	See Jmpr16-1/2	See Jmpr16-1/2	Configure with Jmpr16 for input type (5 V, 7-45V, contact)
Jmpr18-3/4	See Jmpr16-1/2	See Jmpr16-1/2	See Jmpr18-1/2

Table 2: Configuration Jumper Plugs

(part 3 of 4)

Jumper ID	Description	Position	Operation
Jmpr17-1/2	'P2' Opto-Isolated Digital Input – bit 7	See Fig. 5	Configure with Jmpr19 for input type (5 V, 7-45V, contact)
Jmpr17-3/4	See Jmpr17-1/2	See Jmpr17-1/2	See Jmpr17-1/2
Jmpr17-5/6	See Jmpr17-1/2	See Jmpr17-1/2	See Jmpr17-1/2
Jmpr19-1/2	See Jmpr17-1/2	See Jmpr17-1/2	Configure with Jmpr17 for input type (5 V, 7-45V, contact)
Jmpr19-3/4	See Jmpr17-1/2	See Jmpr17-1/2	See Jmpr19-1/2
Jmpr20-1/2	'P2' Opto-Isolated Digital Input – bit 8	See Fig. 5	Configure with Jmpr22 for input type (5 V, 7-45V, contact)
Jmpr20-3/4	See Jmpr20-1/2	See Jmpr20-1/2	See Jmpr20-1/2
Jmpr20-5/6	See Jmpr20-1/2	See Jmpr20-1/2	See Jmpr20-1/2
Jmpr22-1/2	See Jmpr20-1/2	See Jmpr20-1/2	Configure with Jmpr20 for input type (5 V, 7-45V, contact)
Jmpr22-3/4	See Jmpr20-1/2	See Jmpr20-1/2	See Jmpr22-1/2
Jmpr21-1/2	'P2' Opto-Isolated Digital Input – bit 9	See Fig. 5	Configure with Jmpr23 for input type (5 V, 7-45V, contact)
Jmpr21-3/4	See Jmpr21-1/2	See Jmpr21-1/2	See Jmpr21-1/2
Jmpr21-5/6	See Jmpr21-1/2	See Jmpr21-1/2	See Jmpr21-1/2
Jmpr23-1/2	See Jmpr21-1/2	See Jmpr21-1/2	Configure with Jmpr21 for input type (5 V, 7-45V, contact)
Jmpr23-3/4	See Jmpr21-1/2	See Jmpr21-1/2	See Jmpr23-1/2
Jmpr24-1/2	'P2' Opto-Isolated Digital Input – bit 10	See Fig. 5	Configure with Jmpr26 for input type (5 V, 7-45V, contact)
Jmpr24-3/4	See Jmpr24-1/2	See Jmpr24-1/2	See Jmpr24-1/2
Jmpr24-5/6	See Jmpr24-1/2	See Jmpr24-1/2	See Jmpr24-1/2
Jmpr26-1/2	See Jmpr24-1/2	See Jmpr24-1/2	Configure with Jmpr24 for input type (5 V, 7-45V, contact)
Jmpr26-3/4	See Jmpr24-1/2	See Jmpr24-1/2	See Jmpr26-1/2
Jmpr25-1/2	'P2' Opto-Isolated Digital Input – bit 11	See Fig. 5	Configure with Jmpr27 for input type (5 V, 7-45V, contact)
Jmpr25-3/4	See Jmpr25-1/2	See Jmpr25-1/2	See Jmpr25-1/2
Jmpr25-5/6	See Jmpr25-1/2	See Jmpr25-1/2	See Jmpr25-1/2
Jmpr27-1/2	See Jmpr25-1/2	See Jmpr25-1/2	Configure with Jmpr25 for input type (5 V, 7-45V, contact)
Jmpr27-3/4	See Jmpr25-1/2	See Jmpr25-1/2	See Jmpr27-1/2
Jmpr28-1/2	'P2' Opto-Isolated Digital Input – bit 12	See Fig. 5	Configure with Jmpr30 for input type (5 V, 7-45V, contact)
Jmpr28-3/4	See Jmpr28-1/2	See Jmpr28-1/2	See Jmpr28-1/2
Jmpr28-5/6	See Jmpr28-1/2	See Jmpr28-1/2	See Jmpr28-1/2
Jmpr30-1/2	See Jmpr28-1/2	See Jmpr28-1/2	Configure with Jmpr28 for input type (5 V, 7-45V, contact)
Jmpr30-3/4	See Jmpr28-1/2	See Jmpr28-1/2	See Jmpr30-1/2

Table 2: Configuration Jumper Plugs

(part 4 of 4)

Jumper ID	Description	Position	Operation
Jmpr29-1/2	'P2' Opto-Isolated Digital Input – bit 13	See Fig. 5	Configure with Jmpr31 for input type (5 V, 7-45V, contact)
Jmpr29-3/4	See Jmpr29-1/2	See Jmpr29-1/2	See Jmpr29-1/2
Jmpr29-5/6	See Jmpr29-1/2	See Jmpr29-1/2	See Jmpr29-1/2
Jmpr31-1/2	See Jmpr29-1/2	See Jmpr29-1/2	Configure with Jmpr29 for input type (5 V, 7-45V, contact)
Jmpr31-3/4	See Jmpr29-1/2	See Jmpr29-1/2	See Jmpr31-1/2
Jmpr32-1/2	'P2' Opto-Isolated Digital Input – bit 14	See Fig. 5	Configure with Jmpr34 for input type (5 V, 7-45V, contact)
Jmpr32-3/4	See Jmpr32-1/2	See Jmpr32-1/2	See Jmpr32-1/2
Jmpr32-5/6	See Jmpr32-1/2	See Jmpr32-1/2	See Jmpr32-1/2
Jmpr34-1/2	See Jmpr32-1/2	See Jmpr32-1/2	Configure with Jmpr32 for input type (5 V, 7-45V, contact)
Jmpr34-3/4	See Jmpr32-1/2	See Jmpr32-1/2	See Jmpr34-1/2
Jmpr33-1/2	'P2' Opto-Isolated Digital Input – bit 15	See Fig. 5	Configure with Jmpr35 for input type (5 V, 7-45V, contact)
Jmpr33-3/4	See Jmpr33-1/2	See Jmpr33-1/2	See Jmpr33-1/2
Jmpr33-5/6	See Jmpr33-1/2	See Jmpr33-1/2	See Jmpr33-1/2
Jmpr35-1/2	See Jmpr33-1/2	See Jmpr33-1/2	Configure with Jmpr33 for input type (5 V, 7-45V, contact)
Jmpr35-3/4	See Jmpr33-1/2	See Jmpr33-1/2	See Jmpr35-1/2

Table 3: General Timing Values for the DITS

The table below shows estimates of timing parameters for the DITS. There are three system clocks on the DITS that influence the exact timing results: 80 MHz, 32 MHz, and 20 Hz.

Description	Time	units	Comment
FPDP bus frequency and FPDP word-output	16	MHz	
Maximum Sample Clock Frequency	500	KHz	Based upon an 8-word DITS block written in response to the Sample Clock. No minimum frequency.
Delay after Sample Clock's leading edge until first FPDP word	1100	ns	
Delay after Sample Clock's leading edge until trailing edge of DVALID*	1600	ns	