FPDP Output Module/Analog (FOMA)User's Guide

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1.0 Introduction

The FPDP Output Module/Analog (FOMA) is a VME-format board that provides eight analog outputs that are controlled via commands received from the Front Panel Data Port (FPDP). This document will describe the module's characteristics, configuration, operation, performance constraints, and design reference material. A block diagram of the board is shown in fig. 1.

2.0 References

1) FPDP Specification: VITA 17-199X Rev 1.7, November 24, 1998 *(unapproved version from VITA Standards Organization)*
2) Peer Review for FOMA, P. Sichta, et al, July 11 2006. Some slides updated 18AUG2006.
3) FOMA Software Design Document, M. Isaacs, August 2006.
4) FOMA Design Notebook, R. Marsala office files.
5) Family Tree Drawing for FOMA, B-AE4001, SH 10.

3.0 Module Description

The module is fabricated as a single-width B-Size VME board. The front-panel FPDP bus connection is used to receive 32-bit command words that set the output voltage for each of eight on-board DAC's. The DAC's are 14-bit devices. Each of the 8 DACs has two jumper-selectable single-ended output ranges, +/- 10.24 volts and 0 – 10.24 volts. All eight DAC's can be commanded and their output's settled in under 2 microseconds. The module has all 8 analog outputs available at front-panel 'D' connector and also at the (rear) 'P2' VMEbus connector.

An 8-LED array provides diagnostic and operating information. Two pushbuttons are on the front panel to RESET the module and CLEAR latched LEDs. A few general purpose I/O points are available at the rear VMEbus 'P2' connector.

The FOMA contains a CPLD (Complex Programmable Logic Device) which provides a high degree of flexibility in the module's operating characteristics and on-board diagnostic capability. The module is configurable using on-board jumpers. The jumpers are used to select the module's FPDP address, DAC-update method, and output voltage attributes, etc...

4.0 Module Features

4.1 Mechanical Characteristics

The module is fabricated as a B-Size VME board. The front-panel (fig. 2) is single-width. The board requires only +5V (less than 2A) power from the VME bus, on-board DC-DC converters are used to derive the other voltages (3.3 v, +/- 15 v). It will pass the VMEbus control lines as necessary such that the board will not prevent 'downstream' VME modules from operating correctly. The outer rows (A,C) of the P2 connector are used for board-specific I/O.

4.2 Connectors

Front Panel Connectors

- FPDP (80-pin)
- Analog Outputs (25 pin D female) 0 - 7 (fig. 3)

Rear VMEbus Connectors

- P1 and the center row (B) of P2 are reserved for the normal VMEbus connections.
- The outer rows (A,C) of the P2 connector can optionally be used for board-specific I/O. The board-specific P2 pin assignments are shown on fig. 5. If the P2 pins are used then an *on-board ribbon cable* is used to jumper the P2 analog connections to the front-panel 'D' signals.

On-Board Connectors

- JTAG: A 7-pin JTAG connection is available to program the CPLD. Fig. 9 provides information about the JTAG connections and programs.
- P2 Analog Jumper: Male headers are on-board near the VMEbus P2 connector (J5) and the front panel (J4). If the P2 connector is used for analog I/O, then connect the two headers using a ribbon cable.

4.3 FPDP Interface

The FPDP interface uses a 16 MHz pECL clock; timing for this bus is shown in fig. 6. The FPDP can send a command every ~63 nanoseconds, however the time required to update a DAC is on the order of **180** nanoseconds. A 1024-word FIFO is used to buffer the FPDP data such that the FOMA can accept the commands at the maximum rate, for a limited number of words.

The FIFO will be loaded with all words that are addressed to module type '111'. The CPLD will test for a module address match and parity errors. If all this is OK then the appropriate DAC will be written with the 14-bits of command data. There are two parity groups (and bits) as indicated on fig. 7. Odd parity is used.

If the FOMA has been configured for updating the DACs in the FPDP-Sync mode, then the Sync line on the FPDP port will be used to load all of the DACs with their most-recently-written value. The current plan is to have the FPDP Sync bit active on the final word of the entire command block (i.e. after commands sent to all FPDP output modules).

The FOMA will assert the FPDP lines 'NRFD*' (not ready for data) and 'Suspend*'. These two lines will always present the 'ready' state, even if the FIFO has overflowed to avoid the situation where the commands to other devices on the FPDP bus will not be held up due to a particular FOMA becoming 'full'. When its FIFO is full the FPDP commands will not be received by the module and will be lost.

FPDP Word Format

The FPDP Command Word Format for the FOMA is shown in fig. 7.

4.4 Analog Output Characteristics

Analog Output Key Specifications

Consult the data sheets and schematic diagrams, C-AE4240, for additional details.

- Single-ended outputs.
- Range selectable on a per-channel basis using a jumper. Choices: bipolar (+/- 10.24 v) or unipolar (0-10.24).
- Current Drive capability: +/-150mA through 56 ohms
- Output impedance: 56 Ohms in each lead

- Output Overvoltage/Short-circuit Protection: +/15V maximum, current limited by 56 Ohm resistor
- Output settling time: The DAC has a 0.5 microsecond (f.s. transition) settling time. External capacitors are used to limit the frequency response to 160kHz in bipolar mode and 320 KHz in unipolar mode.
- All analog signals leaving the module are sourced from socketed components.

Analog Data Encoding

Table 1 shows examples of the 14-bit data coding for the two analog output ranges (bipolar/unipolar).

DAC RESET Voltage

Upon power-up or pressing the front-panel RESET button, the DACs will be set to their 'reset voltage'. This voltage is configured for each channel using a jumper plug. The voltage will be either the minimum *or* the midpoint of the DACs full-scale output voltage range.

DAC Analog Value Updates

The DAC's are double-buffered. The DAC *input* register is written with its (14-bit) value by the CPLD when an FPDP command is received with no parity errors. The transfer of the DAC input register to the DAC *output* is done in one of three ways, depending upon a configuration jumper:

- **Asynchronous**: The DAC output is updated by the CPLD immediately after the DAC input register is written.
- **FPDP_Sync**: When the FPDP Sync bit is active (along with DVALID*), all DAC outputs will be updated with the most recent DAC (input) register value. In the Sync mode, the Sync bit will update all DAC's, regardless of whether the module is addressed and regardless of a parity error.
- **External_Sync**: When the External Sync pulse is used (see section 4.8) all DAC outputs will be updated with the most recent DAC (input) register value.

4.5 LEDs

A front-panel array of 8 LED's is used to indicate module activity and status. Figure 2 provides details about the LEDs.

In summary:

- Module +3.3 V power
- FPDP Bus Active
- Module Addressed
- DAC Load (analog outputs updated)
- Parity Error
- FIFO Overload
- Voltage Fault
- Spare

4.6 Front-Panel Switches

There are two momentary front-panel momentary buttons:

- RESET: turns off latched LEDs, resets DAC's, clears FIFO, all CPLD state machines to Idle state.
- LATCH RESET: turns off latched LEDs.

4.7 General Purpose Inputs/Outputs

Eight General Purpose Outputs and Eight General Purpose Inputs are available at the VMEbus P2 connector. These inputs/outputs are connected, via a level shifting buffer, to the CPLD. The inputs can be used to alter the operation of the CPLD while the outputs can be used for monitoring and status. External circuitry must be designed to be electrically compatible with the GP input circuit (see fig.4).

4.8 External Update

The first GP input (P2-C9/A9) has been reserved for use as an external DAC update input. If the module is configured for the 'External Update' mode then the DAC outputs will be updated/loaded on the rising edge of the input signal. External circuitry must be designed to be electrically compatible with the GP input circuit (see fig.4). These inputs and outputs are not electrically isolated. The CPLD logic will ensure proper synchronization with FPDP-initiated DAC-writing operations.

4.9 Keep-Alive

The optional Keep-Alive feature is useful in applications where it is important that the controlled device (e.g. a gas valve) goes to a safe/off state if the module does not receive a command within a specified amount of time.

- The 'keep alive enable' jumper applies to all 8 channels.

- The 'safe state' voltage from the DAC must be the 'reset voltage' as described in section 4.4.
- The keep-alive time is hard-coded into the CPLD software. It will nominally be **100 milliseconds**, but will be capable of being programmed with a range from microseconds thru seconds.

4.10 Test Points

To aid in troubleshooting and design verification there are 32 test points (including 4 ground test points) on the printed circuit board. The test points are described in Table 2.

4.11 Configuration Jumper Summary

Table 3 provides details about all the jumper settings. In summary:

- (6) Module Address (range 0-63. 60-63 reserved).
- (8) Analog Output range.
- (8) Analog Output RESET voltage.
- (1) DAC Update/Load Method (Async, FPDP_Sync, External_Sync).
- (1) Keep-Alive Enable (applies to all channels).
- Spare Jumpers

4.12 Fuses

The table below shows the on-board fuses.

Fuse ID	Description	Rating	Mfgr/Part#
F1	+/- 15 V DC-DC Convertor	4A	Wickmann 396 1400 044
F2	not installed		
F3	3.3 V reg.	1A	Wickmann 396 1100 044

Notes: All fuses are type 'time lag'.

5.0 CPLD Description

The CPLD is a XiLinx product (XC9500XL). The software was developed using XiLinx's ISE WebPACK development tool. The CPLD's software is described in reference 3, the FOMA Software Design Document. The module's block diagram (fig. 1) indicates some of the CPLD's functions.

5.1 Module Throughput

Fig. 9 shows a timing diagram that represents the throughput for the FOMA. Table 4 lists some significant timing values. In general, an FPDP command can be received every 63 ns, the FPDP FIFO is 1024 words deep, and a DAC channel can be processed in about 180 nanoseconds. Words clocked into the FIFO that are not targeted to the module can be processed in about of 64 nanoseconds, slightly slower than the FPDP clock period.

6.0 Figures & Tables

Figure 1: Block Diagram
Figure 2: Front Panel Layout & LED's
Figure 3: Analog Outputs (Front Panel)
Figure 4: General Purpose I/O Information
Figure 5: VMEbus P2 Connector Pins
Figure 6: FPDP Timing Diagram
Figure 7: FPDP Command Word Format for FOMA
Figure 8: Module Throughput Timing Diagram
Figure 9: JTAG Connector and Reference

Table 1: Analog Data Encoding
Table 2: Test Points (On-board)
Table 3: Configuration Jumper Plugs
Table 4: Hi-Level Module Timing Characteristics

Figure 1: Block Diagram

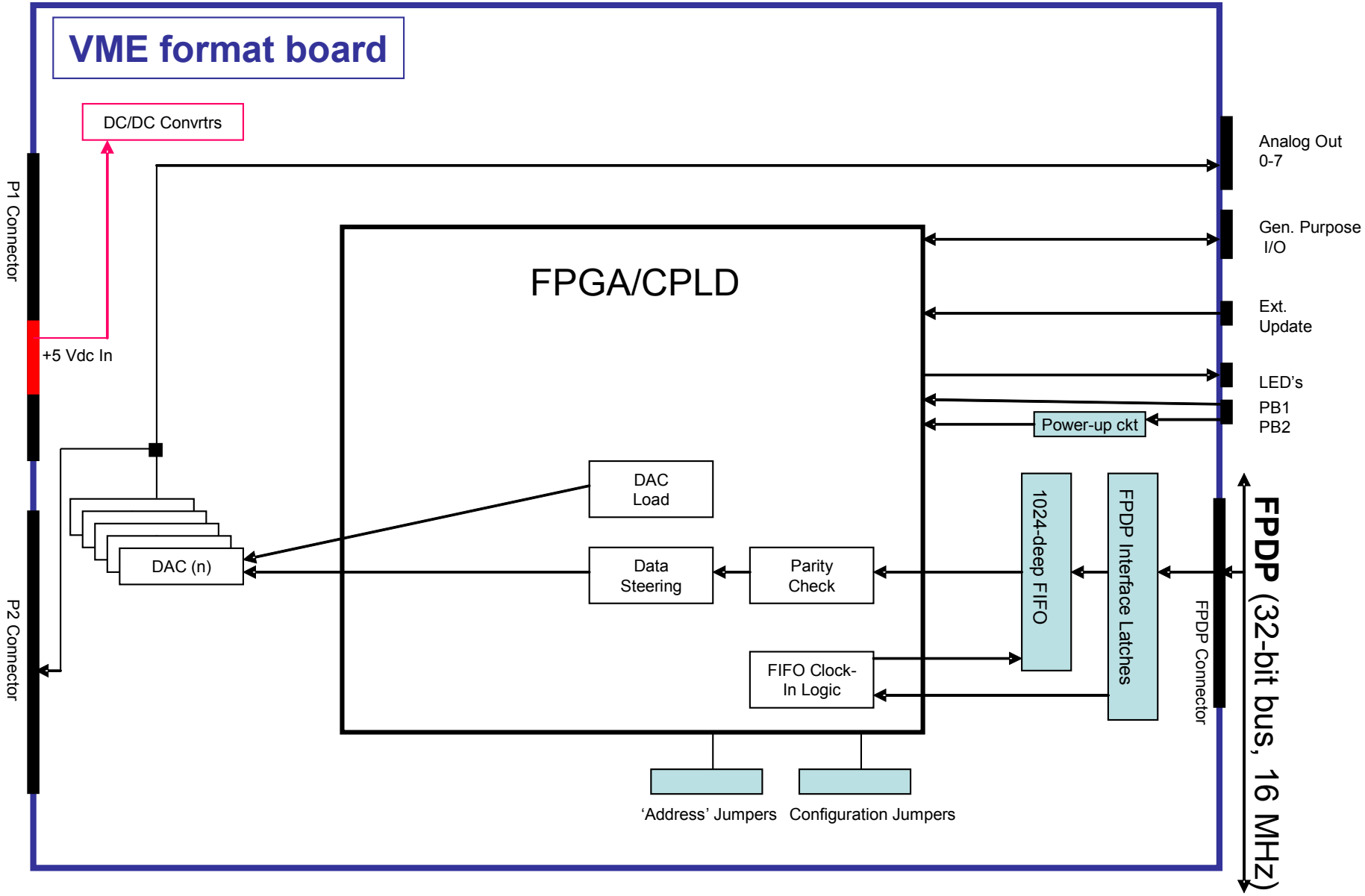
VME format board
DC/DC Convrtrs
P1 Connector
+5 Vdc In
P2 Connector
FPGA/CPLD
Analog Out
0-7
Gen. Purpose
I/O
Ext.
Update
LED's
PB1
PB2
Power-up ckt
DAC
Load
DAC (n)
Data
Steering
Parity
Check
1024-deep FIFO
FPDP Interface Latches
FPDP Connector
FPDP (32-bit bus, 16 MHz)
FIFO Clock-
In Logic
'Address' Jumpers
Configuration Jumpers

Figure 2: Front Panel Layout & LEDs

Description

Power On	Lit when +5 Vdc VMEbus Power is OK
FPDP Active	Flash when any FPDP command occurs
Module Active	Flash when module receives a command
DAC Load	Flash when the DAC outputs are loaded.
Parity Error	Lights (latched) upon detected Data or Address Parity Error
FIFO Error	Lights (latched) upon FIFO overflow condition
Voltage Fault	Lights (latched) upon any out-of-tolerance supply voltage (+15, -15, +5, +3.3)
Spare	

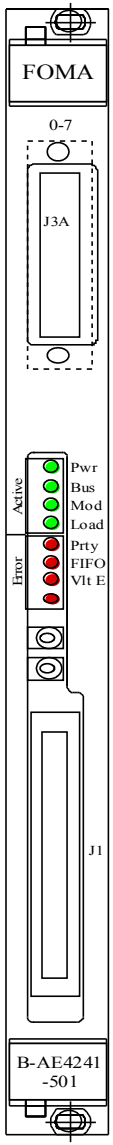

Figure 3: Analog Outputs (Front Panel)

Note: Module uses female (sockets). External mating connector must use DB25P.

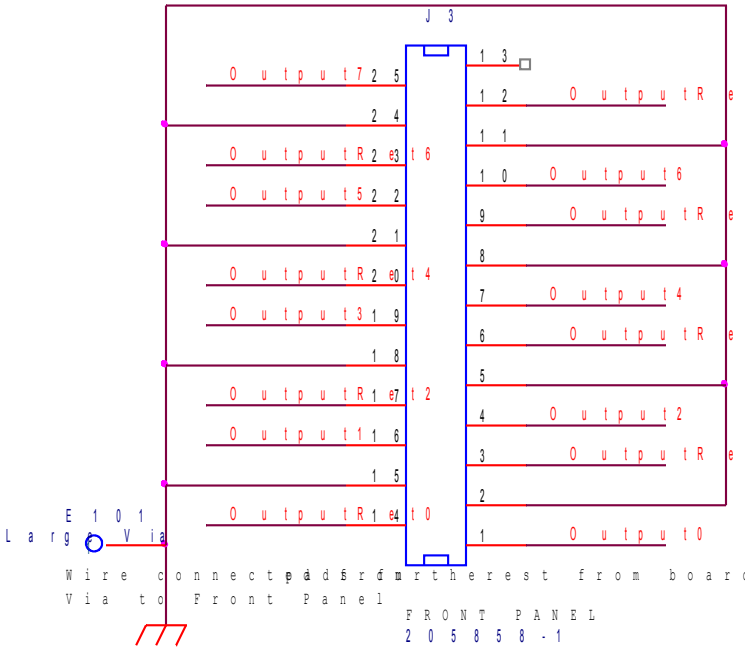

Figure 4: General Purpose I/O Information

Connector P2 Auxillary Input/Outupts

P2 Pin #	Outputs	P2 Pin #	Inputs
C1	Spare Out 0	C9	Spare In 0
C2	Spare Out 1	C10	Spare In 1
C3	Spare Out 2	C11	Spare In 2
C4	Spare Out 3	C12	Spare In 3
C5	Spare Out 4	C13	Spare In 4
C6	Spare Out 5	C14	Spare In 5
C7	Spare Out 6	C15	Spare In 6
C8	Spare Out 7	C16	Spare In 7

- P2-A1 thru P2-A16 are Ground

Table showing basic GP I/O Electrical Characteristics

Description	Value	Unit	Comment
Vin High	2.0	V	Min. (note 2)
Vin Low	0.8	V	Max.
Vout High	4.7	V	Min (@ 24 mA source)
Vout Low	0.55	V	Max (@ 24 mA sink)

1) **Inputs** tied to FOMA internal +5 V supply via 10K resistor. See fig 5.
2) **Max voltage** on any pin w/o damage = 5.5 V.
3) Reference Schematic diagram, C-AE4240 for electrical interface details. Interface device is SN74ACT541E.

Figure 5: VMEbus Connector P2 Input/Outupt

Row A Pin #	Description	Row B Pin #	Description	Row C Pin #	Description
A1	ground	B1	Reserved for VMEbus	C1	Spare Out bit 0
A2	ground	B2	See B1	C2	Spare Out bit 1
A3	ground	B3	See B1	C3	Spare Out bit 2
A4	ground	B4	See B1	C4	Spare Out bit 3
A5	ground	B5	See B1	C5	Spare Out bit 4
A6	ground	B6	See B1	C6	Spare Out bit 5
A7	ground	B7	See B1	C7	Spare Out bit 6
A8	ground	B8	See B1	C8	Spare Out bit 7
A9	ground	B9	See B1	C9	Spare In bit 0
A10	ground	B10	See B1	C10	Spare In bit 1
A11	ground	B11	See B1	C11	Spare In bit 2
A12	ground	B12	See B1	C12	Spare In bit 3
A13	ground	B13	See B1	C13	Spare In bit 4
A14	ground	B14	See B1	C14	Spare In bit 5
A15	ground	B15	See B1	C15	Spare In bit 6
A16	ground	B16	See B1	C16	Spare In bit 7
A17	reserved	B17	See B1	C17	reserved
A18	reserved	B18	See B1	C18	reserved
A19	reserved	B19	See B1	C19	reserved
A20	reserved	B20	See B1	C20	reserved
A21	reserved	B21	See B1	C21	reserved
A22	reserved	B22	See B1	C22	reserved
A23	reserved	B23	See B1	C23	reserved
A24	reserved	B24	See B1	C24	reserved
A25	Ret7	B25	See B1	C25	Analog Out Chan 7
A26	Ret6	B26	See B1	C26	Analog Out Chan 6
A27	Ret5	B27	See B1	C27	Analog Out Chan 5
A28	Ret4	B28	See B1	C28	Analog Out Chan 4
A29	Ret3	B29	See B1	C29	Analog Out Chan 3
A30	Ret2	B30	See B1	C30	Analog Out Chan 2
A31	Ret1	B31	See B1	C31	Analog Out Chan 1
A32	Ret0	B32	See B1	C32	Analog Out Chan 0

- See figure 4 for additional details on Spare/General Purpose inputs and outputs.

- **Figure 6: FPDP Timing Diagram**
  (part 1 of 2)

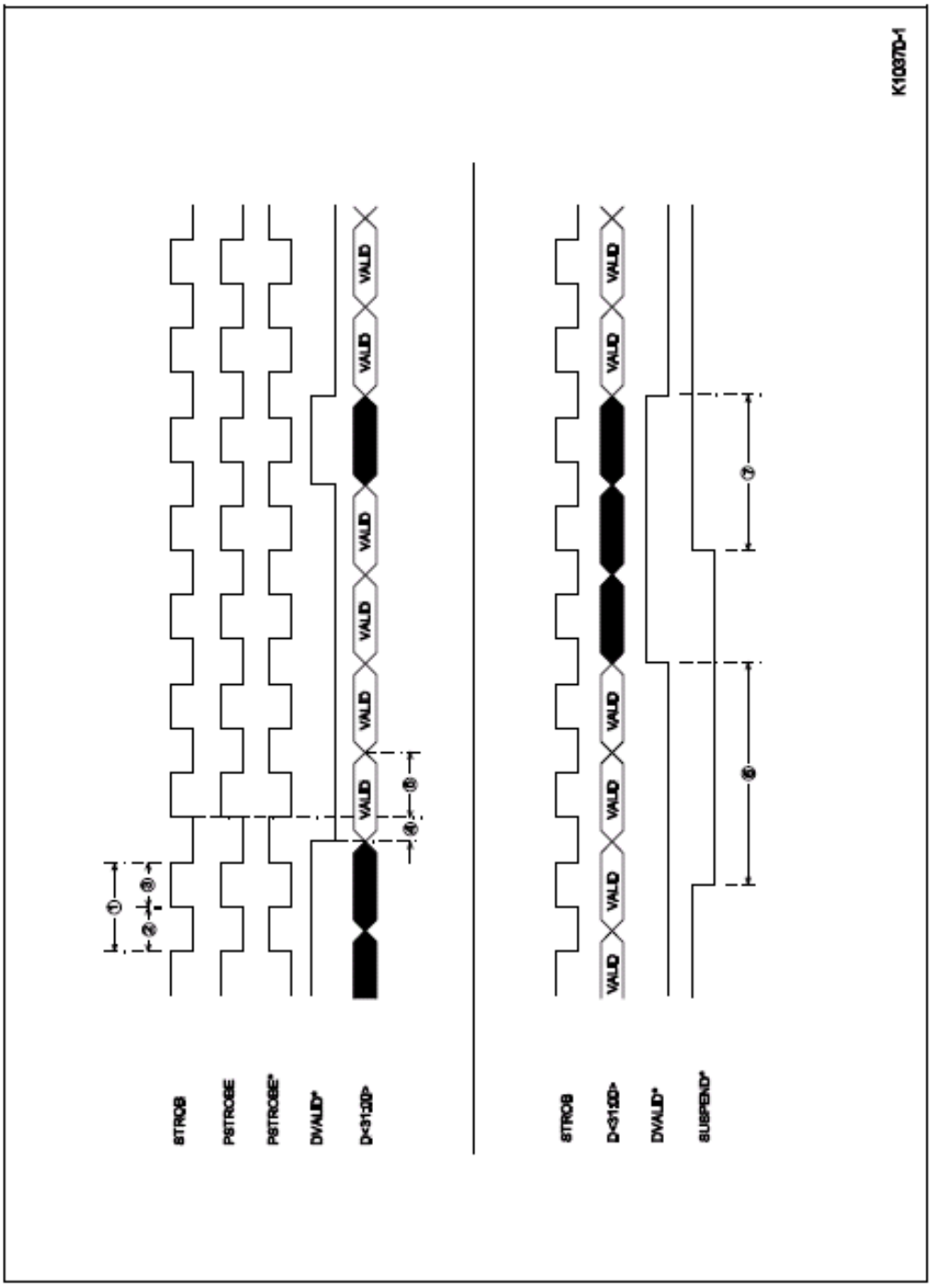

Figure 4 - FPDP Timing Diagrams - All Data Framing Types

Figure 6: FPDP Timing Diagram
(part 2 of 2)

	PARAMETER	At Transmitter End of Cable	At Receiver End of Cable
1	STROB period	25 ns min.	25 ns min.
2	STROB low	10 ns min.	10 ns min.
3	STROB high	10 ns min.	10 ns min.
4	DATA, DVALID* & SYNC* Setup to STROB	5.5 ns min.	4.5 ns min.
5	DATA, DVALID* & SYNC* Hold from STROB	12.0 ns min.	11.0 ns min.
6	SUSPEND* to DVALID* negated	16 STROB max.	16 STROB max.
7	SUSPEND* negated to DVALID* re-asserted	1 STROB min.	1 STROB min.

Note: Parameters 4 and 5 refer to both rising and falling edge transitions of DATA, DVALID* AND SYNC*.

Figure 7: (FPDP) Command Word Format

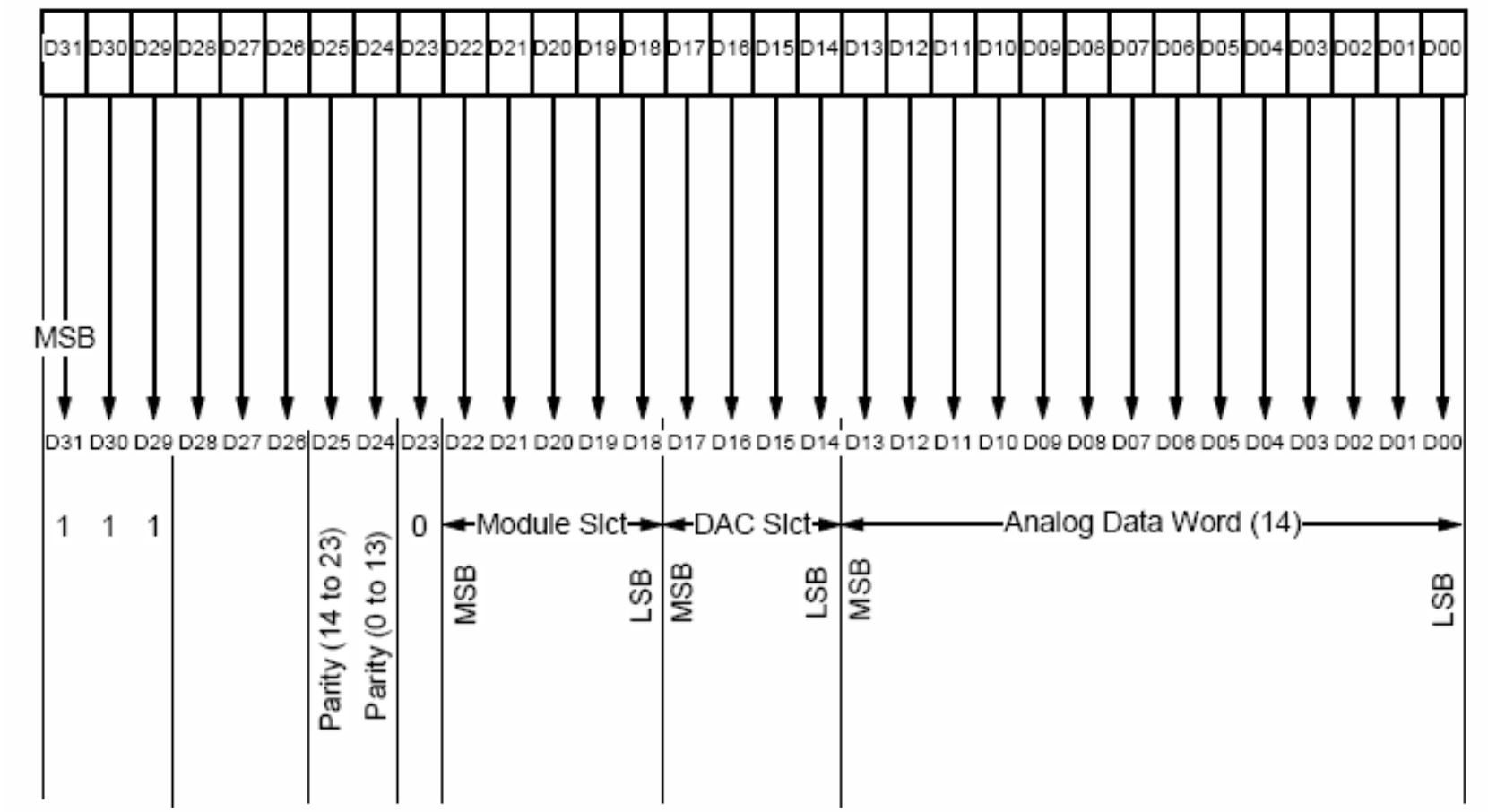

Figure 8: Module Throughput Timing Diagram

Example showing four DAC commands for target module.

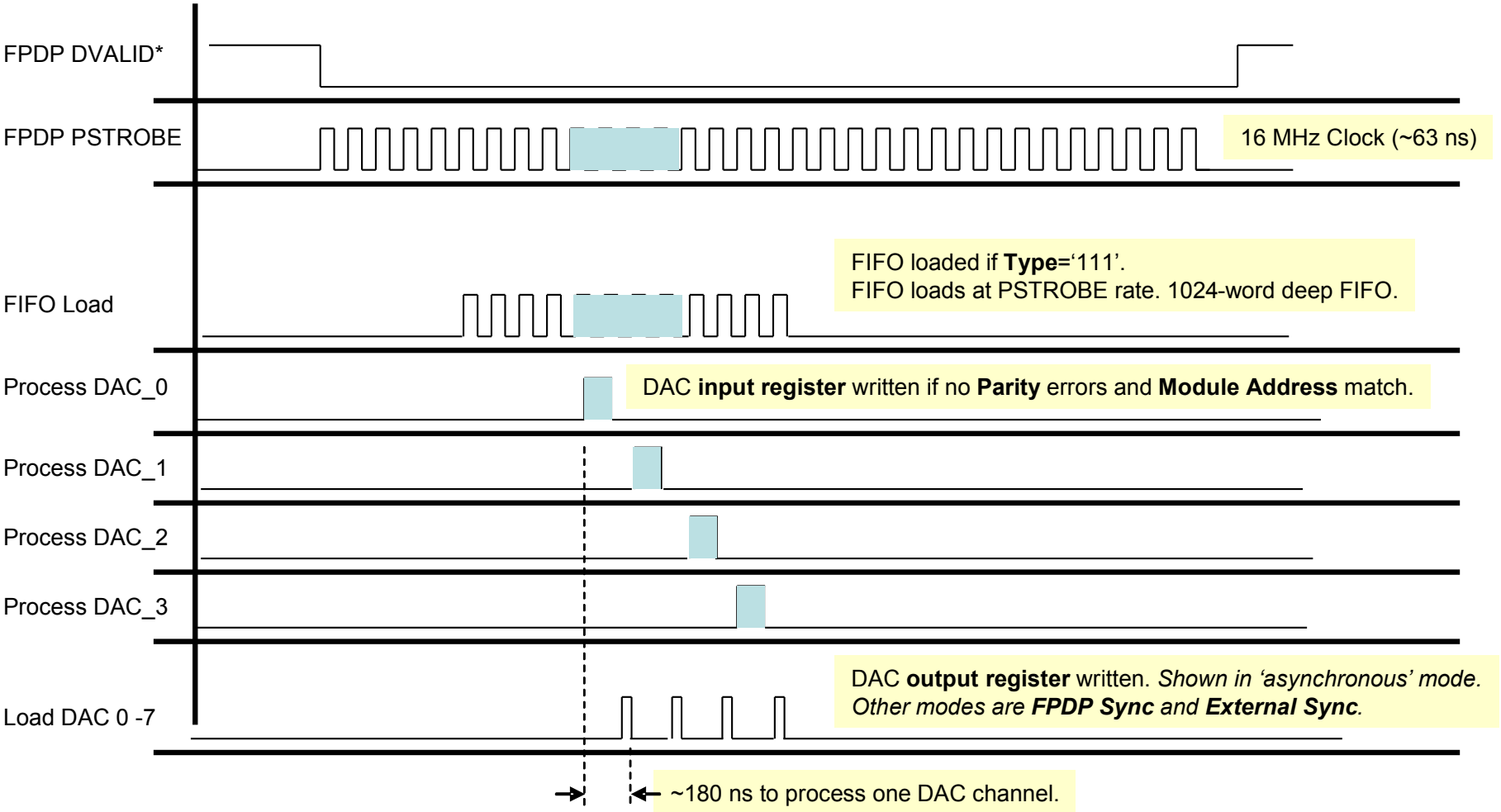

Figure 9: JTAG Connector and Reference

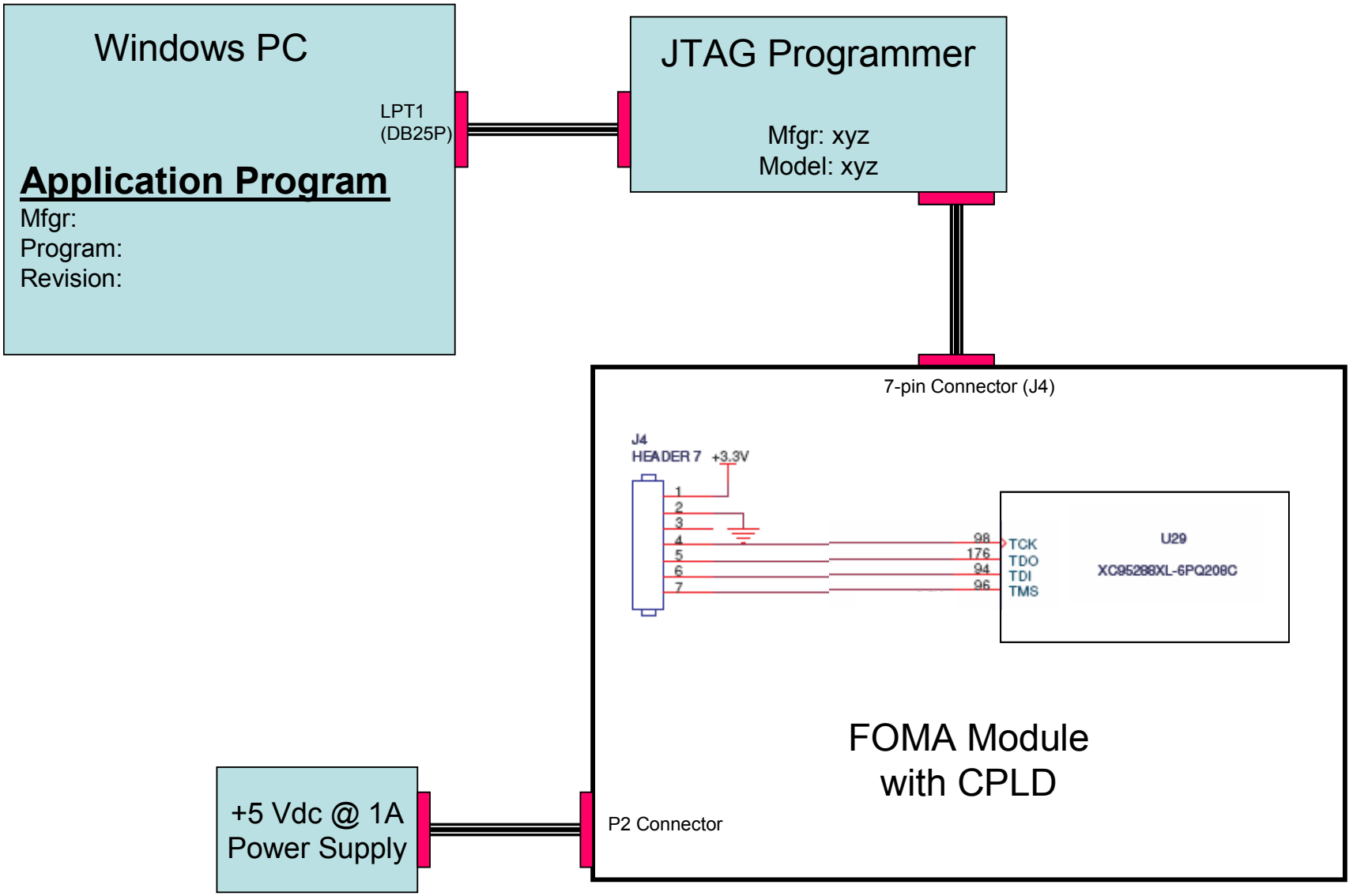
Windows PC
LPT1
(DB25P)
Application Program
Mfgr:
Program:
Revision:
JTAG Programmer
Mfgr: xyz
Model: xyz
7-pin Connector (J4)
J4
HEADER 7
+3.3V
1
2
3
4
5
6
7
98
176
94
96
TCK
TDO
TDI
TMS
U29
XC95288XL-6PQ208C
FOMA Module
with CPLD
+5 Vdc @ 1A
Power Supply
P2 Connector

Table 1: Analog Data Encoding

Analog Data Encoding

Note: DAC's are 14-bit DAC's. The tables below describe the 14-bit word.

Bipolar Output Range +/- 10.24 volts (1.25 millivolts/bit)

signed_decimal_value = output_volts / 0.00125

Data Value (2's compl, decimal)	Data Value (hex, 2's compl, 14-bit)	Output voltage
-8,192	0x2000	-10.24
-4,096	0x3000	-5.12
0000	0x0000	0.000
4,096	0x1000	5.12
8,191	0x1FFF	10.23875

Unipolar Output Range 0 - 10.24 volts (0.625 millivolts/bit)

signed_decimal_value = -8192 + output_volts / 0.000625

Data Value (decimal)	Data Value (hex, 2's compl, 14-bit)	Output voltage
-8,192	0x2000	0.000
0	0x0000	5.12
8,191	0x1FFF	10.239375

Table 2: Test Points (On-board)

Reference schematic diagram for details.

TP	Description
1	BFPDP13, Buffered MSB of Data Word (bit 13)
2	FIFO output MSB of Data Word (bit 13)
3	D13*, CPLD MSB of Data Word (bit 13 inverted)
4	Load DAC (high going edge loads all DACs)
5	FIFO Load Clock (high going edge clocks data into FIFO)
6	FIFO Unload Clock (high going edge clocks data out of FIFO)
7	DVALID* (low level indicates data on the bus is valid)
8	Spare 168 (CPLD pin 168 output)
9	Spare 169 (CPLD pin 169 output)
10	FIFO Sync* (Low going Sync Pulse from FIFO)
11	FIFO Data Valid* (low level indicates data from FIFO is valid)
12	Spare 170 (CPLD pin 170 output)
13	Spare 171 (CPLD pin 171 output)
14	Spare 173 (CPLD pin 173 output)
15	Buffer Data Valid* (low level indicates data from Buffer is valid)
16	Spare 174 (CPLD pin 174 output)
17	Buffer Sync* (Low going Sync Pulse from Buffer)
18	PSTROBE, PECL Levels, High going edge used as clock to buffer
19-22	Ground
23	+15VA
24	+10.24VA
25	-15VA
26	+15VB
27	-10.24VA
28	-15VB
29	+3.3v
30	+10.24vb
31	-10.24vb
32	CPLD Clock

Table 3: Configuration Jumper Plugs

(part 1 of 2)

Jumper ID	Description	Position	Operation
Jmpr1-1/2	Module Address bit 0 - LSB	off on	Binary '1' (note 1) Binary '0'
Jmpr1-3/4	Module Address bit 1	Ref Jmpr1 -1/2	Ref Jmpr1 -1/2
Jmpr1-5/6	Module Address bit 2	Ref Jmpr1 -1/2	Ref Jmpr1 -1/2
Jmpr1-7/8	Module Address bit 3	Ref Jmpr1 -1/2	Ref Jmpr1 -1/2
Jmpr1-9/10	Module Address bit 4	Ref Jmpr1 -1/2	Ref Jmpr1 -1/2
Jmpr1-11/12	Module Address bit 5 - MSB	Ref Jmpr1 -1/2	Ref Jmpr1 -1/2
Jmpr2	DAC Load/update method	b-c b-a off	**External Sync** pulse loads DACs. **FPDP Sync** bit loads DACs. All DACs will load immediately following any of the 8 channel's data write pulse (**Async**). For channel's which are not being written in this cycle, their outputs' will be set to the last-written data.
Jmpr4	Analog output voltage range for Channel 0 of 7	b-c b-a off	+/- 10.24 V 0-10.24 V Invalid
Jmpr5	Analog output voltage range for Channel 1 of 7	Ref Jmpr4	Ref Jmpr4
Jmpr8	Analog output voltage range for Channel 2 of 7	Ref Jmpr4	Ref Jmpr4
Jmpr9	Analog output voltage range for Channel 3 of 7	Ref Jmpr4	Ref Jmpr4
Jmpr12	Analog output voltage range for Channel 4 of 7	Ref Jmpr4	Ref Jmpr4
Jmpr13	Analog output voltage range for Channel 5 of 7	Ref Jmpr4	Ref Jmpr4
Jmpr16	Analog output voltage range for Channel 6 of 7	Ref Jmpr4	Ref Jmpr4
Jmpr17	Analog output voltage range for Channel 7 of 7	Ref Jmpr4	Ref Jmpr4

Notes:
1) 6-bit Module Address value, range 0 - 59. 60-63 are reserved.

Table 3: Configuration Jumper Plugs

(part 2 of 2)

Jumper ID	Description	Position	Operation
Jmpr6	Analog output voltage at RESET for Channel 0 of 7	off on	Output = mid-scale at RESET (note 2) Output = minimum value at RESET (note 3).
Jmpr7	Analog output voltage at RESET for Channel 1 of 7	Ref Jmpr6	Ref Jmpr6
Jmpr10	Analog output voltage at RESET for Channel 2 of 7	Ref Jmpr6	Ref Jmpr6
Jmpr11	Analog output voltage at RESET for Channel 3 of 7	Ref Jmpr6	Ref Jmpr6
Jmpr14	Analog output voltage at RESET for Channel 4 of 7	Ref Jmpr6	Ref Jmpr6
Jmpr15	Analog output voltage at RESET for Channel 5 of 7	Ref Jmpr6	Ref Jmpr6
Jmpr18	Analog output voltage at RESET for Channel 6 of 7	Ref Jmpr6	Ref Jmpr6
Jmpr19	Analog output voltage at RESET for Channel 7 of 7	Ref Jmpr6	Ref Jmpr6
Jmpr3-1/2	**Keep-Alive Control (applies to all DACs)**	**off** **on**	**KA Disabled.** **KA used. Time value per CPLD Software.**
Jmpr3-3/4	SPARE Jumper CPLD pin 199	Ref Jmpr3-15/16	Binary '1' (note 4) Binary '0'
Jmpr3-5/6	SPARE Jumper CPLD pin 200	Ref Jmpr3-15/16	Ref Jmpr3-15/16
Jmpr3-7/8	SPARE Jumper CPLD pin 201	Ref Jmpr3-15/16	Ref Jmpr3-15/16
Jmpr3-9/10	SPARE Jumper CPLD pin 202	Ref Jmpr3-15/16	Ref Jmpr3-15/16
Jmpr3-11/12	SPARE Jumper CPLD pin 203	Ref Jmpr3-15/16	Ref Jmpr3-15/16
Jmpr3-13/14	SPARE Jumper CPLD pin 205	Ref Jmpr3-15/16	Ref Jmpr3-15/16
Jmpr3-15/16	SPARE Jumper CPLD pin 208	n/a	n/a

Notes:
2) Mid-scale value for bipolar output range = 0.000 volts. Mid-scale value for unipolar = 5.12 volts.
3) Minimum value for bipolar output range = -10.24 volts. Minimum value for unipolar range = 0.000 volts.
4) Pin is pulled high (3.3V) with 10k resistor. Jumper ON grounds the point.

Table 4: General Timing Values for the FOMA

The table below shows some timing for various FOMA operations. Many of the times are a function of the CPLD's system clock, so the actual times may vary. The actual system clock will be in the range of 50 MHz – 100 MHz.

Timing for 60 MHz CPLD clock.

Description	Time	units	Comment
FPDP bus frequency	16	MHz	
FIFO Shift-in frequency, upper limit per CPLD programming.	66	MHz	Absolute maximum assuming 50% duty cycle. Based on CPLD combinatorial logic, disregarding actual FIFO limits. FIFO is only rated to 40 MHz.
Delay for first DAC update. Asynchronous DAC load method.	178	ns	Time reference is first DAC word present on FPDP bus. Assume FIFO is empty prior to DAC word.
Delay for 8th DAC update. Asynchronous DAC load method.	1300	ns	Time reference is first DAC word present on FPDP bus. Assume 8 contiguous words. Assume FIFO is empty prior to DAC word.
Delay for external DAC load method	97	ns	Time reference is leading/active edge of external pulse.
Delay for Sync-bit DAC load method	144	ns	Time reference is word with *Sync-bit active* present on FPDP bus. Assume FIFO is empty prior to SYNC word.
Time to inspect and discard a word from the FIFO which is addressed to another module.	64	ns	Start time (0) is the FIFO Shift-Out/Unload clock's active edge. End time is the *next* FIFO Shift-Out/Unload active edge.