FPDP Output Module/Digital (FOMD) User's Guide

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Draft 1	10-16-2006	PS
Rev 0	01-24-2007	PS
Rev 1	24Feb2007	PS

1.0 Introduction

The FPDP Output Module (Digital) (FOMD) is a VME-format board that provides sixtyfour (64) digital outputs that are controlled via commands received from the Front Panel Data Port (FPDP). This document will describe the module's characteristics, configuration, operation, performance constraints, and design reference material. A block diagram of the board is shown in fig. 1.

2.0 References

1) FPDP Specification: *title/rev/date/managing-organization*
2) Peer Review for FOMD, July 12, 2006, per Work Planning Form #1296.
3) FOMD Software Design Document, M. Isaacs, August 2006.
4) FOMD Design Notebook, R. Marsala office files.
4) Family Tree Drawing for FOMD, B-AE4001, SH 11.

3.0 Module Description

The module is fabricated as a B-Size VME board with a single width (4HP by 6U) front panel. The front-panel FPDP bus connection is used to receive 32-bit command words that set the levels for each of four 16-bit on-board latched digital outputs. The 64 latches are set by 4-FPDP words, each word controlling a bank (labeled 0 to 3) of 16-bits. The four banks can be updated in less than 2 microseconds. A notch in the front panel allows four ribbon cables to exit the board. Each of the four cables is configured so that it can be directly connected to an 'Opto 22' relay panel that holds up to 16 output modules. Modules are available with a variety of output characteristics for common controls system applications. In addition the outputs of bank 3 (most significant bank) are interfaced using on-board opto-couplers and connected to the 'P2' VMEbus connector (see fig. 5). Finally, there is one 50-pin connector used to accept 16 input bits from an Opto-22 rack panel which can be outfitted with up to 16 input modules having a range of input characteristics. These bits are routed to the CPLD for applications, such as real-time logic I/O.

An 8-LED array provides diagnostic and operating information. Two pushbuttons are on the front panel to RESET the module and CLEAR latched LEDs. A few general purpose I/O points are available at the rear VMEbus 'P2' connector.

The FOMD contains a CPLD (Complex Programmable Logic Device) which provides a high degree of flexibility in the module's operating characteristics and on-board diagnostic capability. The module is configurable using on-board jumpers. The jumpers are used to select the module's FPDP address and Latch-update method, etc …

4.0 Module Features

4.1 Mechanical Characteristics

The module is fabricated as a B-Size VME board. The front-panel (fig. 2) is single-width (4HP, 0.8"). The board uses +5V an +12V power from the VME bus. Note that the only need of +12V is to power a device that detects out-of-tolerance +5V. It will pass the VMEbus control lines as necessary such that the board will not prevent 'downstream' VME modules from operating correctly. The outer rows (A,C) of the P2 connector are available for board-specific I/O.

4.2 Connectors

Front Panel Connectors

- FPDP (80-pin)

Board Mounted Connectors Accessible Via Front Panel Notch

- 64 Digital Outputs (Four 50-pin headers to interface 4 x 16-bits with Opto-22 rack panel).
- Digital Input (One 50-pin header to interface with an Opto 22 rack panel).

Rear VMEbus Connectors

- P1 and the center row (B) of P2 are reserved for the normal VMEbus connections.
- The outer rows (A, C) of the P2 connector can optionally be used for board-specific I/O. The board-specific P2 pin assignments are shown on fig. 7.
- The FOMD uses the 'P2' connector for 16 opto-coupled digital outputs, 8 general purpose inputs, and 8 general purpose outputs.

On-Board Connectors

- JTAG: A 7-pin JTAG connection is available to program the CPLD. Fig. 11 provides information about the JTAG connections and programs.

4.3 FPDP Interface

The FPDP interface uses a 16 MHz pECL clock; timing for this bus is shown in fig. 8. The FPDP can send a command every ~63 nanoseconds, however the time required to update a 16-bit on-board latch is on the order of 180 nanoseconds. A 1024-word FIFO is used to buffer the FPDP data such that the FOMD can accept the commands at the maximum rate.

The FIFO will be loaded with all words that are addressed to module type '111'. The CPLD will test for a module address match and parity errors. If all this is OK then the appropriate bank will be written with its 16-bits of command data. There are two parity groups (and bits) as indicated on fig. 9. Odd parity is used.

If the FOMD has been configured for updating the banks in the FPDP-Sync mode, then the Sync line on the FPDP port will be used to load all of the banks with their most-recently-written value. The current plan is to have the FPDP Sync bit active on the final word of the entire command block (i.e. after commands sent to all FPDP output modules).

The FOMD will assert the FPDP lines 'NRFD*' (not ready for data) and 'Suspend*'. These two lines will always present the 'ready' state, even if the FIFO has overflowed to avoid the situation where the commands to other devices on the FPDP bus will not be held up due to a particular FOMD becoming 'full'. When its FIFO is full the FPDP commands will not be received by the module and will be lost.

FPDP Word Format

The FPDP Command Word Format for the FOMD is shown in fig. 9.

4.4 Opto-22 Style Digital Output Characteristics

The FOMD provides 4 banks of 16 digital outputs via four 50-pin headers. The headers are located near the front panel and are configured to ribbon-cable directly to an Opto-22 Rack Panel, supporting the G1 and G4 I/O module families. The 'field' side of the Opto-22 modules are compatible with a variety of AC and DC control voltages. The Opto-22 modules provide electrical isolation between the FOMD and the 'field' wiring. Consult the

Opto-22 data sheets and schematic diagram (C-AE4245) for additional details.

- Figure 3 is a portion of the schematic diagram that shows some characteristics of the electrical interface and Opto-22 part references.
- A '1' on the FPDP word's bit location will set the Opto-22 output state to a '1' (5 V). This will cause a 'normally-open/off' Opto-22 output module to enter the 'closed/conducting' state.
- Upon power-up or pressing the front-panel RESET button, the output banks will be cleared to their 'reset/safe' state (logic '0').

Opto-22 Logic Power

- The I/O modules on the Opto-22 rack panel require a source of 5 Vdc power to operate their 'logic' side. The logic power can be supplied by either the DITS or from an external power supply. The modules' 'field' power is electrically isolated from the logic power and is separately supplied by the 'field' electrical system.
- A DITS front-panel LED will illuminate if the +5V Logic power is not present (from either external supply or DITS-sourced via the fuse). This will also be annunciated on the FPDP bus via the module status bits in word 3.
- If the DITS is used to supply the logic power:
  - The DITS 5V VMEbus power is used via a 1A fuse, for each 50-pin header/rack panel.
  - The fuse on the Opto-22 rack panel has no affect.
- If an external 5V power supply is used to supply the logic power:
  - The DITS 5V 1A fuse, for each 50-pin header/rack panel, must be removed.
  - The fuse on the Opto-22 rack panel must be installed.

Digital Output Updates

The output banks are double-buffered. The bank's *data* register is written with its (16-bit) value by the CPLD when an addresses FPDP command is received with no parity errors. The transfer of the bank's *data* register to the bank's buffered *output* register is done in one of three ways, depending upon a configuration jumper:

- **Asynchronous**: The bank's output is updated by the CPLD immediately after the bank *data* register is written.

- **FPDP_Sync** Load: When the FPDP Sync bit is active (along with DVALID*), all bank outputs will be updated with the most recent bank (*data*) register value. In the Sync mode, the Sync bit will update all DAC's, regardless of whether the module is addressed and regardless of a parity error.
  - **External**: When the External Sync pulse is used (see section 4.8) all bank outputs will be updated with the most recent bank (*data*) register value.

Digital Output Bank Reference

Bank ID	50-pin Connector ID	Fuse ID	Keep-Alive Jumper
Output Bank 0	J3	F1	Jmpr3-1/2
Output Bank 1	J4	F2	Jmpr3-1/2
Output Bank 2	J5	F3	Jmpr3-3/4
Output Bank 3	J6	F4	Jmpr3-3/4

4.5 Opto-22 Style Digital Inputs

The FOMD provides one bank of 16 digital inputs via a 50-pin header. The header is located near the front panel and is configured to ribbon-cable directly to an Opto-22 Rack Panel, supporting the G1 and G4 I/O module families. The 'field' side of the Opto-22 modules are compatible with a variety of AC and DC control voltages. The Opto-22 modules provide electrical isolation between the DITS and the 'field' wiring.

- Figure 4 is a portion of the schematic diagram that shows some characteristics of the electrical interface and Opto-22 part references.
- An 'energized' Opto-22 input module will present a logic '1' to the CPLD.

Opto-22 Logic Power

- The I/O modules on the Opto-22 rack panel require a source of 5 Vdc power to operate their 'logic' side. The logic power can be supplied by either the FOMD or from an external power supply. The modules' 'field' power is electrically isolated from the logic power and is separately supplied by the 'field' electrical system.
- A FOMD front-panel LED will illuminate if the +5V Logic power is not present (from either external supply or FOMD-sourced via the fuse). This will also be annunciated on the FPDP bus via the module status bits in word 3.
- If the FOMD is used to supply the logic power:

- The FOMD 5V VMEbus power is used via a 1A fuse, for each 50-pin header/rack panel.
- The fuse on the Opto-22 rack panel has no affect.

o If an external 5V power supply is used to supply the logic power:

- The FOMD 5V 1A fuse, for each 50-pin header/rack panel, must be removed.
- The fuse on the Opto-22 rack panel must be installed.

Digital Input Bank Reference

Bank ID	50-pin Connector ID	Fuse ID
Input Bank (0)	J9	F5

4.6 'P2' Opto-Coupled Digital Outputs

The fourth bank (bank 3) of 16 bits is available at both the Opto-22 style outputs but also at the VMEbus 'P2' connector via 16 on-board opto-couplers. The pinouts are shown on fig. 7 and the electrical characteristics are shown on fig. 5 .

- If the 'P2' opto-cp=oupled outputs are used then an on-board 16-pin ribbon connector must be installed. This is to simplify the PCB layout.

The on-board opto-isolators for bank 3 will enter the 'conducting' state when the command bit is a '1'.

- The basic electrical characteristics of the opto-coupled outputs are:

Output Transistor – Collector to Emitter Basic Electrical Characteristics	
Parameter	**Value**
Breakdown Voltage	30 V
Output voltage at 15 mA collector current	0.4 V
Fmax	150 KHz

4.7 LEDs

A front-panel array of 8 LED's is used to indicate module activity and status. Figure 2 provides details about the LEDs.

In summary:

- Module +5 V power
- FPDP Bus Active
- Module Addressed

- Outputs Loaded (digital outputs updated)
- Data or Address Parity Error
- FIFO Overload
- Voltage Fault
- Opto-22 Logic Power Fault

4.8 Front-Panel Switches

There are two momentary front-panel momentary buttons:

- RESET: turns off latched LEDs, resets output banks (to '0'/off state), clears FIFO, all CPLD state machines to Idle state.
- CLEAR LATCH RESET: turns off latched LEDs.

4.9 General Purpose Inputs/Outputs

Eight General Purpose Outputs and eight General Purpose Inputs are available at the VMEbus P2 connector. These inputs/outputs are connected, via a level shifting buffer, to the CPLD. The inputs can be used to alter the operation of the CPLD while the outputs can be used for monitoring and status. External circuitry must be designed to be electrically compatible with the GP input circuit (see fig. 6).

4.10 External Update

The first GP input (P2-C9/A9) may be used as an external DAC update input. If the module is configured for the 'External Update' mode then the digital outputs will be updated/loaded on the rising edge of the input signal. External circuitry must be designed to be electrically compatible with the GP input circuit (see fig.6). The CPLD logic will ensure proper synchronization with FPDP-initiated bank-writing operations.

4.11 Keep-Alive

The optional Keep-Alive feature is useful in applications where it is important that the controlled device (e.g. a gas valve) goes to a safe/off state if the module does not receive a command within a specified amount of time.

- All output banks will share a keep-alive jumper. The jumper applies to all 16-bits in all banks.
- The 'safe state' output state must be the 'reset state' as described in section 4.4.

- The keep-alive time is hard-coded into the CPLD software. It will nominally be **100 milliseconds**, but will be capable of being programmed with a range from microseconds thru seconds.

4.12 Test Points

To aid in troubleshooting and design verification there are xx test points (including 4 ground test points) on the printed circuit board. The test points are described in Table 2.

4.13 Configuration Jumper Summary

Table 3 provides details about all the jumper settings. In summary:

- (5) Module Address (range 0 -31. 27-31 are reserved).
- (1) Output Update/Load Method (Async, FPDP_Sync, External).
- (1) Keep-Alive Enable (one for all banks).
- Spare Jumpers

4.14 Fuses

The table below shows the on-board fuses.

Fuse ID	Description	Rating	Mfgr/Part#
F1	Opto-22 Output Bank 0 Logic pwr	1A	Wickmann 396 1100 044
F2	Opto-22 Output Bank 1 Logic pwr	1A	Wickmann 396 1100 044
F3	Opto-22 Output Bank 2 Logic pwr	1A	Wickmann 396 1100 044
F4	Opto-22 Output Bank 3 Logic pwr	1A	Wickmann 396 1100 044
F5	Opto-22 Input Bank Logic pwr	1A	Wickmann 396 1100 044
F6	3.3 V reg.	1A	Wickmann 396 1100 044

Notes: All fuses are type 'time lag'.

5.0 CPLD Description

The CPLD is a XiLinx product (XC9500XL). The software was developed using XiLinx's ISE WebPACK development tool. The CPLD's functions and timing diagrams are described in reference 3, the FOMA CPLD Design Notebook. The module's block diagram (fig. 1) indicates some of the CPLD's functions.

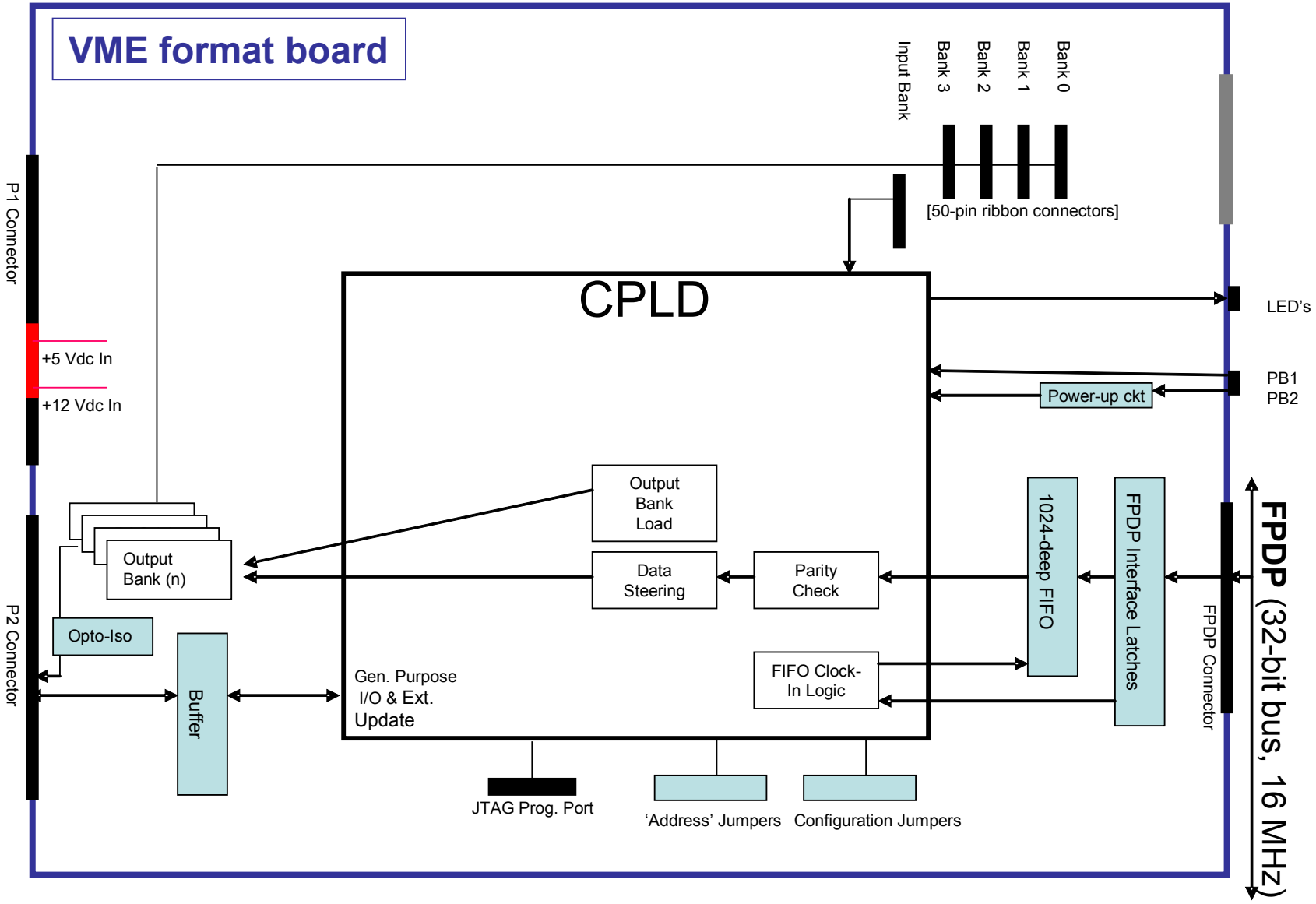
5.1 Module Throughput

Fig. 10 shows a timing diagram that represents the throughput for the FOMD. In general, an FPDP command can be received every 63 ns, the FPDP FIFO is 1024 words deep, and an output bank can be processed in about 100 nanoseconds. Words clocked into the FIFO

that are not targeted to the module can be processed in about of 40 nanoseconds, faster than the FPDP clock period.

6.0 Figures & Tables

Figure 1: Block Diagram



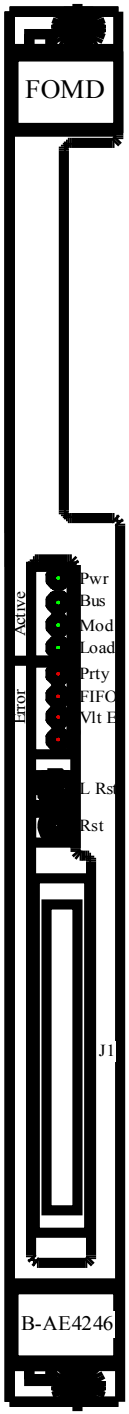
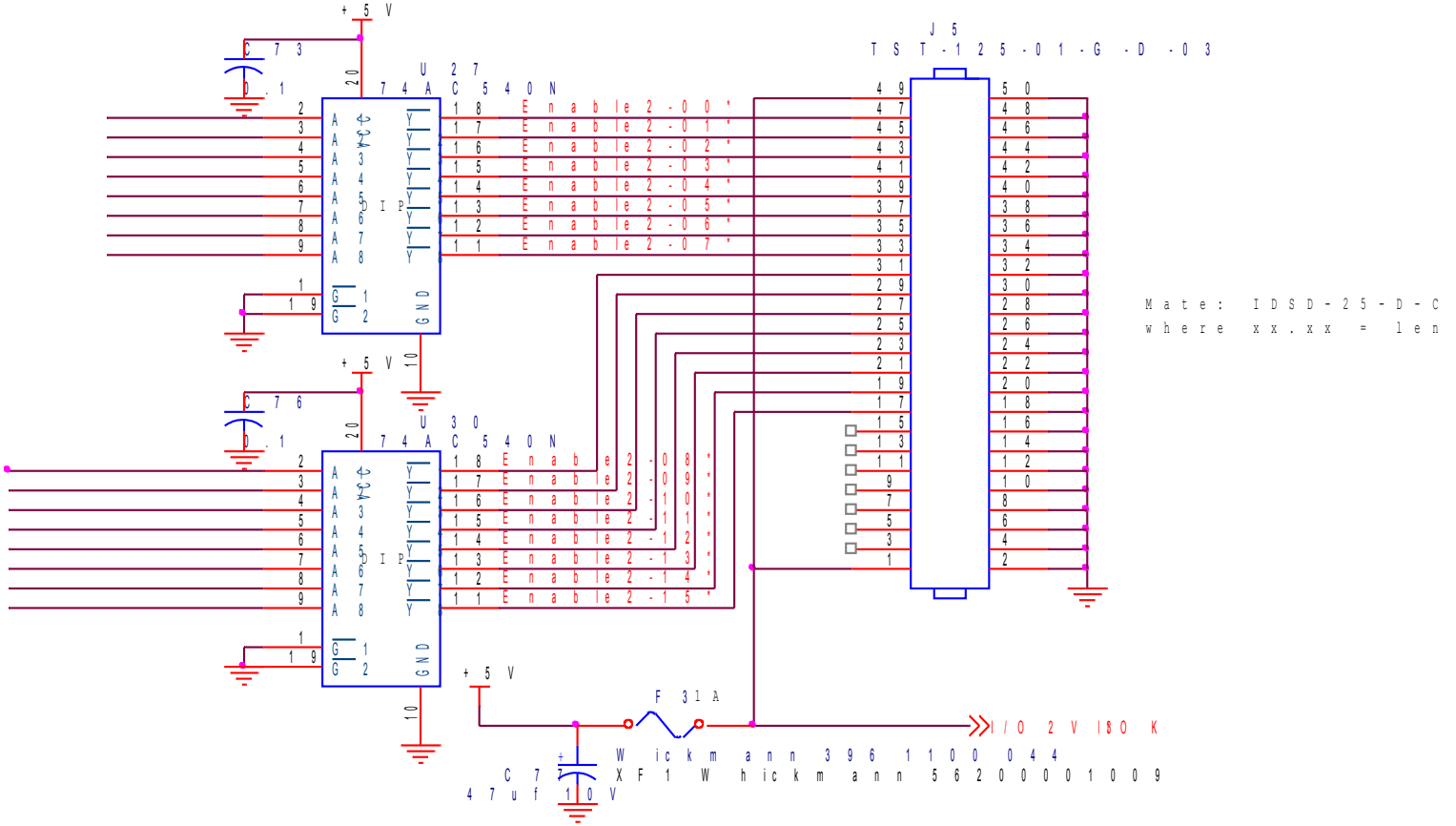


Figure 2: Front Panel Layout & LEDs

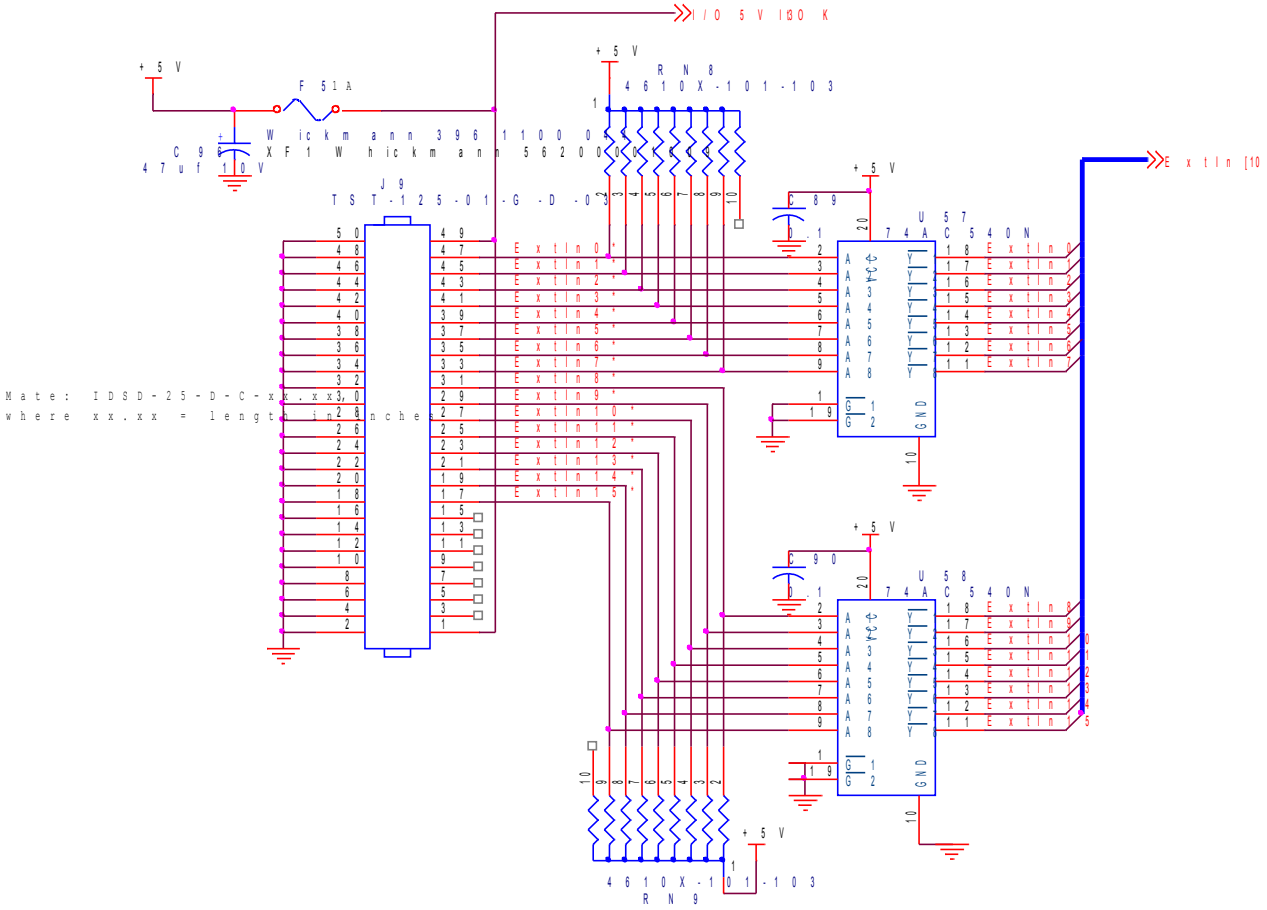
	Description
Power On	Lit when +5 Vdc VMEbus Power is OK
FPDP Active	Flash when any FPDP command occurs
Module Active	Flash when module receives a command
Reg Load	Flash when the Digital Outputs are loaded.
Parity Error	Lights (latched) upon detected Data or Address Parity Error
FIFO Error	Lights (latched) upon FIFO overflow condition
Voltage Fault	Lights (latched) upon any out-of-tolerance supply voltage (+5, +3.3)
I/O Pwr Fault	Lights (not latched) when any Opto-22 Logic Power is bad.

Figure 3: Opto-22 Style Digital Output Signals (front panel notch)



Notes:
1) Single-ended outputs. VoutHi : VoutLow:
2) An Opto-22 rack panel which mates with the DITS 50-pin connector via a ribbon cable is part# PB16H for the G1 I/O module family, or G4PB16H for the G4 I/O module family.
3) If the 'Logic Side' +5V power on the Opto 22 rack panel is **externally supplied** (i.e., external supply is wired to PB16H terminals [+5 & GND]) then **remove the 1A fuse on the FOMD board**. See section 4.14 for a listing of the fuses.

Figure 4: Opto-22 Style Digital Input Signals (front panel notch)



Notes:

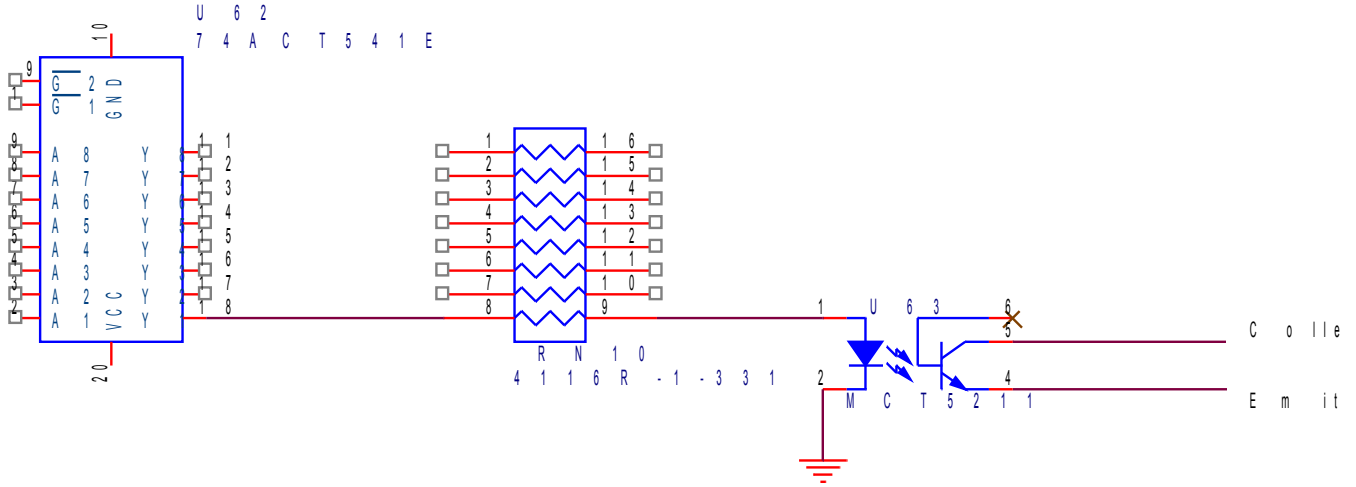
1) Single-ended inputs. Vmax = ____ V Vmin (for a logic '1') = ___ V.

2) An Opto-22 rack panel which mates with the DITS 50-pin connector via a ribbon cable is part# PB16H for the G1 I/O module family, or G4PB16H for the G4 I/O module family.

3) If the 'Logic Side' +5V power on the Opto 22 rack panel is **externally supplied** (i.e., external supply is wired to PB16H terminals [+5 & GND]) then

remove the 1A fuse on the FOMD board. See section 4.14 for a listing of the fuses.

Figure 5: 'P2' Bank 3 Opto-coupled Outputs



Output Transistor – Collector to Emitter Basic Electrical Characteristics	
Parameter	**Value**
Breakdown Voltage	30 V
Output voltage at 15 mA collector current	0.4 V
Max Output Current	Rated to 150 mA (but most you'll get is about 15 mA due to10 mA LED current)
Leakage current with no (LED) diode current	100 nA
Prop delay H-L / L-H	20 uS / 20 uS
Fmax	150 KHz

Notes:
1) Output via MCT5211. A Logic '1' will cause the opto-coupler to conduct.
2) Circuit above typical for 16 outputs.

Figure 6: General Purpose I/O Information

VMEbus Connector 'P2' Auxiliary Input/Outputs

P2 Pin #	Outputs	P2 Pin #	Inputs
C1	Spare Out 0	C9	Spare In 0
C2	Spare Out 1	C10	Spare In 1
C3	Spare Out 2	C11	Spare In 2
C4	Spare Out 3	C12	Spare In 3
C5	Spare Out 4	C13	Spare In 4
C6	Spare Out 5	C14	Spare In 5
C7	Spare Out 6	C15	Spare In 6
C8	Spare Out 7	C16	Spare In 7

- P2-A1 thru P2-A16 are Ground

Table showing basic GP I/O Electrical Characteristics

Description	Value	Unit	Comment
Vin High	2.0	V	Min. (note 2)
Vin Low	0.8	V	Max.
Vout High	4.7	V	Min (@ 24 mA source)
Vout Low	0.55	V	Max (@ 24 mA sink)

1) **Inputs** tied to DITS internal +5 V supply via 10K resistor. See fig 5.
2) **Max voltage** on any pin w/o damage = 5.5 V.
3) Reference Schematic diagram, C-AE4240 for electrical interface details. Interface device is SN74ACT541E.

Figure 7: VMEbus Connector P2 Input/Output

Row A Pin #	Description	Row B Pin #	Description	Row C Pin #	Description
A1	ground	B1	Reserved for VMEbus	C1	Spare Out bit 0
A2	ground	B2	See B1	C2	Spare Out bit 1
A3	ground	B3	See B1	C3	Spare Out bit 2
A4	ground	B4	See B1	C4	Spare Out bit 3
A5	ground	B5	See B1	C5	Spare Out bit 4
A6	ground	B6	See B1	C6	Spare Out bit 5
A7	ground	B7	See B1	C7	Spare Out bit 6
A8	ground	B8	See B1	C8	Spare Out bit 7
A9	ground	B9	See B1	C9	Spare In bit 0
A10	ground	B10	See B1	C10	Spare In bit 1
A11	ground	B11	See B1	C11	Spare In bit 2
A12	ground	B12	See B1	C12	Spare In bit 3
A13	ground	B13	See B1	C13	Spare In bit 4
A14	ground	B14	See B1	C14	Spare In bit 5
A15	ground	B15	See B1	C15	Spare In bit 6
A16	ground	B16	See B1	C16	Spare In bit 7
A17	Emitter bit 15 (-)	B17	See B1	C17	Collector bit 15 (+)
A18	Emitter bit 14 (-)	B18	See B1	C18	Collector bit 14 (+)
A19	Emitter bit 13 (-)	B19	See B1	C19	Collector bit 13 (+)
A20	Emitter bit 12 (-)	B20	See B1	C20	Collector bit 12 (+)
A21	Emitter bit 11 (-)	B21	See B1	C21	Collector bit 11 (+)
A22	Emitter bit 10 (-)	B22	See B1	C22	Collector bit 10 (+)
A23	Emitter bit 9 (-)	B23	See B1	C23	Collector bit 9 (+)
A24	Emitter bit 8 (-)	B24	See B1	C24	Collector bit 8 (+)
A25	Emitter bit 7 (-)	B25	See B1	C25	Collector bit 7 (+)
A26	Emitter bit 6 (-)	B26	See B1	C26	Collector bit 6 (+)
A27	Emitter bit 5 (-)	B27	See B1	C27	Collector bit 5 (+)
A28	Emitter bit 4 (-)	B28	See B1	C28	Collector bit 4 (+)
A29	Emitter bit 3 (-)	B29	See B1	C29	Collector bit 3 (+)
A30	Emitter bit 2 (-)	B30	See B1	C30	Collector bit 2 (+)
A31	Emitter bit 1 (-)	B31	See B1	C31	Collector bit 1 (+)
A32	Emitter bit 0 (-)	B32	See B1	C32	Collector bit 0 (+)

- See figure 6 for additional details on Spare/General Purpose inputs and outputs.

Figure 8: FPDP Timing Diagram
(Part 1 of 2)

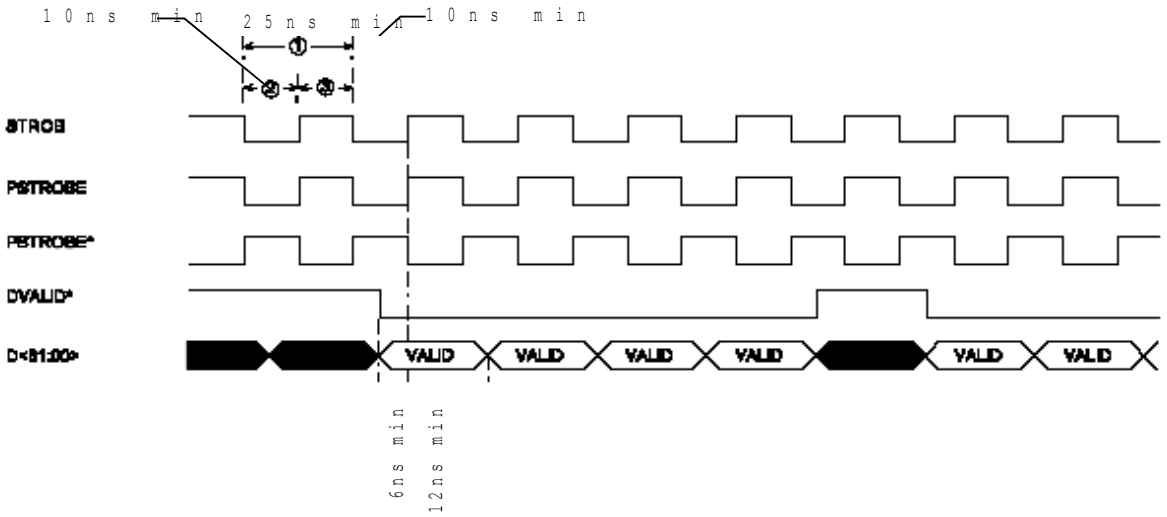


Figure 8: FPDP Timing Diagram
(part 2 of 2)

	PARAMETER	At Transmitter End of Cable	At Receiver End of Cable
1	STROB period	25 ns min.	25 ns min.
2	STROB low	10 ns min.	10 ns min.
3	STROB high	10 ns min.	10 ns min.
4	DATA, DVALID* & SYNC* Setup to STROB	5.5 ns min.	4.5 ns min.
5	DATA, DVALID* & SYNC* Hold from STROB	12.0 ns min.	11.0 ns min.
6	SUSPEND* to DVALID* negated	16 STROB max.	16 STROB max.
7	SUSPEND* negated to DVALID* re-asserted	1 STROB min.	1 STROB min.

Note: Parameters 4 and 5 refer to both rising and falling edge transitions of DATA, DVALID* AND SYNC*.

Figure 9: (FPDP) Command Word Format

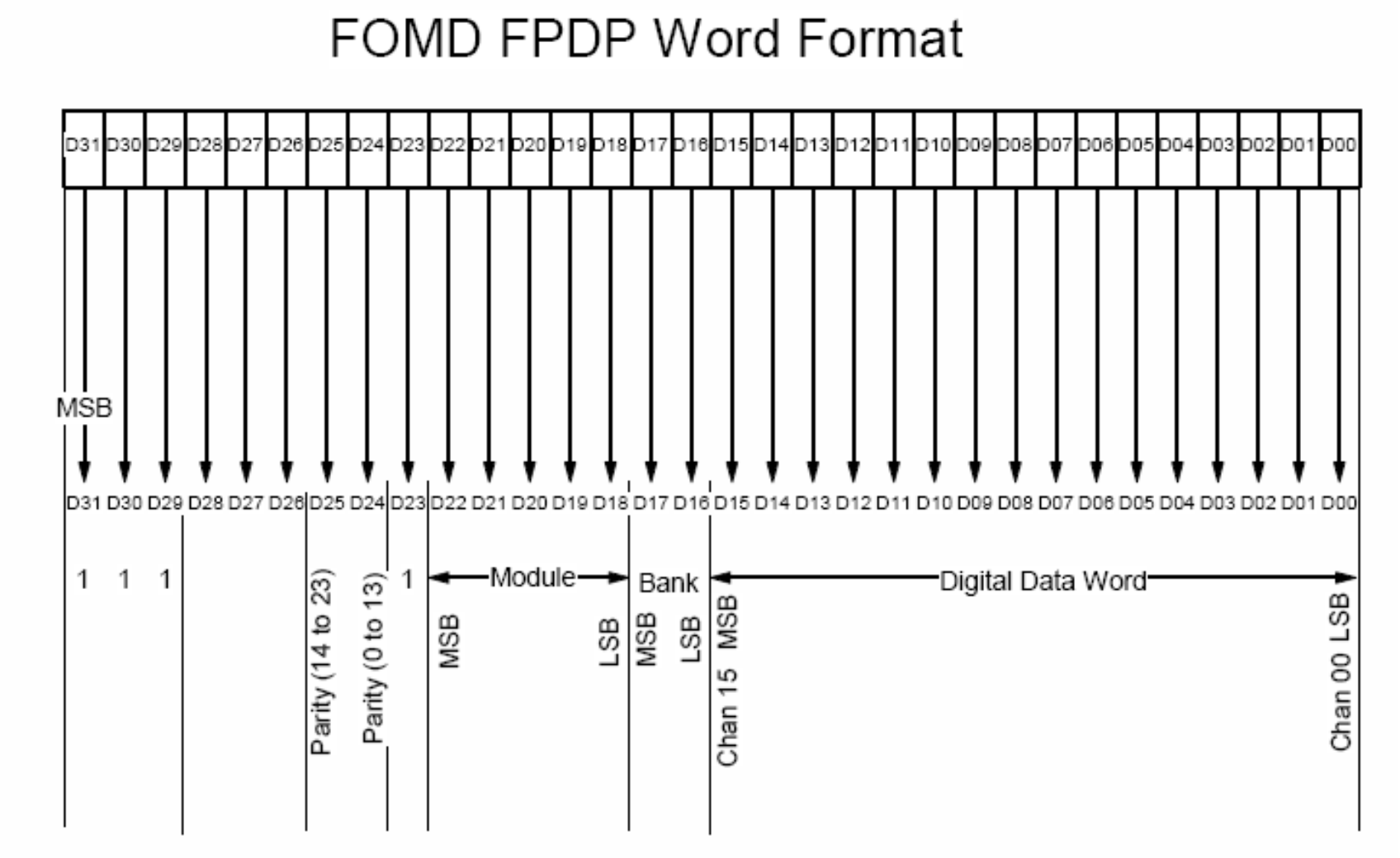


Figure 10: Module Throughput Timing Diagram

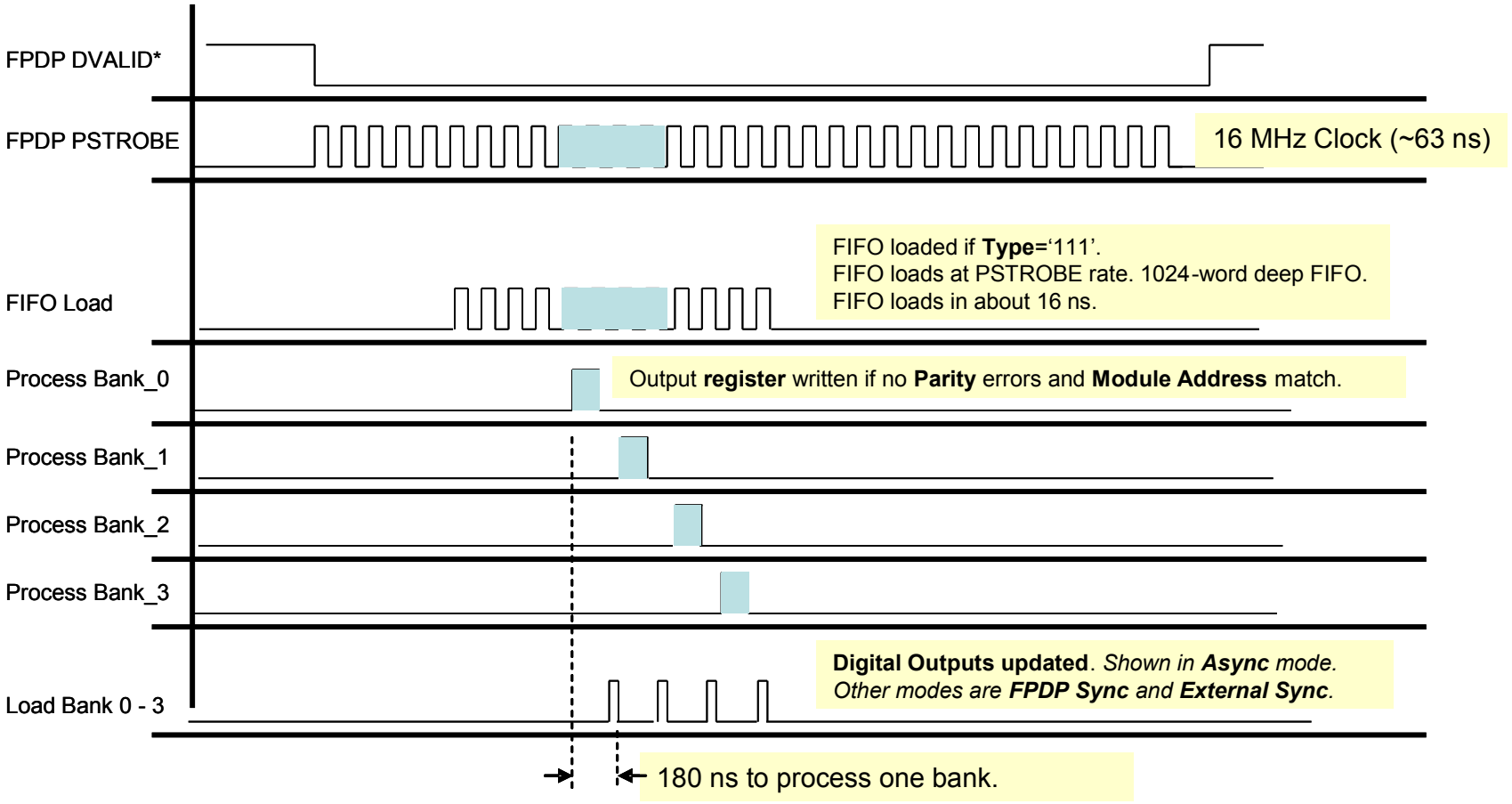


Figure 11: JTAG Connector and Reference

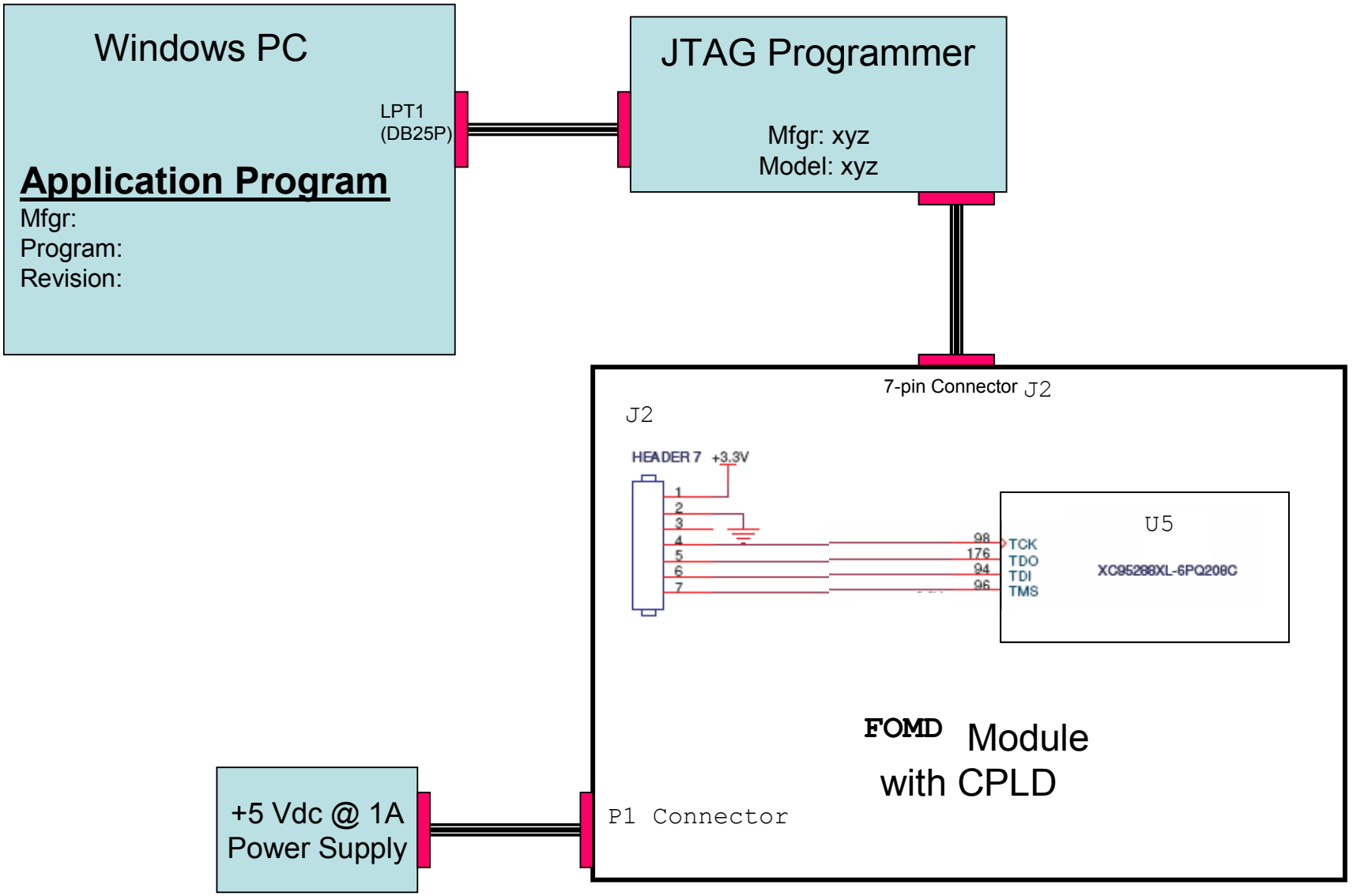

Windows PC
LPT1
(DB25P)
Application Program
Mfgr:
Program:
Revision:
JTAG Programmer
Mfgr: xyz
Model: xyz
7-pin Connector J2
J2
HEADER 7
+3.3V
1
2
3
4
5
6
7
98
176
94
96
TCK
TDO
TDI
TMS
U5
XC95288XL-6PQ208C
FOMD Module
with CPLD
+5 Vdc @ 1A
Power Supply
P1 Connector

Table 1: Test Points

Reference schematic diagram for details.

TP	Description
1	Buffered FPDP Data bit 0/LSB
2	Can't locate this one……..
3	CPLD-output Data bit 15
4	Load Data (high going edge loads all banks)
5	FIFO Load Clock (high going edge clocks data into FIFO)
6	FIFO Unload Clock (high going edge clocks data out of FIFO)
7	DVALID* (direct on bus) (low level indicates data on the bus is valid)
8	Spare 168 (CPLD pin 168 output)
9	Spare 169 (CPLD pin 169 output)
10	FIFO Sync*
11	FIFO Data Valid*
12	Spare 170 (CPLD pin 170 output)
13	Spare 171 (CPLD pin 171 output)
14	Spare 173 (CPLD pin 173 output)
15	BDVALID* (low level indicates data on the bus is valid)
16	Spare 174 (CPLD pin 174 output)
17	BSYNC* (Buffered FPDP SNYC*)
18	P Strobe (buffered version of FPDP bus signal)
19-22	Ground
23	CPLD System Clock
24	+3.3v

Notes:

1) An asterisk '*' at the end of a signal name indicates an ACTIVE LOW signal.

Table 2: Configuration Jumper Plugs

Jumper ID	Description	Position	Operation
Jmpr1-1/2	Module Address bit 0 - LSB	off on	Binary '1' (note 1) to CPLD Binary '0' to CPLD (want this to be a binary '1' for the module address selection?)
Jmpr1-3/4	Module Address bit 1	Ref Jmpr1 -1/2	Ref Jmpr1 -1/2
Jmpr1-5/6	Module Address bit 2	Ref Jmpr1 -1/2	Ref Jmpr1 -1/2
Jmpr1-7/8	Module Address bit 3	Ref Jmpr1 -1/2	Ref Jmpr1 -1/2
Jmpr1-9/10	Module Address bit 4 - MSB	Ref Jmpr1 -1/2	Ref Jmpr1 -1/2
Jmpr2	Output Bank Load/update method	b-c a-b off	• **External Sync** pulse loads banks. • **FPDP Sync** bit loads banks. • All banks will load immediately following any of the 8 channel's data write pulse (**Async**). For channel's which are not being written in this cycle, their outputs' will be set to the last-written data.
Jmpr3-1/2	Keep-Alive Control for Output Banks 0 & 1 & 2 & 3	off on	KA Disabled. KA used. Time value per CPLD Software.
Jmpr3-3/4	SPARE Jumper CPLD pin	off on	not used
Jmpr3-5/6	SPARE Jumper CPLD pin 200	Ref Jmpr3-15/16	Binary '1' (note 2) Binary '0'
Jmpr3-7/8	SPARE Jumper CPLD pin 201	Ref Jmpr3-15/16	Ref Jmpr3-15/16
Jmpr3-9/10	SPARE Jumper CPLD pin 202	Ref Jmpr3-15/16	Ref Jmpr3-15/16
Jmpr3-11/12	SPARE Jumper CPLD pin 203	Ref Jmpr3-15/16	Ref Jmpr3-15/16
Jmpr3-13/14	SPARE Jumper CPLD pin 205	Ref Jmpr3-15/16	Ref Jmpr3-15/16
Jmpr3-15/16	SPARE Jumper CPLD pin 208	off on	Binary '1' to CPLD Binary '0'

Notes:
1) 5-bit Module Address value, range 0 - 27. 28-31 are reserved.
2) Pin is pulled high (3.3V) with 10k resistor. Jumper ON grounds the point.

Table 3: General Timing Values for the FOMD

The table below shows some timing for various FOMD operations. Many of the times are a function of the CPLD's system clock, so the actual times may vary. The actual system clock will be in the range of 50 MHz – 100 MHz.

Timing for 60 MHz CPLD clock.

Description	Time	units	Comment
FPDP bus frequency	16	MHz	
FIFO Shift-in frequency, upper limit per CPLD programming.	66	MHz	Absolute maximum assuming 50% duty cycle. Based on CPLD combinatorial logic, disregarding actual FIFO limits. FIFO is only rated to 40 MHz.
Delay for first Output Bank update. Asynchronous load method.	178	ns	Time reference is first bank word present on FPDP bus. Assume FIFO is empty prior to word.
Delay for 4th bank update. Asynchronous load method.	720	ns	Time reference is first bank word present on FPDP bus. Assume 4 contiguous words. Assume FIFO is empty prior to first word.
Delay for external load method	97	ns	Time reference is leading/active edge of external pulse.
Delay for Sync-bit load method	144	ns	Time reference is word with *Sync-bit active* present on FPDP bus. Assume FIFO is empty prior to SYNC word.
Time to inspect and discard a word from the FIFO which is addressed to another module.	64	ns	Start time (0) is the FIFO Shift-Out/Unload clock's active edge. End time is the *next* FIFO Shift-Out/Unload active edge.