4.4.3. Serial Output Value Updates

The output shift registers are double-buffered. The output holding register is written with its 16 bit value by the CPLD when an FPDP command is received with no parity errors. The transfer of the holding register to the output shift register is done in one of four ways, depending upon a configuration jumper:

- **J5 1-2: 1 to 8 Broadcasting**

When an FPDP command is received at the P.S. address (FPDP word D16D17D18=000), all the 8 P.S. channels output shift register will be updated with the same holding register value. Under this mode, all the FPDP command with different P.S. address will be ignored.

- **J5 3-4: 1 to 4 Broadcasting**

When an FPDP command is received at the P.S. address (FPDP word D16D17D18=000), the P.S. channels 0 to 3 output shift register will be updated with the same holding register value. The FPDP command with P.S. address D16D17D18=010,100,110 will be ignored.

When an FPDP command is received at the P.S. address (FPDP word D16D17D18=001), the P.S. channels 4 to 7 will be updated with the same holding register value. The FPDP command with P.S. address D16D17D18=011,101,111 will be ignored.

- **J5 5-6: 1 to 2 Broadcasting**

When an FPDP command is received:
At address D16D17D18=000, the P.S. channels 0 to 1 output shift registers are updated with the same holding register value.
At address D16D17D18=100, the FPDP command is ignored.

At address D16D17D18=010, the P.S. channels 2 to 3 output shift registers are updated with the same holding register value.
At address D16D17D18=110, the FPDP command is ignored.

At address D16D17D18=001, the P.S. channels 4 to 5 output shift registers are updated with the same holding register value.
At address D16D17D18=101, the FPDP command is ignored.

At address D16D17D18=011, the P.S channels 6 to 7 output shift registers are updated with the same holding register value.
At address D16D17D18=111, the FPDP command is ignored.

• **J5 7-8: 1 to 1 _ Asynchronous**
The output is updated by the CPLD immediately after the holding register is written.

• **J5 open** – error, the Group Address Error light will be ON.

4.8. Keep-Alive

The optional Keep-Alive feature is useful in applications where it is important that the controlled device (e.g. a gas valve) goes to a safe/off state if the module does not receive a command within a specified amount of time.

• The ‘keep alive enable’ jumper applies to all 8 channels.
• The ‘safe state’ value from the shift register must be the ‘reset value’ as described in section 4.4.2.
• The keep-alive time is hard-coded into the CPLD software. It will nominally be 4 milliseconds, but will be capable of being programmed with a range from microseconds thru seconds.

The jumper settings for the keep-alive function are:
• JMPR 3 1-2 – Keep-alive enable
• JMPR 3 3-4 – default to 0x000
• JMPR 3 5-6 – default to 0xFFF
• JMPR 3 7-8 – default to 0x7FF
• JMPR 3 9-10 – default to 0x800
Selecting more than one default level will result in an error condition. The Group Address Error light will be ON.