FPDP Output Module – Serial (FOMS) Specification
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J. E. Lawson

1. Introduction

The FPDP Output Module/Serial (FOMS) is a VME-format board that provides eight serial outputs that are controlled via commands received from the Front Panel Data Port (FPDP). There is an auxiliary output module which can mount to the VME chassis rails, but which does not use any of the VME power or signal lines. There is also a corresponding receiver unit, intended to interface with other equipment such as a Transrex power supply firing generator and fault detector. This document will describe all of the module's characteristics, configuration, operation, performance constraints, and design reference material. A block diagram of the transmitter board is shown in figure 1, the receiver is shown in figure 2.

2. References

1) FPDP Specification: VITA 17-199X Rev 1.7, November 24, 1998 *(unapproved version from VITA Standards Organization)*
2) The VMEbus Specification, Rev C.1, VMEbus International Trade Association, October 1985
3) Family Tree Drawing for FOMS, AE4300.

3. Module Descrptions

3.1. FOMS Transmitter

The transmitter module is fabricated as a 4E, 6U VME board. The front-panel FPDP bus connection is used to receive 32-bit command words that assemble the output word for each of eight on-board shift registers. The shift registers take 12 bits of alpha data, four control bits, an odd parity bit and Manchester encode them as a serial output. All eight output channels can be commanded to update individually or simultaneously. The module has all 8 outputs available at the (rear) 'P2' VME bus connector as well as a 40 pin header. The electrical signals at the 'P2' connector can be connected by a ribbon cable to a paddle board that provides an optical output for each channel as well as an external trigger input and module address switches (see 3.2). A 16-LED array provides diagnostic and operating information. This includes the module and group address as set

by the switch on the paddle board. Two pushbuttons are on the front panel to RESET the module and CLEAR latched LEDs.

The FOMS contains several CPLDs (Complex Programmable Logic Device) which provides a high degree of flexibility in the module's operating characteristics and on-board diagnostic capability. The module is configurable using on-board jumpers. The jumpers are used to select the serial output update method, and test.

3.2. Optical Output

The optical output module is a paddle board with an 8E, 6U front panel, but less than 2" deep behind the panel. The optical output for each channel is available on a 'ST' connector with an 850nm wavelength LED suitable for coupling to a 62.5/125 micron multi-mode fiber. The paddle board also provides the module FPDP address, allowing the FOMS to be changed without requiring jumper changes.

3.3. FOMS Receiver

There are two versions of the FOMS receiver, the unipolar receiver for use with the Transrex firing generators, and the bipolar version for use with the switching power amplifiers (SPA). See figure 2 for an example receiver block diagram.

4. Module Features

4.1. Mechanical Characteristics

The module is fabricated as a B-Size VME board. The front-panel (fig. 2) is single-width. The board requires +5V from the VME bus, on-board DC-DC convertors are used to derive the other voltages (3.3 v). It will pass the VME bus control lines as necessary such that the board will not prevent 'downstream' VME modules from operating correctly. The outer rows (A,C) of the P2 connector are available for board-specific I/O.

4.2. Connectors

Front Panel Connectors

- FPDP (80-pin)

Rear VMEbus Connectors

- P1 and the center row (B) of P2 are reserved for the normal VMEbus connections.
- The outer rows (A,C) of the P2 connector can optionally be used for board-specific I/O. The board-specific P2 pin assignments are shown on fig. 5.

On-Board Connectors

- JTAG: A 7-pin JTAG connection is available to program each of the CPLDs. The JTAG connections are:
- Pin 1 – 3.3V
- Pin 2 – signal ground
- Pin 3 – no connection/ keying
- Pin 4 – TCK
- Pin 5 – TDO
- Pin 6 – TDI
- Pin 7 - TMS

4.3. FPDP Interface

The FPDP interface uses a 16 MHz pECL clock; timing for this bus is shown in fig. 6. The FPDP can send a command every ~63 nanoseconds, however the time required to update an output shift register is on the order of **180** nanoseconds. A 1024-word FIFO is used to buffer the FPDP data such that the FOMS can accept the commands at the maximum rate.

The FIFO will be loaded with all words that are addressed to group select values in the range of '000' to '110' that match the selected group address. The CPLD will test for a module address match and parity errors. If all this is OK then the appropriate output register will be written with the 16 bits of command data.

If the FOMS has been configured for updating the outputs in the FPDP-Sync mode, then the Sync line on the FPDP port will be used to load all of the outputs with their most-recently-written value. The current plan is to have the FPDP Sync bit active on the final word of the entire command block (i.e. after commands sent to all FPDP output modules). Alternately the unit can be set to sync on the FPDP bus P2 line, or on an external input via a 3 pin Lemo on the output paddle board.

The FOMS will assert the FPDP lines 'NRFD*' (not ready for data) and 'Suspend*'. These two lines will always present the 'ready' state, even if the FIFO has overflowed to avoid the situation where the commands to other devices on the FPDP bus will not be held up due to a particular FOMS becoming 'full'. When its FIFO is full the FPDP commands will not be received by the module and will be lost.

The FPDP Command Word Format for the FOMS is shown in figure 5.

4.4. Serial Output Characteristics

4.4.1. Alpha Data Encoding

The 12 bit data coding for the two output ranges are:

Unipolar	Bipolar
0xFFF - 165°	0x7FF - +full scale
0X000 - 0°	0x000 – 0
	0x800 - -full scale

4.4.2. Serial Output RESET Value

Upon power-up or pressing the front-panel RESET button, the output registers will be set to their 'reset value'. This value is configured for all of the channels on a FOMS module using a jumper plug. The value will be either the minimum or the maximum value.

4.4.3. Serial Output Value Updates

The output shift registers are double-buffered. The output holding register is written with its 16 bit value by the CPLD when an FPDP command is received with no parity errors. The transfer of the holding register to the output shift register is done in one of three ways, depending upon a configuration jumper:

- **J5 7-8 - Asynchronous:** The output is updated by the CPLD immediately after the holding register is written.
- **J5 3-4 - FPDP_Sync:** When the FPDP Sync bit is active (along with DVALID*), all outputs will be updated with the most recent holding register value.
- **J5 5-6 - External_Sync:** When the External Sync pulse is used (see section 4.7) all outputs will be updated with the most recent holding register value.

- **J5 1-2 - PIO2_Sync:** This is the same as external sync but the signal comes from the FPDP PIO2 line.
- **J5 open** - error

4.5. Front Panel Indicators

There is an array of 16 LEDs on the front panel which are used to display module activity and status. Figure 2 provides details about these LEDs.

In summary:

- Module +5 V power (green)
- FPDP Bus Active (green)
- Module Addressed (green)
- Output Load (shift register outputs updated) (green)
- Parity Error (red)
- FIFO Overload (red)
- Voltage Fault (red)
- Group address fault (red)
- Group address (3 bits) (yellow)
- Module address (5 bits) (yellow)

4.6. Front Panel Switches

There are two momentary front-panel momentary buttons:

- RESET: turns off the latched LEDs, resets the output shift registers, clears the FIFO and resets the internal state machines to the Idle state.
- LATCH RESET: turns off all latched LEDs.

4.7. External Update

The P2 connector pins (P2-C17/A17) are the external shift register update input. If the module is configured for the 'External Update' mode then the shift register outputs will be loaded on the rising edge of the input signal. The external input is a 5V pulse of at least 1 micro-second duration. The CPLD logic will ensure proper synchronization with FPDP initiated shift register writing operations.

4.8. Keep-Alive

The optional Keep-Alive feature is useful in applications where it is important that the controlled device (e.g. a gas valve) goes to

a safe/off state if the module does not receive a command within a specified amount of time.

- The 'keep alive enable' jumper applies to all 8 channels.
- The 'safe state' value from the shift register must be the 'reset value' as described in section 4.4.2.
- The keep-alive time is hard-coded into the CPLD software. It will nominally be **100 milliseconds**, but will be capable of being programmed with a range from microseconds thru seconds.

The jumper settings for the keep-alive function are:

- JMPR 3 1-2 – Keep-alive enable
- JMPR 3 3-4 – default to 0x000
- JMPR 3 5-6 – default to 0xFFF
- JMPR 3 7-8 – default to 0x7FF
- JMPR 3 9-10 – default to 0x800

Selecting more than one default level will result in an error condition.

4.9. Test Points

To aid in troubleshooting and design verification there are a number of test points on the printed circuit board. The test points are described in Table 1.

4.10. Configuration Jumper Summary

The jumper settings are described in the keep-alive section and the output update sections, the other jumper is:

- JMPR 20 – PSTROBE termination resistor enable

5. CPLD Description

The CPLDs used are the Xilinx XC9500XL series. The software was developed using Xilinx's ISE WebPACK development tool. The CPLD's software is described in reference 3, the FOMS Software Design Document. The module's block diagram (fig. 1) indicates some of the CPLD's functions.

5.1. Module Throughput

Table 2 lists some significant timing values. In general, an FPDP command can be received every 63 ns, the FPDP FIFO is 1024 words deep, and an output channel can be processed in about 180 nanoseconds. Words clocked into the FIFO that are not targeted to the module can be processed in about of 64 nanoseconds, slightly slower than the FPDP clock period.

6. Figures & Tables

Figure 1: Transmitter Block Diagram

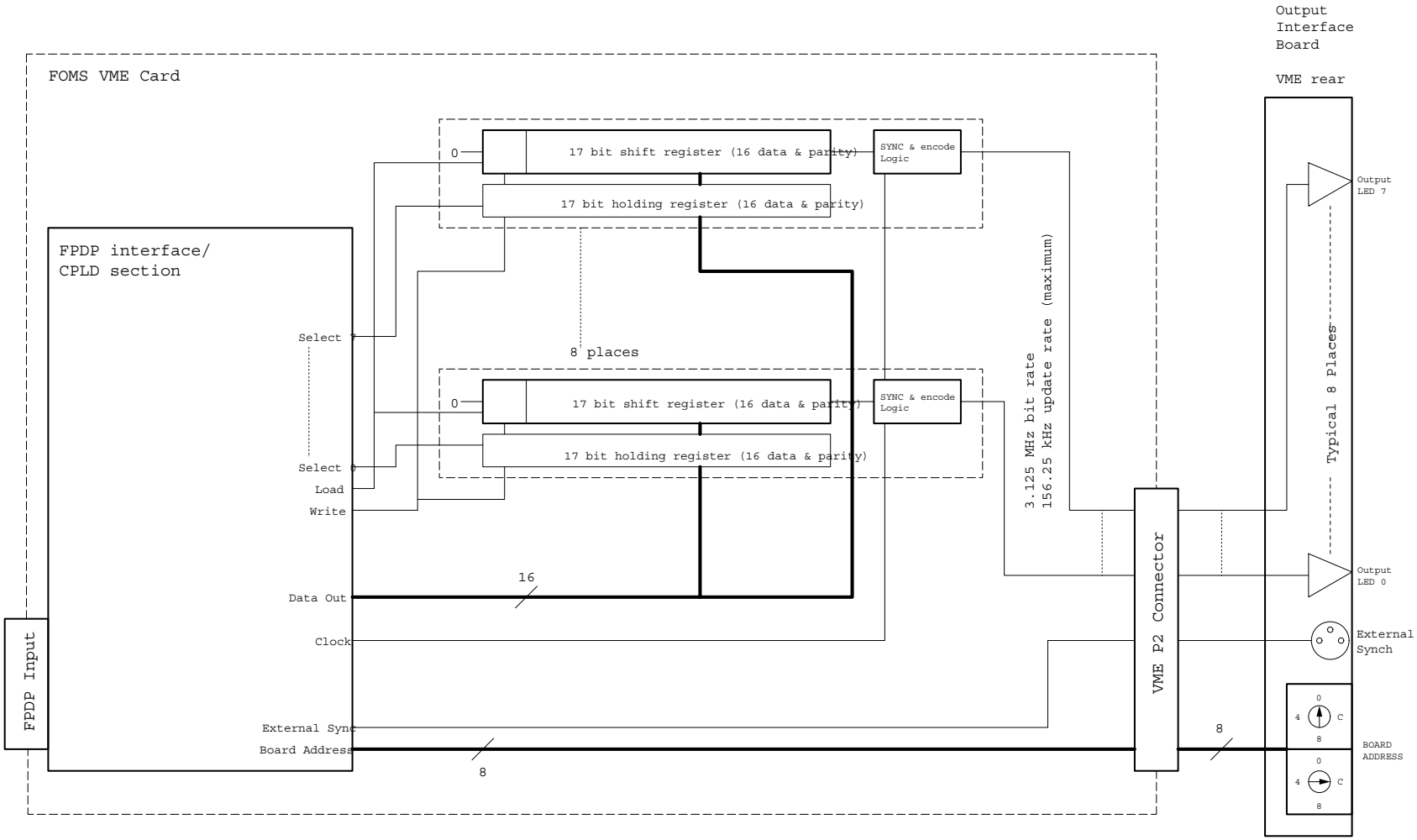
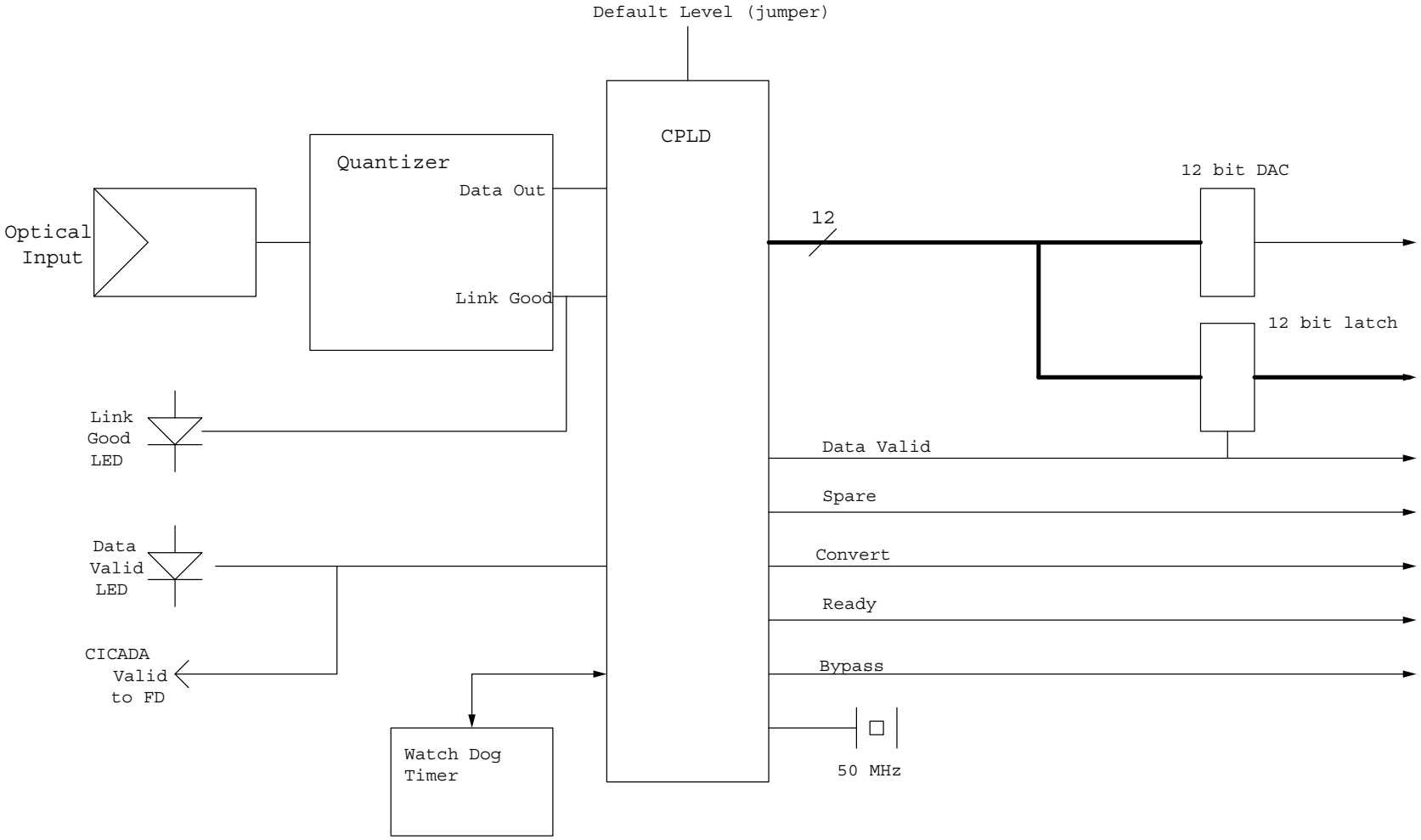


Figure 2: Receiver Block Diagram



FOMS Receiver

Figure 3: Front Panel Layout

GA2 Group Address bit 2
GA1 Group Address bit 1
GA0 Group Address bit 0
MA4 Module Address bit 4
MA3 Module Address bit 3
MA2 Module Address bit 2
MA1 Module Address bit 1
MA0 Module Address bit 0
Pwr Power On
Bus FPDP bus active
Mod Module active
Load Shift register load
Prty FPDP parity error, data or address (latched)
FIFO FIFO overflow (latched)
Vflt Power supply fault (latched)
Adr Group address error (latched)

LRst Latched fault reset
Rst Module reset

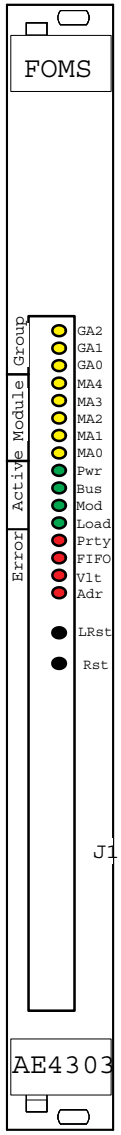


Figure 4: VMEbus Connector P2 Input/Output

Row A Pin #	Description	Row B Pin #	Description	Row C Pin #	Description
A1	ground	**B1**	Reserved for VMEbus	**C1**	Module address bit 0
A2	ground	**B2**	See B1	**C2**	Module address bit 1
A3	ground	**B3**	See B1	**C3**	Module address bit 2
A4	ground	**B4**	See B1	**C4**	Module address bit 3
A5	ground	**B5**	See B1	**C5**	Module address bit 4
A6	ground	**B6**	See B1	**C6**	Group address bit 0
A7	ground	**B7**	See B1	**C7**	Group address bit 1
A8	ground	**B8**	See B1	**C8**	Group address bit 2
A9	ground	**B9**	See B1	**C9**	FOMS out channel 0
A10	ground	**B10**	See B1	**C10**	FOMS out channel 1
A11	ground	**B11**	See B1	**C11**	FOMS out channel 2
A12	ground	**B12**	See B1	**C12**	FOMS out channel 3
A13	ground	**B13**	See B1	**C13**	FOMS out channel 4
A14	ground	**B14**	See B1	**C14**	FOMS out channel 5
A15	ground	**B15**	See B1	**C15**	FOMS out channel 6
A16	ground	**B16**	See B1	**C16**	FOMS out channel 7
A17	ground	**B17**	See B1	**C17**	External synch in
A18	ground	**B18**	See B1	**C18**	+5V
A19	ground	**B19**	See B1	**C19**	+5V
A20	ground	**B20**	See B1	**C20**	+5V
A21	reserved	**B21**	See B1	**C21**	reserved
A22	reserved	**B22**	See B1	**C22**	reserved
A23	reserved	**B23**	See B1	**C23**	reserved
A24	reserved	**B24**	See B1	**C24**	reserved
A25	reserved	**B25**	See B1	**C25**	reserved
A26	reserved	**B26**	See B1	**C26**	reserved
A27	reserved	**B27**	See B1	**C27**	reserved
A28	reserved	**B28**	See B1	**C28**	reserved
A29	reserved	**B29**	See B1	**C29**	reserved
A30	reserved	**B30**	See B1	**C30**	reserved
A31	reserved	**B31**	See B1	**C31**	reserved
A32	reserved	**B32**	See B1	**C32**	reserved

- **Figure 5: (FPDP) Command Word Format**

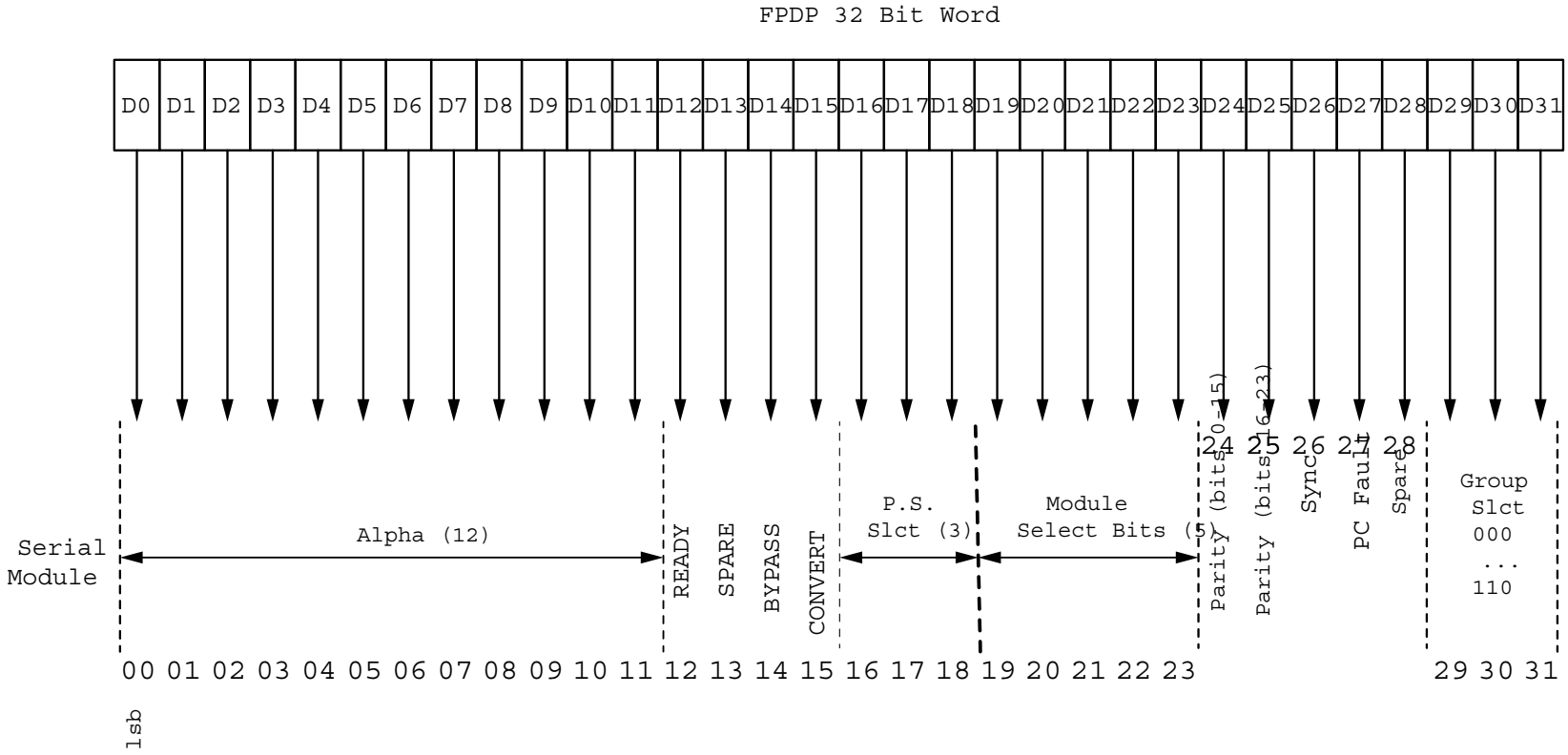
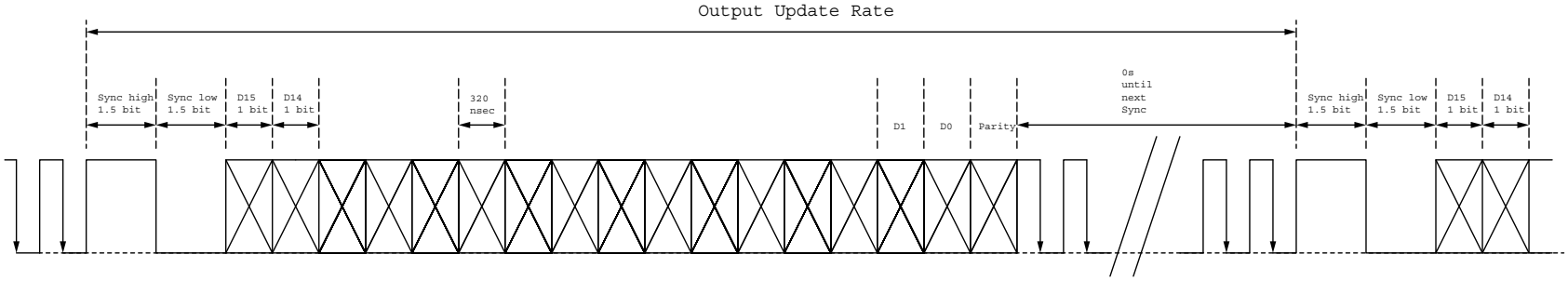
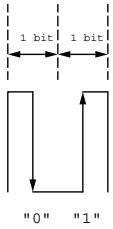


Figure 6: Serial Output Diagram





FOMS Data Format

Table 1: Test Points (On-board)

Reference schematic diagram for details.

TP	Description
1	BFPDP11, Buffered MSB of Data Word (bit 11)
2	FIFO output MSB of Data Word (bit 11)
3	FIFO Load Clock (high going edge clocks data into FIFO)
4	Load shift register (high going edge loads all selected SRs)
5	FIFO Unload Clock (high going edge clocks data out of FIFO)
6	DVALID* (low level indicates data on the bus is valid)
7	Spare 168 (CPLD pin 168 output)
8	Spare 169 (CPLD pin 169 output)
9	FIFO Sync* (Low going Sync Pulse from FIFO)
10	FIFO Data Valid* (low level indicates data from FIFO is valid)
12	Spare 170 (CPLD pin 170 output)
13	Spare 171 (CPLD pin 171 output)
14	Spare 173 (CPLD pin 173 output)
15	Buffer Data Valid* (low level indicates data from Buffer is valid)
16	Spare 174 (CPLD pin 174 output)
17	Buffer Sync* (Low going Sync Pulse from Buffer)
18	PSTROBE, PECL Levels, High going edge used as clock to buffer
19-22	Ground
29	+3.3v
32,45	CPLD Clock
33	+5V
34	Power OK
35	Serial 0,1 CPLD pin 61
36	Serial 0,1 CPLD pin 56
37-44	Serial data out channels 0-7
46	Write shift register to output (high going edge starts all selected SRs)
47	Select shift register 0
48	Select shift register 1

Table 2: General Timing Values for the FOMS

The table below shows some timing for various FOMS operations. Many of the times are a function of the CPLD's system clock, so the actual times may vary. The actual system clock will be in the range of 50 MHz – 100 MHz.

Timing for 60 MHz CPLD clock.

Description	Time	units	Comment
FPDP bus frequency	16	MHz	
FIFO Shift-in frequency, upper limit per CPLD programming.	66	MHz	Absolute maximum assuming 50% duty cycle. Based on CPLD combinatorial logic, disregarding actual FIFO limits. FIFO is only rated to 40 MHz.
Delay for first output update. Asynchronous output load method.	178	ns	Time reference is first DAC word present on FPDP bus. Assume FIFO is empty prior to DAC word.
Delay for 8^{th} output update. Asynchronous output load method.	1300	ns	Time reference is first DAC word present on FPDP bus. Assume 8 contiguous words. Assume FIFO is empty prior to DAC word.
Delay for external output load method	97	ns	Time reference is leading/active edge of external pulse.
Delay for Sync-bit output load method	144	ns	Time reference is word with *Sync-bit active* present on FPDP bus. Assume FIFO is empty prior to SYNC word.
Time to inspect and discard a word from the FIFO which is addressed to another module.	64	ns	Start time (0) is the FIFO Shift-Out/Unload clock's active edge. End time is the *next* FIFO Shift-Out/Unload active edge.