Flexible FPDP I/O and Time Stamping for the NSTX Plasma Control System

M.O. Isaacs, R.J. Marsala, J.E. Lawson, P. Sichta

Princeton Plasma Physics Lab

Princeton University

Princeton, N.J. 08543 USA

Abstract # 117

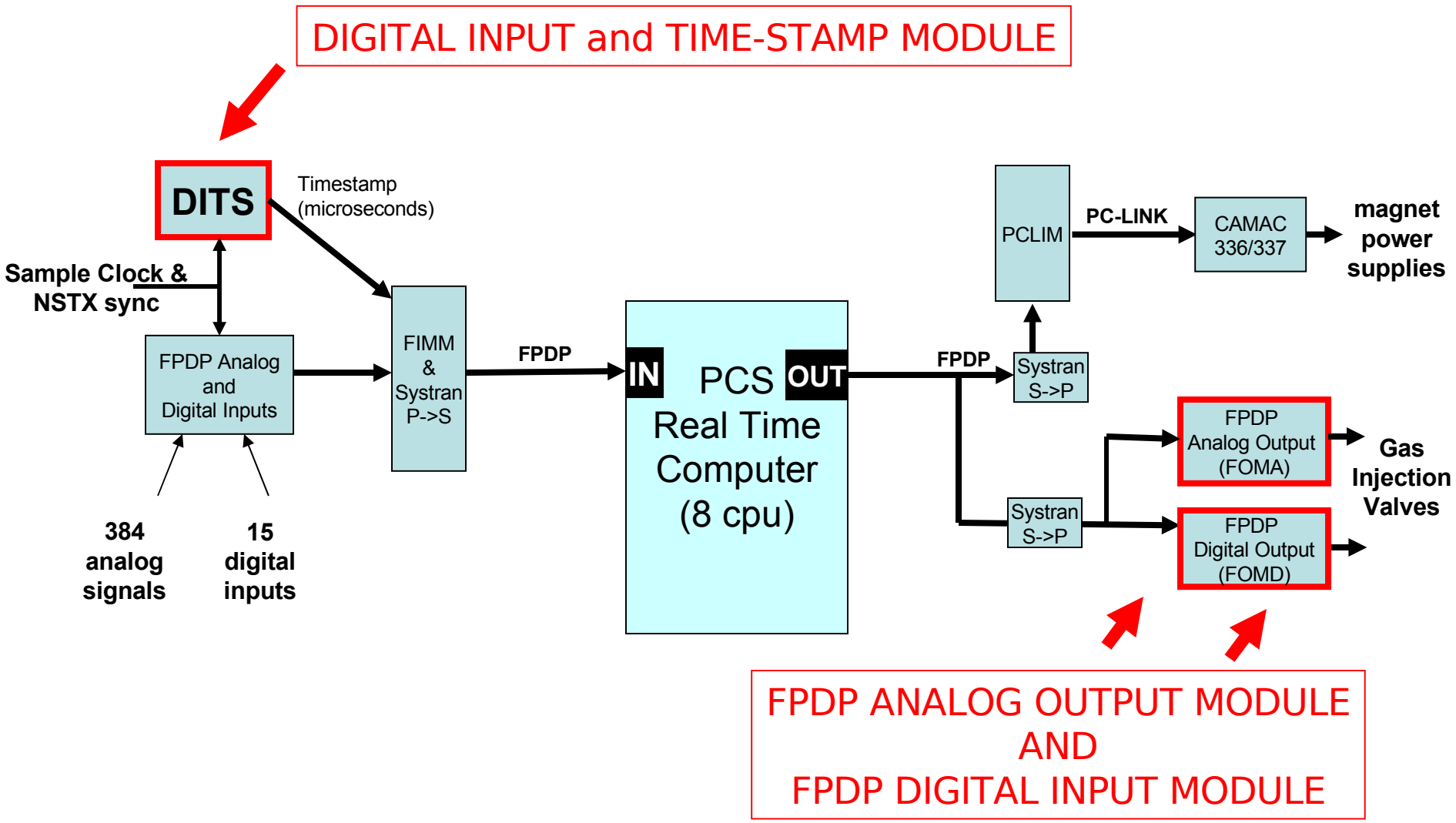
Abstract

As part of the NSTX control systems upgrade, the Digital Input and Timestamp (DITS), FPDP Output Module Digital (FOMD) and Analog (FOMA) have been under development at PPPL. The DITS provides a 48-bit timestamp value, a 32-bit block counter, as well as a total of 56 bits of digital inputs from a variety of sources. The FOMD provides 4 banks of 16-bit digital outputs, while the FOMA has 8 analog channels with 14-bit resolution.

Each board was designed with flexibility in mind, and their functionality and feature sets can be dramatically altered in firmware. The use of programmable logic (CPLD) has reduced hardware complexity substantially and has eased troubleshooting. All three boards were designed for use in VME crates and can access the VME P2 connector, however they don't use the VME bus from primary communication.

Communication between the boards and the central control computer occurs over an FPDP connection. While the boards were designed with gas injection applications in mind, they are flexible enough to be used in other applications.

Plasma Control System Diagram



What is FPDP?

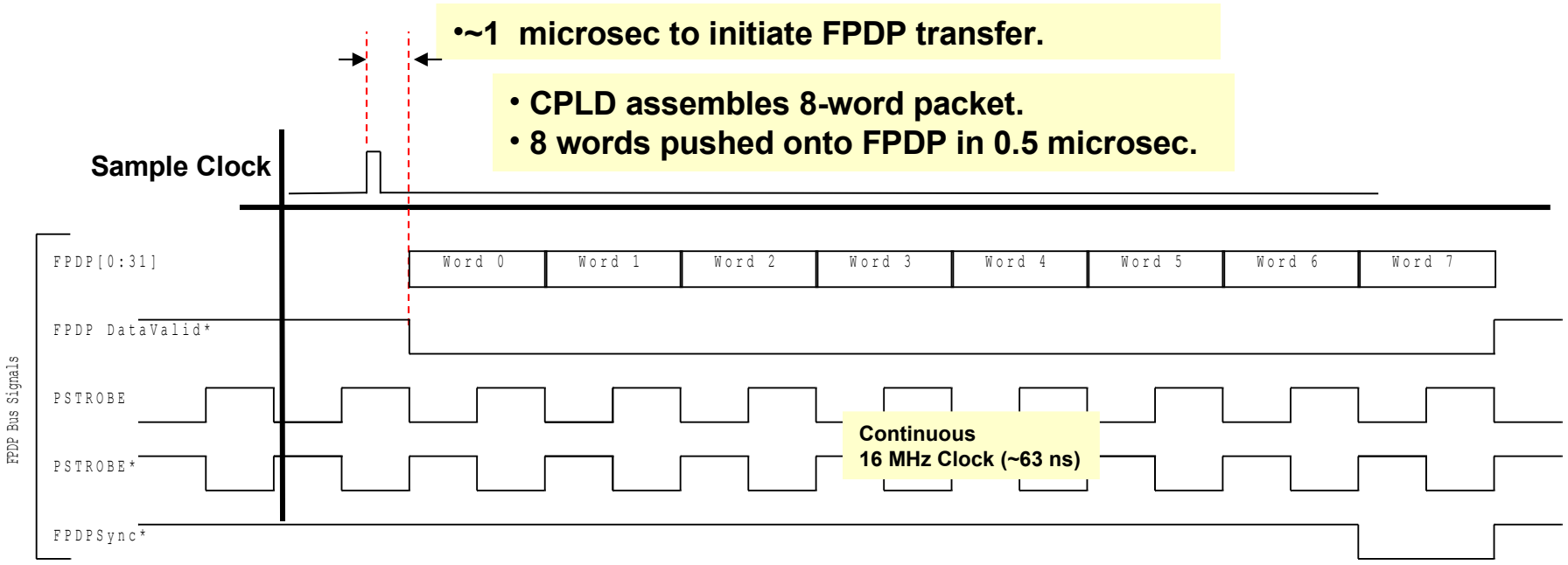
- The Front Panel Data Port (FPDP) is a 32-bit synchronous data flow path that allows data to be transfered at high speeds (160 MBytes/sec for FPDP-I and and 3.2 GBit/Sec for FPDP-II.).
- It is designed to have minimum latency for real-time applications
- The physical transmission media is ribbon cable for local connections and and fiber optic cable for longer distances.

- Some FPDP products available from the commercial sector.
- Due to the simple bus specification it is practical to develop cost-effective, in-house designs.

The CPLD

- Each FPDP module has a Complex Programmable Logic Device (CPLD) on it.
- The CPLD can be programmed and used to perform functions traditionally implemented using discrete components. Timing and logic changes do not require new circuit designs aor printed circuit board fabrication.
- Logic functions occur in hardware, it is not a processor. Timing and performance is deterministic to several nano-seconds.

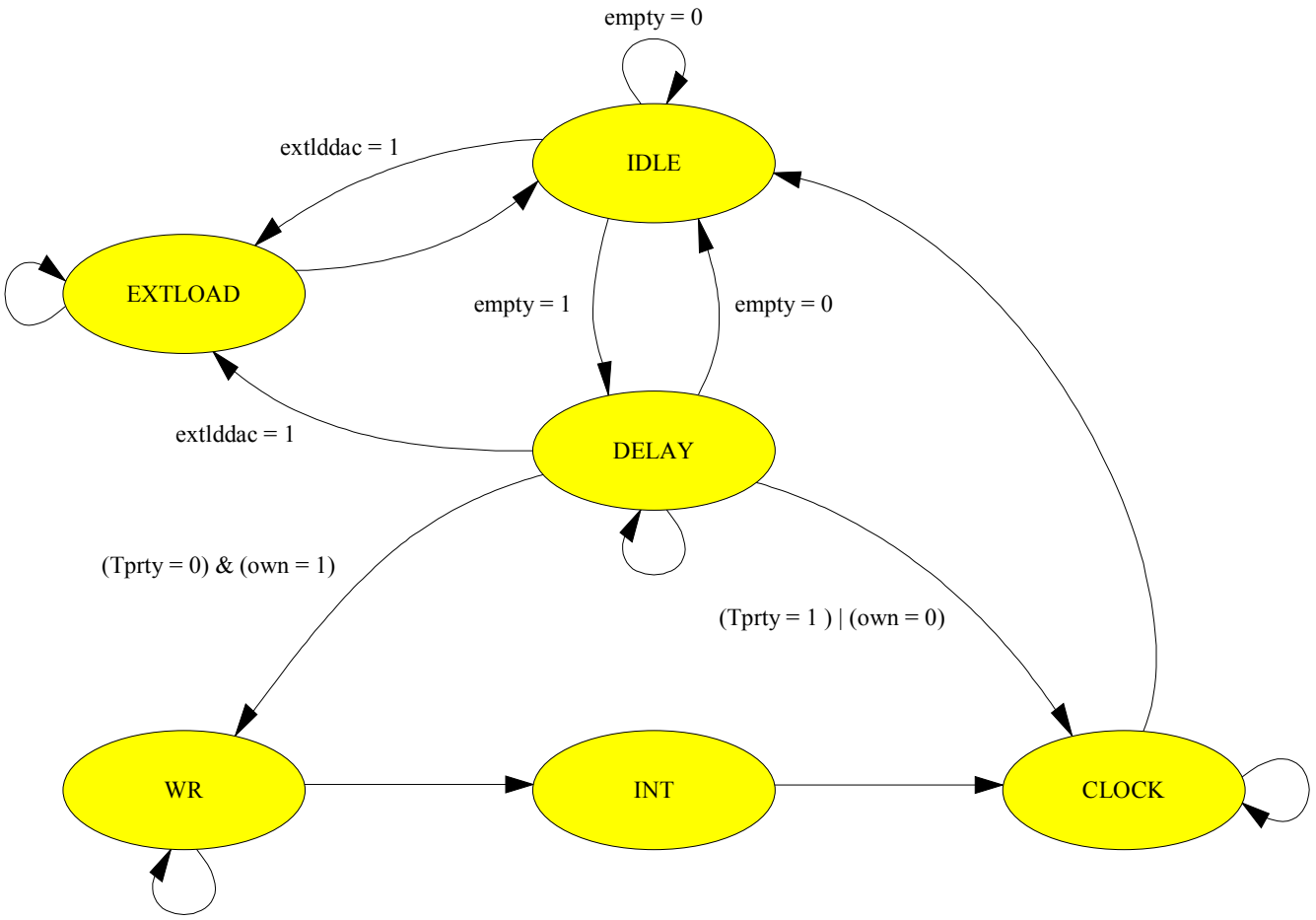
Typical Timing Diagram



Software Development

- The CPLD software was written in the **Verilog** language.
- The software was developed, tested, and simulated using in Xilinx's free **ISE** development environment.
- Several board-testing programs were written using **GTK+.**

CPLD programs incorporate the State-Machine model



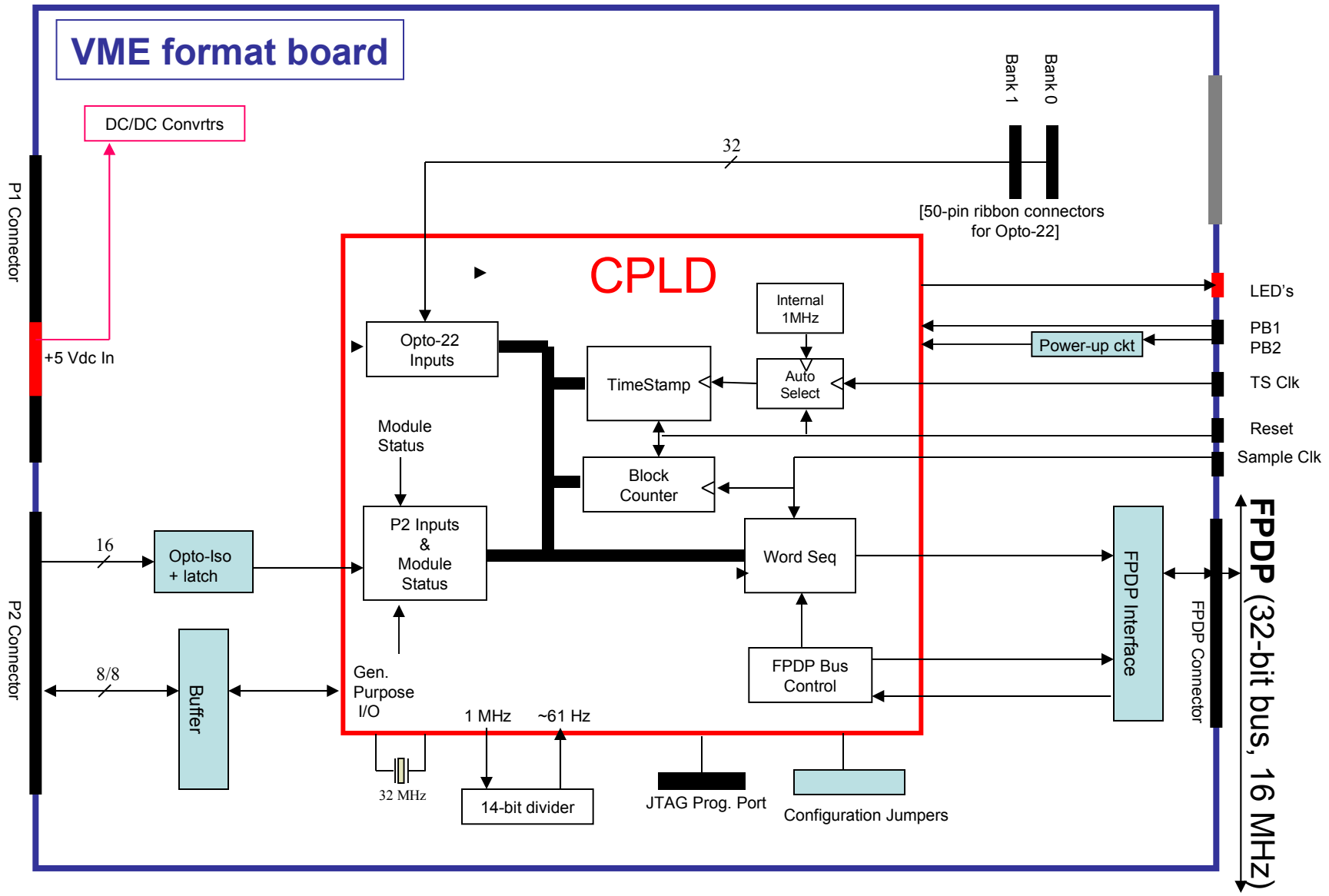
Digital Input and Time-Stamp Module
General Features

- The DITS pushes eight 32-bit words onto the FPDP bus. Separate multiplexor modules (FIMM) buffer and sequence data from multiple FPDP data sources to create a single input data stream for the *PCS Realtime Computer*.

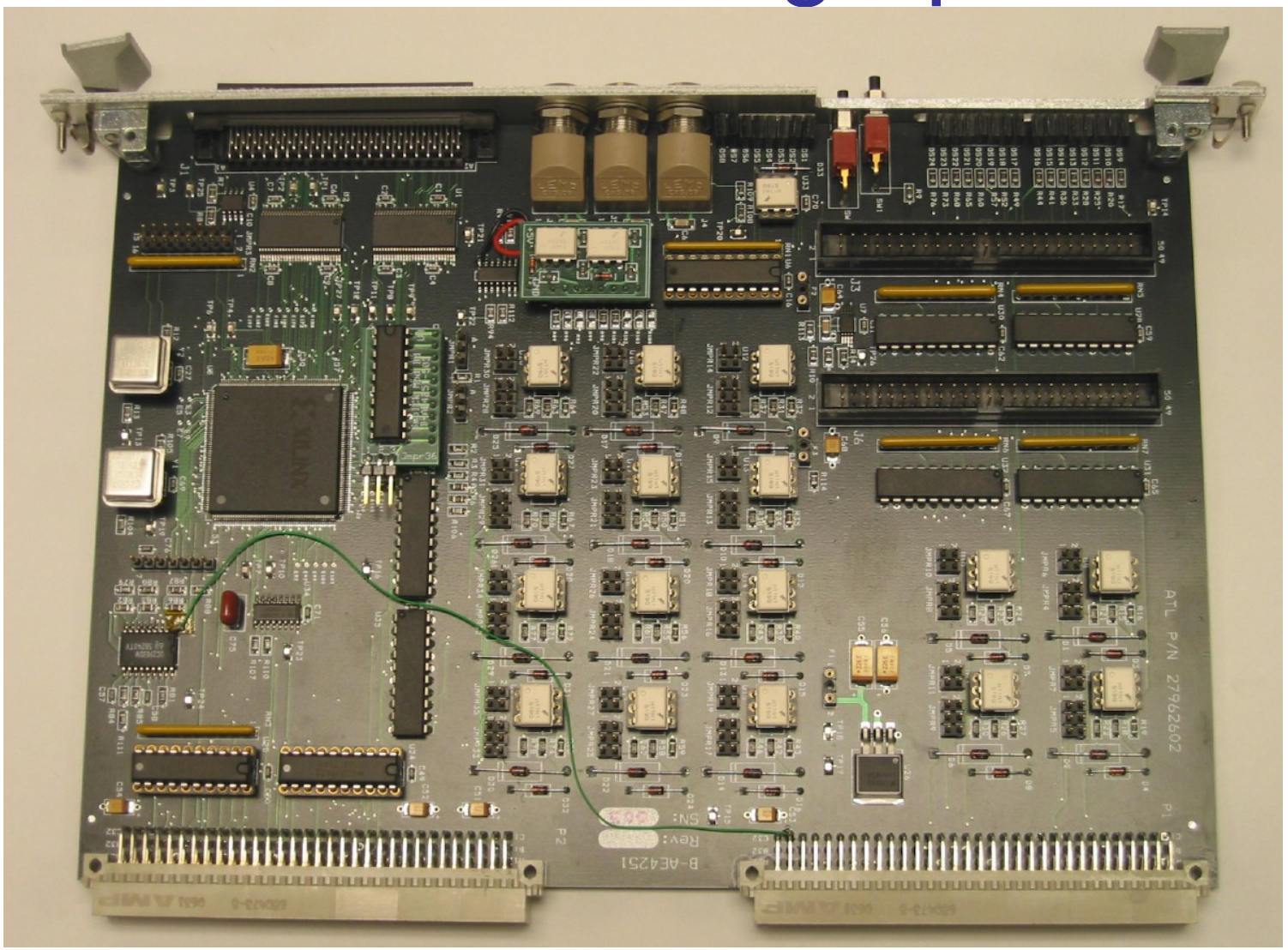
- The DITS provides a **Time-Stamp** for the PCS FPDP input data.
  - A 48-bit Time Stamp will come in with each 'block' of FPDP data and will indicate when the **PCS ADC Sample Clock** was received.
  - The timer has one microsecond accuracy.

- The DITS also provides (48) **Digital Inputs**:
  - (3) 16-bit banks of digital Input
    - 2 banks compatible with *external* Opto-22 modules.

DITS Block Diagram



DITS Photograph



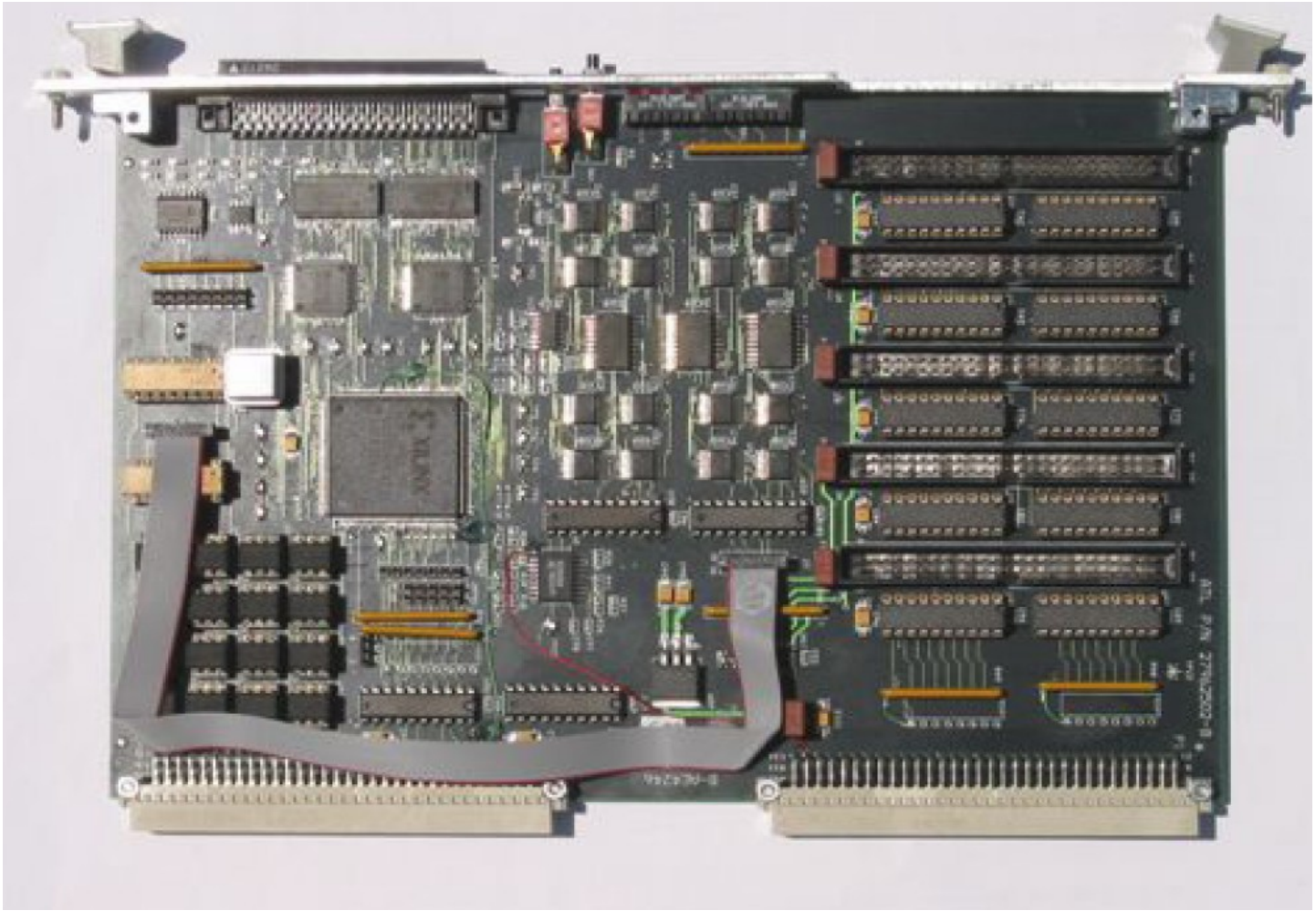
B-Size VME Board Format

FPDP Output Module / Digital

General Features

- 64 Digital Outputs commanded via FPDP
  - 4 banks of 16-bits, configured for use with external Opto-22 panel.
  - Double-buffered (separate *write*, *load* controls).
- Three types of output-synchronization.
- Timing:
  - FPDP word to output delay: 180 ns.
  - All 4 outputs processed in ~ 1 micro-sec?.

FOMD Photograph

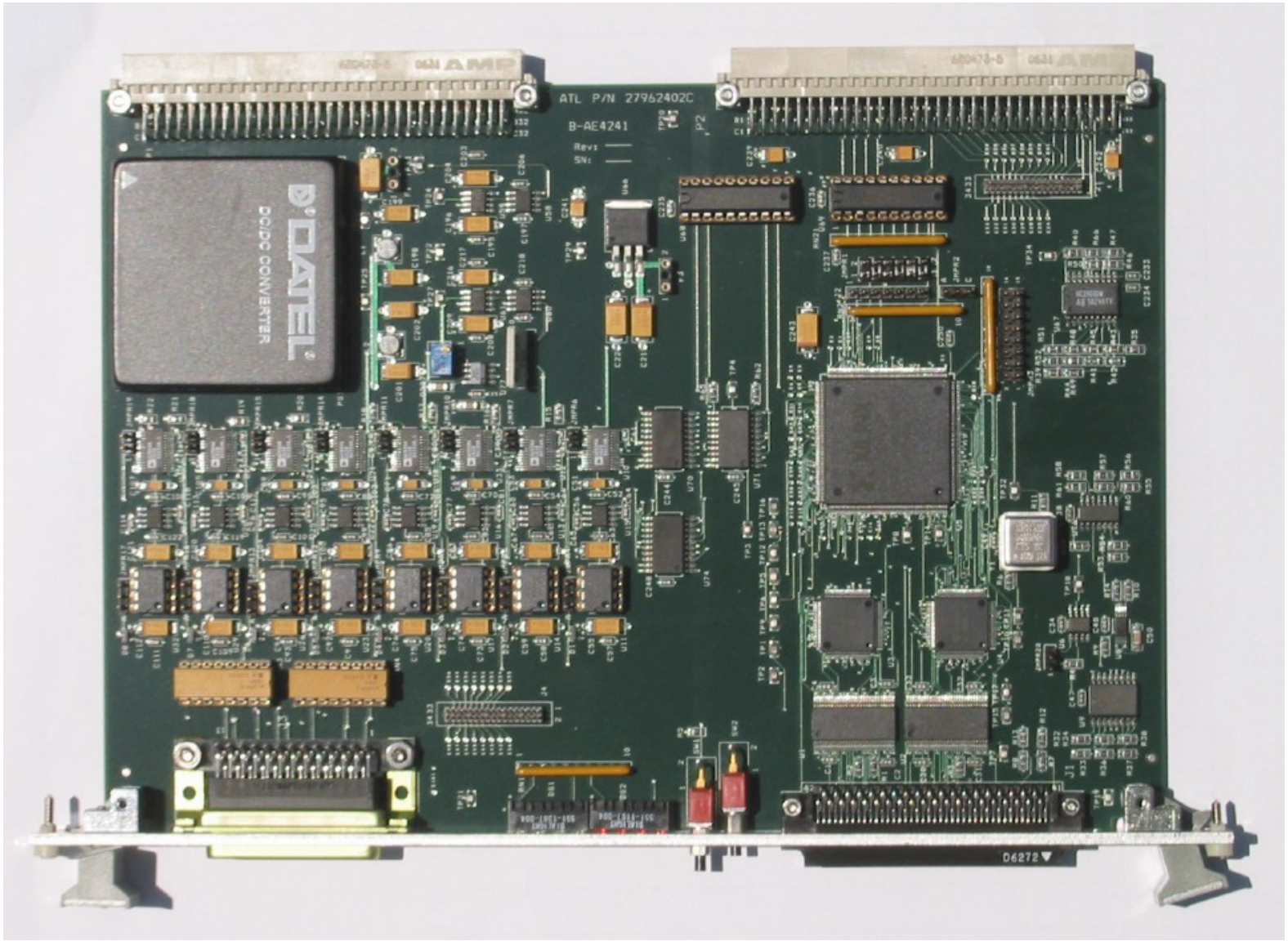


FPDP Output Module / Analog

General Features

- 8 Analog Outputs commanded via FPDP
  - 14-bit DAC, 160 KHz bandwidth
  - +/- 10.24 or 0-10.24 volt output ranges
  - Configurable ‘reset’ voltages.
  - Double-buffered (separate *write*, *load* controls)
- Three types of output-synchronization.
- Timing:
  - FPDP word to output delay: ~180 ns.
  - All 16 8 outputs processed in ~ 2.0 micro-sec.

FOMA Phototgraph



Summary

- Three FPDP input/output modules were developed at PPPL.
- The boards share common hardware and software design.
- The boards were used in production after the first manufacturing run.
- Each has a complete documentation package.