Procedure Title: NTSX Control System Latency Testing

Number **D-NSTX-PTP-ECS-060**	**Revision: 0**	Effective Date: **6/10/2008** Expiration Date: **6/10/2010** *(2 yr. unless otherwise stipulated)*

Procedure Approvals
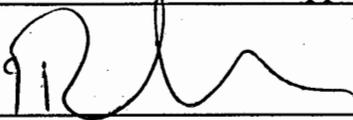
Author **R.E. Hatcher**   Date 6/10/08

ATI **R. Marsala**   Date 6/10/08

RLM **A. Von Halle**   Date 6/10/08

Responsible Division: **NCSX**
ST NSM

Procedure Requirements

LABWIDE:

☐	Work Planning Form #1050(ENG-032)	☐	Lockout/Tagout (ESH-016)
☐	Confined Space Permit (5008, Sec. 8, Chap 5)	☐	Lift Procedure (ENG-021)
☐	Master Equip. List Mod (GEN-005)	☐	ES&H Review (NEPA, IH, etc.)
☐	RWP (HP-OP-20)	☒	Independent Review
☐	ATI Walkdown	☐	Pre-job Brief
☐	Post-job Brief *		

D-SITE SPECIFIC:

☐	D-Site Work Permit (OP-AD-09)	☐	Door Permit (OP-G-93)
☐	Tritium Work Permit (OP-AD-49)	☐	USQD (OP-AD-63)
☐	Pre-job brief (OP-AD-79)	☐	T-MOD (OP-AD-03)
☐	DCA/DCN (OP-AD-104) # _____		

REVIEWERS (designated by RLM)
Accountable Technical Individual **R. Marsala**
Test Director T.B.D.
Independent Reviewer **J. Lawson**
D-Site Shift Supervisor
NSTX **R. Marsala, D. Gates, R. Camp**
TFTR Caretaking
Vacuum _____
Computer _____
Tritium _____
Quality Assurance/Quality Control _____
AC Power _____
Maintenance and Operations Division _____
Energy Conversion System/MG System
Environmental Restoration & Waste Management Division _____
Water _____
Neutral Beam (Heating Systems Branch of Electrical Engineering) _____
Radiofrequency (Heating Systems Branch of Electrical Engineering) _____
Diagnostics _____
Environmental, Safety, & Health

TRAINING (designated by RLM)			
No training required ☒ Instructor _____			
Personnel (group, job title or individual name)	Read Only	Instruction	Hands-On
_____ *ATI performs procedure*	☐	☐	☐
_____	☐	☐	☐
Training Rep. _____			
RLM _____			

1. PURPOSE

1.1 The procedure provides instructions to perform a latency test on the NSTX plasma control system.

2. SCOPE

2.1 The scope of this procedure includes:

• Steps required to place the control system hardware into a configuration compatible with latency testing;

• Steps required to place the control system software in a configuration compatible with latency testing; and

• Steps required to acquire the Latency Test System permissive key from the COE.

3. REFERENCES

1. D/D-SITE-OP-AD-39, Conduct of Operations.

2. ENG-030, PPPL Technical Procedures for Experimental Facilities.

3. OP-AD-56, Control of Equipment and Status.

4. RESPONSIBILITIES

Head of NSTX Operations: Shall appoint Test Director

Head of NSTX Operations: _____ *Init.* _____

Test Director: Overall responsibility for conduct of tests, and documentation of results in the form of a Test Record (completed Run Copy, Test Data Sheets, and any other relevant data or information collected during the tests).

Run Copy Test Director: _____ *Init.* _____

PSRTC Operator: Responsible for configuration of the real-time power supply control software (PSRTC).

PSRTC Operator: _____ *Init.* _____

Physics Operator: In conjunction with the Test Director shall direct the testing, interpret the data, and decide when testing is complete.

Physics Operator: _____ *Init.* _____

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5. PREREQUISITES

5.1 The Test Director shall ensure that the following prior to the start of testing:

5.1.1 The NSTX COE shall ensure that the NSTX coil system power supplies are both disarmed and disabled but otherwise in a state to allow Latency testing.

NSTX COE   Init. _____

5.1.2 An authorized PSRTC operator is available to configure input files or the PSRTC GUI for the test(s).

PSRTC Operator: _____   *Test Director   Init.* _____

5.1.3 An NSTX Physics Operator is available to direct the testing and to interpret the test results.

Physics Operator: _____   *Test Director Init.* _____

5.2 The COE shall remain available throughout the testing and shall ensure the Latency Testing permissive key is returned and secured at the end of testing.

6   Latency Testing

6.1   The Test Director shall obtain the Latency Testing permissive key from the COE.

Test Director   *Init.* _____   *NSTX COE*   *Init.* _____

6.2   The PSRTC operator shall (using the GUI or appropriately modified files):

6.2.1   Ensure that PSRTC is in the "PCS" mode.

6.2.2   Ensure that PSRTC is in the "nohcs" mode.

6.2.3   Ensure that the variable VDOTMAX is set to 1e6 for all systems in the GUI or in the c.d file.

6.2.4   Start the PSRTC process checking to make sure that there are no errors which would normally prevent a successful clock cycle.

PSRTC Operator   *Init.* _____

6.3   The NSTX physics operator shall ensure that the waveform for the system under test is identically zero over the normal active interval (-0.75 s $\leq$ t ≤ 1.4 s).

6.4   With concurrence of the COE the Test Director may at this time use the key obtained in 6.1 to enable the Latency Test hardware. (Note that this causes a Level 3 fault in FCPC which is intercepted by the hardware to simplify the tests).

Test Director   *Init.* _____

6.5   The COE shall attempt to reset the Level 3 fault caused by the actions of step 6.4 and ensure that the fault remains "in effect" for the power supplies.

NSTX COE   *Init.* _____

6.6   At this point the Physics Operator may conduct tests, as appropriate, using the NSTX clock cycle.

7   RE-CONFIGURING FOR NORMAL OPERATION

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7.1   Once testing is complete the Test Director shall disable the Latency Test hardware, remove the permissive key and return it to the COE.

Test Director   Init. _____   *NSTX COE*   Init. _____

7.2   The NSTX COE shall secure the Latency Test key which closes out this procedure.

Latency Test Key Secure   *NSTX COE*   Init. _____

7.3   Once the Latency Test key is secured, the COE may clear the Level 3 fault and have the Test Director (or his designee) reset the ACP to allow operations to proceed.