National Spherical Torus eXperiment Upgrade

Shorted Turn Protection System
WBS 1.10.01.01

NSTX-U Recovery Project FDR – March 17-19, 2020

Greg Tchilinguirian - Cognizant Engineer

Last edit: 3/10/20

Outline

1. Overview
2. Scope
3. Requirements and Interfaces
4. Analysis/Prototyping
5. Chit Closure
6. Procurement, Fabrication, Installation, and Test
7. Risk - Project Risks and Design FMECA
8. Quality, Environmental, Safety, and Health
9. Summary

Overview - WBS 1.01.02.04

(CDE-3B Scope)

WBS Title	Shorted Turn Protection System	WBS #	1.10.01.01
Project Cog.	Greg Tchilinguirian	Assoc. Proj. Man.	Tom Jernigan
Design Scope	Design a realtime system to look for coil terminal arcs, layer-to-layer faults, and other current - voltage anomalies		
Technical Impact of Scope	As part of the larger coil protection system, provide enhanced protection again terminal and other arcs that might lead to very long outages		
Design Status	FDR completed on 1/23/2020 (link) chits: link calculations: N/A drawings: link SoW/Tech Spec: link		
Fabrication Status	Awaiting CDE-3B ESAAB approval		
Installation Status			

Outline

1. Overview
2. Scope
3. Requirements and Interfaces
4. Analysis/Prototyping
5. Chit Closure
6. Procurement, Fabrication, Installation, and Test
7. Risk - Project Risks and Design FMECA
8. Quality, Environmental, Safety, and Health
9. Summary

Shorted Turn Protection (STP) Fits Within the Larger Coil Protection Context

Fault Condition	Coil Protection System	Status
Coil and bus work ground faults	Power conversion ground fault detection	Existing
Coil overcurrent	Digital Coil Protection System	Existing
excessive pulse I^2t	Digital Coil Protection System	Existing
excessive mechanical force/torque/moment	Digital Coil Protection System	Existing
magnet pulses with insufficient time between pulses	Pulse Duration and Period Timer	Existing
Elevated temperature at start of pulse	Cooling water interlocks	Existing
Coil terminal & layer-to-layer faults	Shorted Turn Protection system	**NEW**

The STP is credited in the Project FMECA with mitigation of arcs at the terminal leads, at water feeds, etc;
Note: turn-to-turn faults within coils may not be possible to detect with STP, but the reduction of risk for terminal arcs makes the system valuable

Scope Introduction

What will the system do:

- Compare currents measured in real-time to those predicted from applied voltages based on reduced coil/vessel/plasma circuit model'

What does this difference mean?

- Current is flowing in areas where it was not intended to. The system can detect changes in the resistance + inductance circuit against a model in real-time.

What is the scope of this work?

- Design/procure voltage measurement & support equipment
- Add to NSTX-U's real-time computing/processing infrastructure
- Develop Real-time Software
- Modify system test Infrastructure
- Generate algorithm code using MatLab Simulink for operational support

Scope Introduction

Scope Detail

- Design/procure voltage measurement & support equipment
  - Replace existing (TFTR Era) Ross Voltage dividers with pairs of matched units for redundancy
  - Build Amplifiers, install in Ross amplifier locations
  - Use existing cabling from FCPC to Junction area (tested)
- Add to NSTX-U's real-time computing/processing infrastructure
  - New Real-Time iHawk system, will use Centos 7
  - Use spare Real-time Clock & Interrupt Module (RCIM) interface chassis for timing and signaling
- Develop real-time software
  - Re-use some existing code, design elements.
- Modify system test infrastructure
  - Add analog output card to Autotester, update VI to output current
- Generate Algorithm code using MatLab Simulink for operational support
  - New capability, tested on current real-time equipment
  - Integrate into real-time Linux software/infrastructure

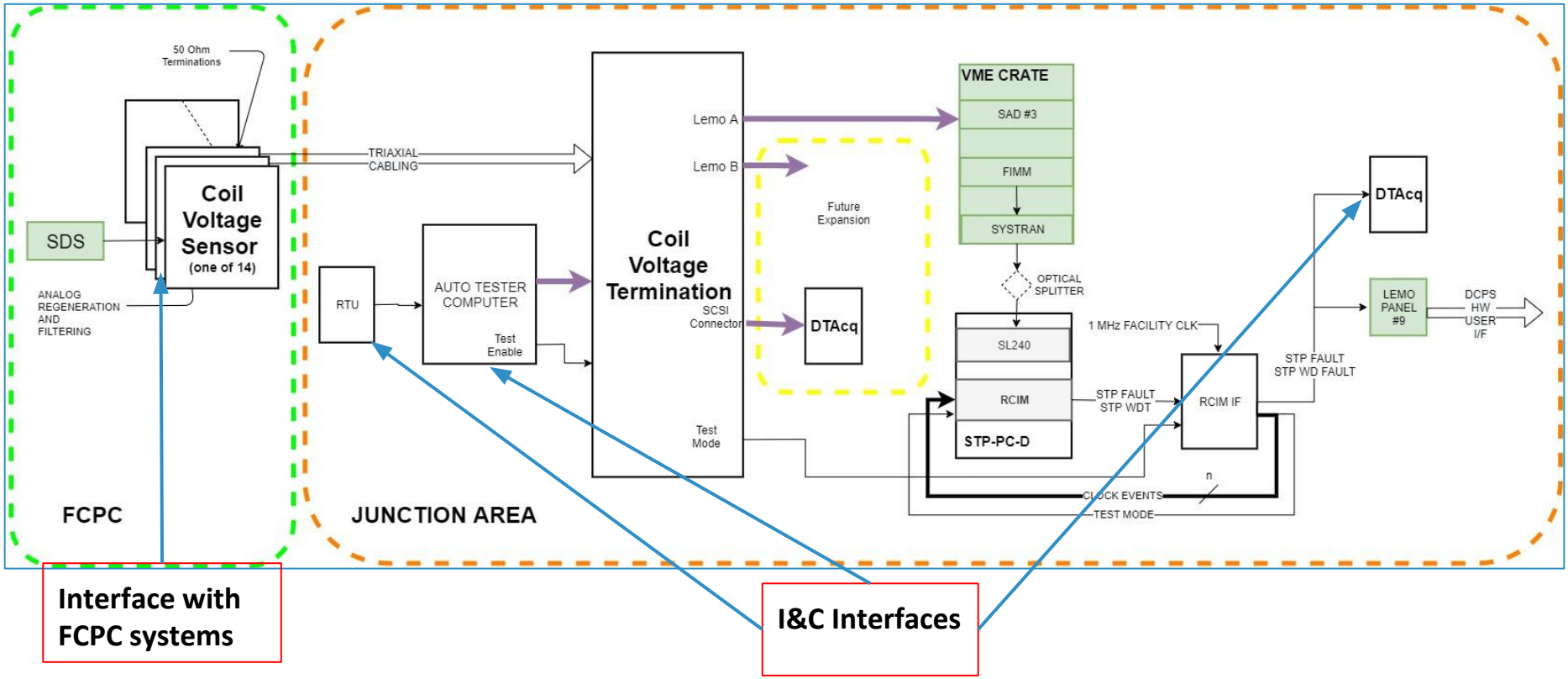
Outline

1. Overview
2. Scope
3. Requirements and Interfaces
4. Analysis/Prototyping
5. Chit Closure
6. Procurement, Fabrication, Installation, and Test
7. Risk - Project Risks and Design FMECA
8. Quality, Environmental, Safety, and Health
9. Summary

Requirements Defined and Met

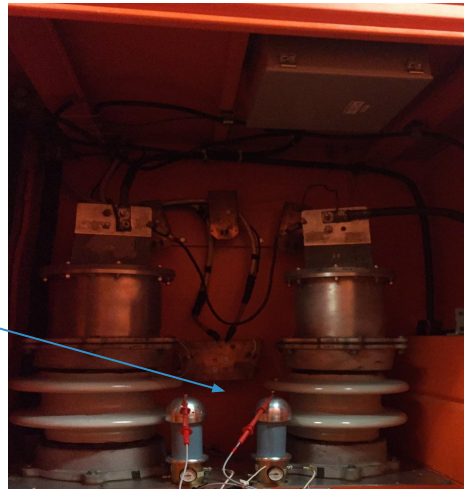
Source	Requirements	Comment	met
NSTX-U-RQMT-GRD-001			✔
NSTX-U-RQMT-SRD-008(5.3.1)	Data Stream	what is digitized, calibrations, auctioneering, secure input parameter data	✔
NSTX-U-RQMT-SRD-008(5.3.2d)	Fail Safe Design	Fail safe design required (active high, watchdogs, etc)	✔
NSTX-U-RQMT-SRD-008(5.3.3)	Timing	Shall be aligned with the facility clock, protect from SoP to EoP	✔
NSTX-U-RQMT-SRD-008(5.4a)	Sensitivity Requirements	terminal arcs, layer-to-layer faults, arcs at water feed, etc.	✔
NSTX-U-RQMT-SRD-008 (5.4b)	Fault Requirements	detected fault, timing error, input mismatch	✔
NSTXU_1-7-3-6-9_RD-100 (3)	Functions	monitor and model the NSTX-U coil currents/voltages, declare an L1 fault in the event of an anomaly	✔
NSTXU_1-7-3-6-9_RD-100 (4)	Design Requirements	Conform to industry standards for electronics, use of vendor-supported or open source software, etc	✔
NSTXU_1-7-3-6-9_RD-100(6)	Baseline Performance & Operational Requirements	Measurement, timing, processing and output performance - react to timing and input signals, process data through models and output status/faults	✔

The Design Accommodates Required Interfaces



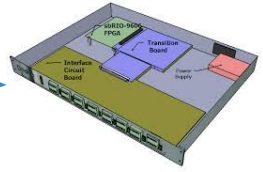
The Design Accommodates Required Interfaces

1. Shorted Turn Protections system interfaces with Field Coil Power Conversion (FCPC) at the voltage dividers
2. Shorted Turn Protection System interfaces with I&C Plant Control and Monitoring System
3. Shorted Turn Protection System interfaces with I&C Data Archiving System
4. Shorted Turn Protection System interfaces with I&C Timing system



EPICS

MDSplus



Details of Interfaces Defined in Interface Control Documents

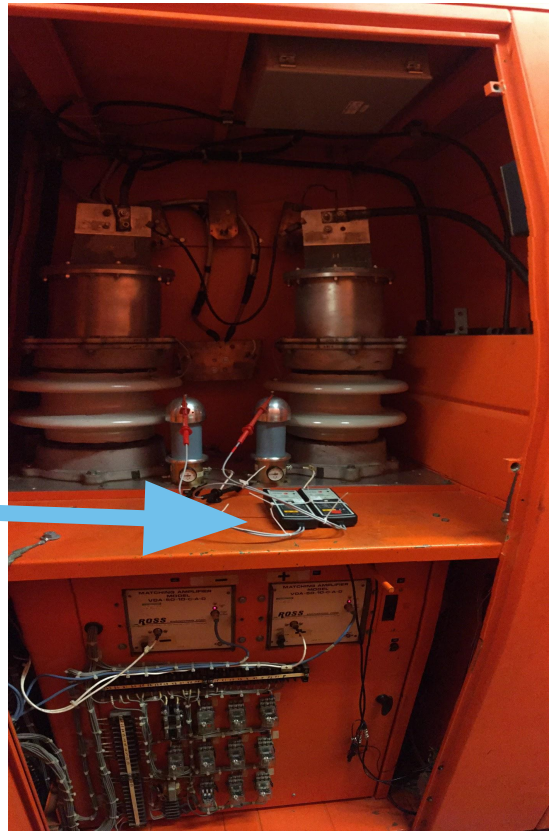
System 1	System 2	ICD Link	Exposition
Integrated Machine Operations	Power Systems	link	Defines interface between the Machine Instrumentation and CI&C
Integrated Machine Operations	CI&C	link	Defines interface between the Machine Instrumentation and CI&C

Outline

1. Overview
2. Scope
3. Requirements and Interfaces
4. Analysis/Prototyping
5. Chit Closure
6. Procurement, Fabrication, Installation, and Test
7. Risk - Project Risks and Design FMECA
8. Quality, Environmental, Safety, and Health
9. Summary

Voltage Testing

- **Intent:**
  - Confirm quality of *differential* voltage measurements in the FCPC.
  - Compare with measurements using existing equipment.
- **Methodology:**
  - Use dummy load coil to simulate actual conditions
  - Utilize COTS HV probes.
    - Calibrated.
    - Data recorded with local o-scope.
- **Recorded Data:**
  - +/- Differential Voltage.
  - Firing Angle from Alpha cart via MDS+.
  - Ross voltage data via MDS+ (for comparison).



FCPC SDS Cabinet

Voltage Testing

Shorted Turn Protection (STP) requires voltage and current measurements

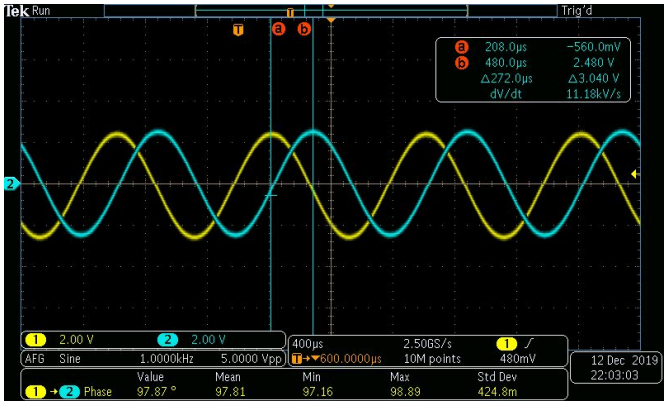
- Current measurements already exist
- Existing voltage measurements are not available for Control and Protection.

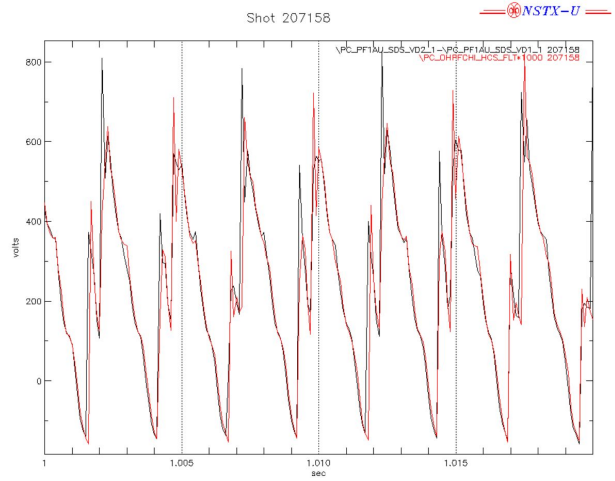
Existing voltage data acquisition hardware is from "TFTR Era"

- Many broken sensors.
- Non-robust hardware/expensive to maintain.
- Hardware is geared for 30KV (lacking in dynamic range for our purposes).

Conclusion:

- It is possible to acquire signals of sufficient quality to enable the STP system to meet requirements.





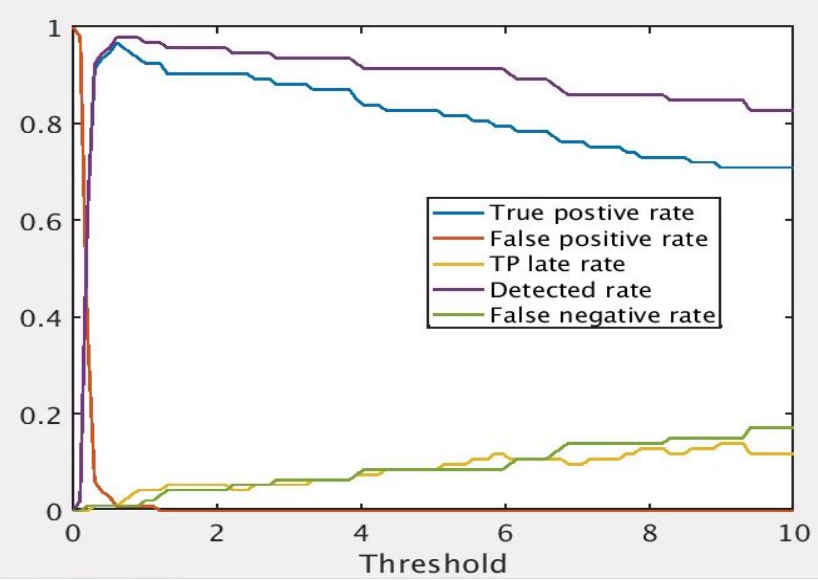
Black = Ross (pos-neg trace)

Red = HV Probe

Algorithm Testing

- Simulate many fault conditions to develop database
- Shot type
  - Single coil 100% test shot
  - Combined field vacuum shot
  - Plasma shot
- Randomly select
  - Coil to fault
  - Time to initiate fault
  - Fault conditions
    - % of turns shorted (0-100%)
    - Short resistance (as % of nominal resistance) (1%-200%)

- Compare classification rates to select fault thresholds



Outline

1. Overview
2. Scope
3. Requirements and Interfaces
4. Analysis/Prototyping
5. Chit Closure
6. Procurement, Fabrication, Installation, and Test
7. Risk - Project Risks and Design FMECA
8. Quality, Environmental, Safety, and Health
9. Summary

Chit Closure is Closing Out

All pre-FDR Chits addressed and closed before the FDR

10 CHITS were generated by the FDR, now closed as well

APPROVED
PPPL

PPPL PRINCETON PLASMA PHYSICS LABORATORY

ENG-033 - CRR - CHIT RESOLUTION REPORT

RTC&P SHORTED TURN PROTECTION CHIT RESOLUTION REPORT

NSTXU_1-7-3-6-9_CRR_100

Rev. 2

Work Planning #: **3066**
Effective Date: **03/10/2020**
Prepared By: **Greg Tchilinguirian**

Reviewed By	Frank Hoffmann, Responsible Engineer	03/09/2020 09:55:12 AM
Reviewed By	Yuhu Zhai, Project Engineer	03/09/2020 08:30:25 AM
Approved By	Robert A. Ellis, Chief Engineer	03/10/2020 09:19:04 AM

Chit Resolution Report: link

Outline

1. Overview
2. Scope
3. Requirements and Interfaces
4. Analysis/Prototyping
5. Chit Closure
6. Procurement, Fabrication, Installation, and Test
7. Risk - Project Risks and Design FMECA
8. Quality, Environmental, Safety, and Health
9. Summary

Procurement Plan

Four procurements are key executing the impementation of the Shorted Turn Protections System

1. Procure Matched Voltage Dividers (up to 16 week lead time)
   - Vendor advocated continuous delivery of units as they are produced
2. Procure production-ready amplifier boards (PPPL design)
   - Spin 1 board currently undergoing bench tests prior to production run following CDE-3B ESAAB approval.
3. Procure custom amplifier board enclosures
4. Procure Real-Time computers
   - Upgrade of development system to current OS/SW
   - Procurement of additional system matched to development system

Fabrication

Voltage Measurement:

- Amplifier boards will be built and stuffed offsite
- Final assembly and bench test will occur on-site
- Expected to take 3 months of work to build, install and test voltage measurement equipment.

Software:

- UML design has been turned into a C++ framework
- Development of the alpha test code will commence after 3B approval

Integration & Testing

Strategy:

- Install Amplifier and Voltage DIviders during periods between Coil tests
- Test system one SDS cabinet at a time
- Utilize “autotester” (already developed for a different system) to develop real-time software in parallel
  - Has been used to drive framework design element already
- Develop Data “scenarios” to challenge function of system during development

Outline

1. Overview
2. Scope
3. Requirements and Interfaces
4. Analysis/Prototyping
5. Chit Closure
6. Procurement, Fabrication, Installation, and Test
7. Risk - Project Risks and Design FMECA
8. Quality, Environmental, Safety, and Health
9. Summary

Project Risks are Actively Being Managed

Risk	Score (1-81)	Open/Retired	Risk Retirement Event
No WBS-specific risks for this control account			

Many risks (delivery delays) held at the Project level

FMECA (I)

System	Failure Mode	Failure Cause	Failure Effect	R	Detection/ Mitigation System (1)	Detection/ Mitigation System (2)	Detection/ Mitigation System (3)	R_R
Shorted Turn Protection System	RCIM Interface Chassis (RIC) fails to detect clock events	Electronics failure, wiring failure	No Clock events, system times outs- system faults	6	Shorted Turn Protection System	None	None	6
Shorted Turn Protection System	RCIM Interface Chassis (RIC) fails to output a fault	Electronics failure, wiring failure	System is basically dysfunctional	6	Shorted Turn Protection System	None	None	6
Shorted Turn Protection System	RCIM Interface Chassis fault output cabling fails	cable is snagged by a worker; cable degradation over time; inadvertent or errant disconnection	active-high input to DCPS interface panel falls low, leading to L1 fault	6	Shorted Turn Protection System	None	None	6
Shorted Turn Protection System	RCIM Interface Chassis WDT output cabling fails	cable is snagged by a worker; cable degradation over time; inadvertent or errant disconnection	active-high input to DCPS interface panel falls low, leading to L1 fault	6	Shorted Turn Protection System	None	None	6
Shorted Turn Protection System	RCIM Interface Chassis electronics freezes in unsafe state	Electronics failure	WDT output (that which is sent to the interconnection chassis) is no longer indicative of the health of the computer	6	Plant Control and Monitoring	None	None	6

FMECA (II)

System	Failure Mode	Failure Cause	Failure Effect	R	Detection/ Mitigation System (1)	Detection/ Mitigation System (2)	Detection/ Mitigation System (3)	R_R
Shorted Turn Protection System	Computer: General Hardware Failure (hard drive, motherboard, etc)	Age; thermal excursions in JA; quality issue	No watchdog timer, system Faults	6	Shorted Turn Protection System	None	None	6
Shorted Turn Protection System	Computer loses connection to MDS+ server when reading setup parameters	Network failure; MDS+ server problem	STP cannot get setup parameters; declares a fault	6	Shorted Turn Protection System	None	None	6
Shorted Turn Protection System	Software lock-up during pulse	Hardware issue; input to software that generates an untested response	Watchdog timer stops; loss of toggling is detected by RCIM Interface Chassis, fault is declared.	6	Shorted Turn Protection System	None	None	3
Shorted Turn Protection System	Loss of power to JA Racks	Breaker trip at many levels of the AC power infrastructure of the lab; site-wide power outage	Power loss to all equipment. Active-high fault line goes low - fault declared	6	Shorted Turn Protection System	DCPS Software	None	6
FPDP Data Stream	Loss of data stream	Electronics failure, fiber breakage, etc leads to the FPDP stream failing	Data stream stops updating, is detected by STP SW, system declares fault	6	Shorted Turn Protection System	DCPS Software	None	6

FMECA (I)

System	Failure Mode	Failure Cause	Failure Effect	R	Detection/ Mitigation System (1)	Detection/ Mitigation System (2)	Detection/ Mitigation System (3)	R_R
Rectifier DC Systems	Resistor on low-voltage side of divider fails open	Quality issue in manufacture, beyond-design-basis voltage transient	high voltage applied to the input of the amplifier in the SDS cabinets, but through high resistance. Fuse-like features in signal conditioners open. Inconsistent voltage measurement recorded by redundant sensor, leading to STP fault.	4	Shorted Turn Protection System	FCPC Ground Fault Detection	None	4
Rectifier DC Systems	Resistor on low-voltage side of divider fails closed	Quality issue in manufacture, beyond-design-basis voltage transient	inconsistent voltage measurement recorded by redundant sensor, leading to STP fault.	4	Shorted Turn Protection System	None	None	4
Rectifier DC Systems	Signal conditioning electronics for voltage measurement fails - lower-than-actual voltage indicated	Electronics failure	inconsistent voltage measurement recorded by redundant sensor, leading to STP fault.	4	Shorted Turn Protection System	None	None	4

FMECA (II)

System	Failure Mode	Failure Cause	Failure Effect	R	Detection/ Mitigation System (1)	Detection/ Mitigation System (2)	Detection/ Mitigation System (3)	R_R
Rectifier DC Systems	Current transducer fails - less than actual current indicated	Failure of the measurement head or signal processing electronics.	Inconsistent current measurement, system Faults	3	Shorted Turn Protection System	DCPS Software	None	3
Rectifier DC Systems	Current transducer fails - greater than actual current indicated	Failure of the measurement head or signal processing electronics.	Inconsistent current measurement, system Faults	3	Shorted Turn Protection System	DCPS Software	None	3
Shorted Turn Protection System	Computer RCIM Card Failure	Age; thermal excursions in JA; quality issue	No STP fault output and no watchdog timer output (the latter leading to system fault)	3	Shorted Turn Protection System	None	None	3
Shorted Turn Protection System	Clock events come in unexpected sequence	Failure of the clock system	SW detects events coming in out of sequence and declares STP fault	3	Shorted Turn Protection System		None	3
Shorted Turn Protection System	Computer loses connection to MDS+ server when archiving data	Network failure; MDS+ server problem	STP cannot archive, declares fault	3	Shorted Turn Protection System		None	3
Shorted Turn Protection System	Power loss on realtime computer during pulse	breaker trip, power cable comes unplugged	Active-high STP fault signal goes low; FCPC L1 fault declared	3	Shorted Turn Protection System	None	None	3

System	Failure Mode	Failure Cause	Failure Effect	R	Detection/ Mitigation System (1)	Detection/ Mitigation System (2)	Detection/ Mitigation System (3)	R_R
Shorted Turn Protection System	Improper test mode status indicated from RCIM interface panel to STP computer	RCIM Failure, cable failure, improper input to software	Inconsistent state between software and hardware results in STP fault	3	Shorted Turn Protection System	None	None	3
Shorted Turn Protection System	Front panel test mode switch fail in closed position	Mechanical failure, cable failure	Inconsistent voltage and current signals result in STP fault	3	Shorted Turn Protection System	None	None	3
Rectifier DC Systems	Signal conditioning electronics for voltage measurement fails - higher-than-actual voltage indicated	Electronics failure	inconsistent voltage measurement recorded by redundant sensor, leading to STP fault.	2	Shorted Turn Protection System	None	None	4

FMECA (III)

System	Failure Mode	Failure Cause	Failure Effect	R	Detection/ Mitigation System (1)	Detection/ Mitigation System (2)	Detection/ Mitigation System (3)	R_R
Rectifier DC Systems	Resistor on high-voltage side of divider fails open	Quality issue in manufacture, beyond-design-basis voltage transient.	inconsistent voltage measurement recorded by redundant sensor, leading to STP fault.	4	Shorted Turn Protection System	None	None	4
Rectifier DC Systems	Resistor on high-voltage side of divider fails closed	Quality issue in manufacture, beyond-design-basis voltage transient	High voltage applied to signal conditioner electronics in SDS cabined, likely causing catastrophic failure of the electronics; protection features on boards prevent transmission of voltage to junction area; inconsistent voltage measurement recorded by redundant sensor, leading to STP fault.	4	Shorted Turn Protection System	FCPC Ground Fault Detection	None	4

All failure modes have acceptable risk

See memo on reliability requirements and redundancy: link

Outline

1. Overview
2. Scope
3. Requirements and Interfaces
4. Analysis/Prototyping
5. Chit Closure
6. Procurement, Fabrication, Installation, and Test
7. Risk - Project Risks and Design FMECA
8. Quality, Environmental, Safety, and Health
9. Summary

Safety and QA Concerns

Safety:

- Typical for installation and field work performed
- Access to High voltage components governed by FCPC procedures, LOTO

QA:

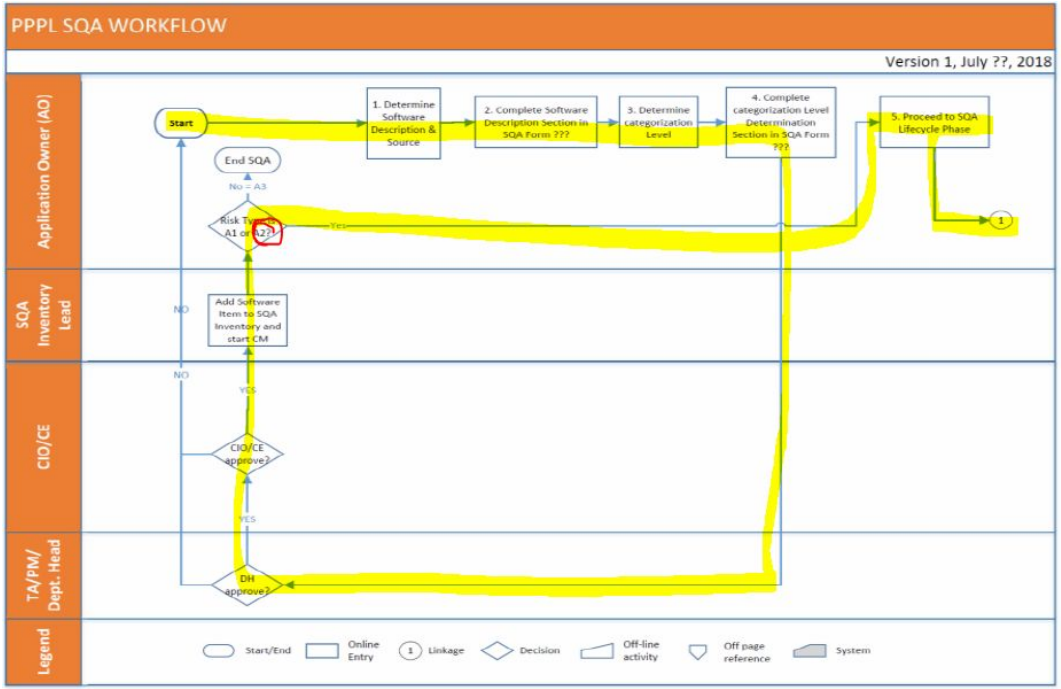
- Ross Engineering is an approved A1 vendor.
- Amplifier and Interconnection Boards are A3 but will be tested upon receipt an end-to-end after installation.

Software Quality Assurance

The software component of this system has been categorized through engineering process as A2.

Many controls are needed for SQA compliance, will utilize:

- Bugzilla System for Defect tracking
- NSTX-U's Software Change Notification (SCN) System
- Software Framework and test code is under revision control (SVN) already



Outline

1. Overview
2. Scope
3. Requirements and Interfaces
4. Analysis/Prototyping
5. Chit Closure
6. Procurement, Fabrication, Installation, and Test
7. Risk - Project Risks and Design FMECA
8. Quality, Environmental, Safety, and Health
9. Summary

Summary

- Requirements have been met via a combination of analysis and test.
- Interfaces are considered in the design and documented in the ICDs
- All chits related to the Shorted Turn Protections job are closed
- Risks are in line with projects risks (staffing, scheduling)
- Tasks are sufficiently discrete and isolated to multiplex well with other project activities.
- Safety issues were identified and addressed through engineered and administrative controls.